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Energy Efficient Approximate 8-bit Vedic Multiplier

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Abstract: ***The digital signal processing and its classification applications on the energy constrained devices should be supported based on efficiency. Because such applications must perform highly complex computations especially complex multiplication processes while exhibiting tolerance for a large amount of noise and for computational errors too. So, comparing all the arithmetic computations, improving the energy efficiency of multiplication is critical. In this project, an energy efficient approximate 8-bit Vedic multiplier is proposed which gives a tradeoff between computational accuracy and energy consumption. The proposed architecture has reduced area compared to other multiplier architectures which process same number of bits. The reduced architecture area reduces the power consumption. Also, the Vedic technology adopted for the multiplication reduces the delay further. But the approximate architecture output possesses a small amount of computational accuracy which is negligible for DSP applications.***

Keywords*: *Digital Signal Processing, Energy Efficient, Vedic Multiplier, Approximate Multiplier Verilog HDL, and Simulations

I. INTRODUCTION

For today's electronic world embedded system and mobiles, energy consumption is a critical design problem lot of efforts have already been taken at various levels for improving the energy efficiency. Among other arithmetic operations, multiplication is the most time and power consuming operation. It becomes more significant for large operands and complex multiplication. Considering these constraints, a new approximate multiplier is proposed. This new method can provide much more energy efficiency than the truncated methods. The error rate is low because it effectively captures the noteworthy lower bits. For DSP and its classification algorithm, generally one of two operands in the multiplication is stored in the memory. Here it is exploited to improve the energy efficiency of the approximate multiplier further. The area can be effectively reduced by the proposed approximate multiplier because many adders and gates can be excluded in this method as compared to other multipliers. Within the approximate multiplier architecture, a Vedic technology is used for the multiplication which reduces the delay in the multiplication. As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amount of energy. While performance and Area remain to be the two major design tolls, power consumption has become a critical concern in today's VLSI system design. The need for low-power VLSI system arises from two main forces. First, with the steady growth of operating frequency and processing capacity per chip, large currents must be delivered and the heat due to large power consumption must be removed by proper cooling techniques. Second, battery life in portable electronic devices is limited. Low power design directly leads to prolonged operation time in these portable devices. Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore, low-power multiplier design has been an important part in low power VLSI system design. There has been extensive work on low-power multipliers at technology, physical, circuit and logic levels. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas.

II. MULTIPLIER MODULE

A. Vedic Multiplier

The Booth multiplication algorithm and Array multiplication algorithm are associated with high propagation time. But the fast multiplication process is defined by Vedic Mathematics. The Veda means store of knowledge. The Vedic mathematics means storage of knowledge of mathematics related to the high-speed operations.

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This Vedic mathematics provides the knowledge of varies area of mathematics like arithmetic, algebra, geometry using 16 important sutras. The method given in the Vedic math's is very simple. The Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja has combined all concepts together and given its explanation. Out of 16 sutras the Urdhva-Tiryagbhyam Vedic Sutra is very much useful multiplication operation. Present work is an effort to design and implement the multiplier using Urdhva- Tiryagbhyam Vedic Sutra.

B. Urdhva-Triyagbhyam Sutra and its Implementation

The Urdhva Tiryagbhyam sutra is based on vertical and crosswise multiplication algorithm. This sutra enables the parallel generation of intermediate products and eliminates unwanted multiplication steps. This type of multiplier takes a form of one of the low powers and high-speed multiplier.

Design: Urdhva Triyagbhyam means "Vertically and Crosswise", which is the method of multiplication followed. For the Vedic multiplication consider a 4×4 multiplier whose operands are $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$.For the multiplication of a single bit a simple AND gate is used. So, the generalized equations for the output bits of 4X4 Vedicmultiplier can be written as:

1) $S_0=A_0B_0$
2) $S_1=A_0B_1+A_1B_0$
3) $S_2=A_0B_2+A_1B_1+A_2B_0$+previous carry
4) $S_3=A_0B_3+A_1B_2+A_2B_1+A_3B_0$+previous carry
5) $S_4=A_1B_3+A_2B_2+A_3B_1$+previous carry
6) $S_5=A_2B_3+A_3B_2$+previous carry
7) $S_6=A_3B_3$

The S_7 bit is the carry of the previous addition process. Thus, 8bit output is been obtained.

The block diagram of this sutra in being referred in the Fig. 1-

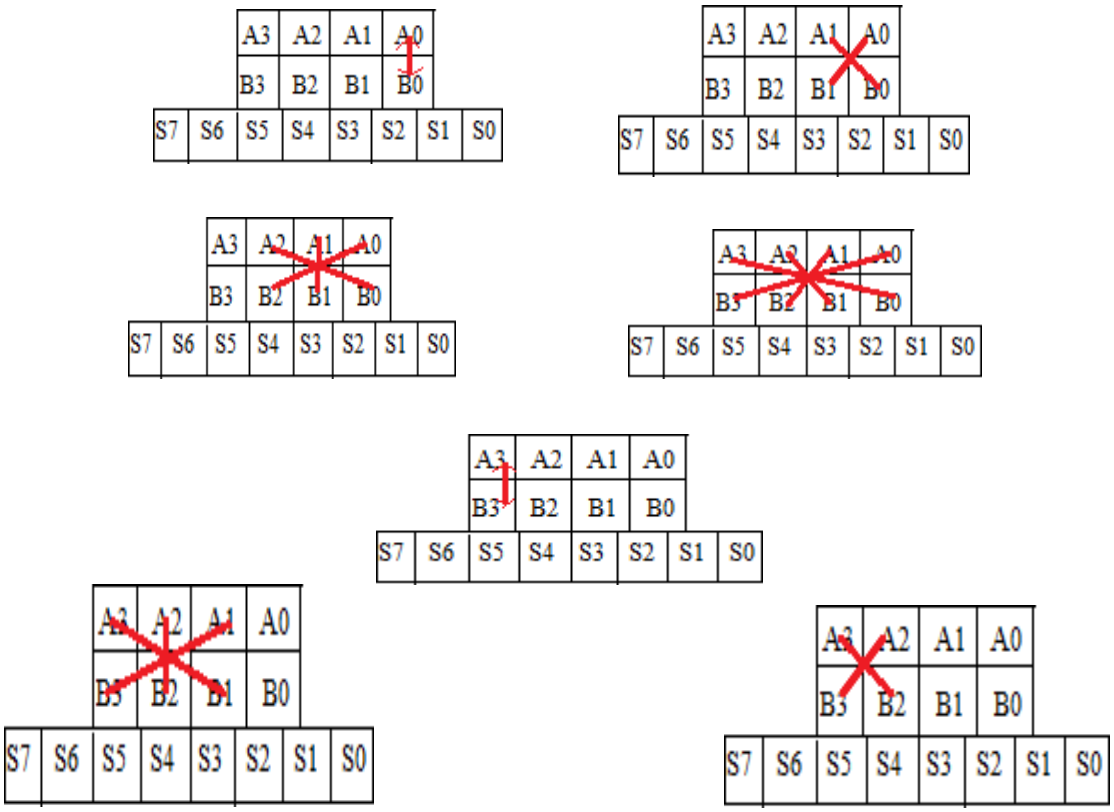


Fig. 1 Calculation of output bits from S0 to S7 respectively.

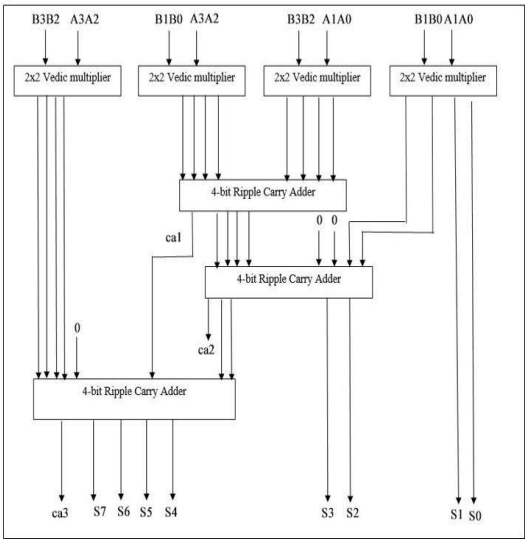


Fig.2Existing 4x4 Vedic Multiplier

Using four 2x2 bit Vedic multipliers and 3 adders we can build 4x4 bit Vedic multiplier as shown in Fig. 2 with proper instantiating of the 2x2 Vedic multipliers and adders. First 2x2 bit Vedic multiplier has inputs as A_1A_0 and B_1B_0. The last block is also 2x2 bit Vedic multiplier with inputs A_3A_2 and B_3B_2. The blocks in the middle are 2x2 bit multipliers with inputs A_3A_2 & B_1B_0 and A_1A_0 & B_3B_2. So, the result of multiplication will be of 8-bit as S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0. As compared to Array Multiplier, Vedic Multiplier is efficient in terms of delay and speed. The Vedic Multiplier can be used to reduce delay.

III. ARCHITECTURE OF APPROXIMATE 8-BIT MULTIPLIER

A. Design Process

The following steps are followed in the design of the multiplier

1) Design a basic 4-bit Adder which performs the function of 4-bit addition.
2) Design an efficient 4x4 bit Vedic multiplier using half adder, full adder and 4-bit adder.
3) Design 8x8 Vedic multiplier using 4x4 bit Vedic Multiplier and 8 Bit RippleCarry Adder.
4) Design 8-bit selection architecture using 2:1 Mux and design a 3:1 Mux toperform shifting operations on output bits.
5) Energy consumption and delay of the circuit is estimated.

B. Proposed 4 Bit Adder

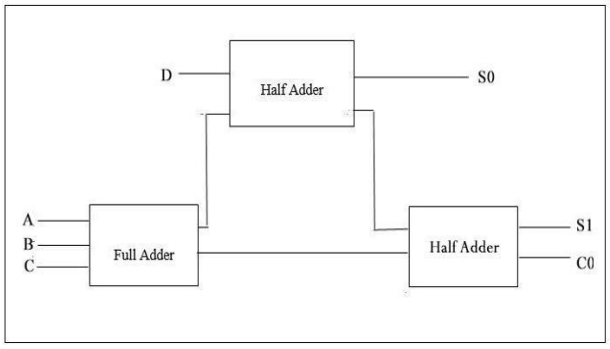


Fig. 3 A 4-bit adder is designed using half adders and full adder

Proposed 4-bit adder performs the function of 4-bit addition that gives two bits of sum and one carry as output. Its block diagram contains one full adder (FA) and two half adders (HA) as shown in the Fig.3. Here, A, B, C, D are four inputs. S_0 and S_1 are LSB and MSB of Sum outputs respectively and Sum is the sum of four inputs whereas C_0 is the carry bit. The delay of the 4x4 Vedic Multiplier can be further decreased by using this proposed 4 Bit Adder.

C. 4X4 Vedic Multiplier

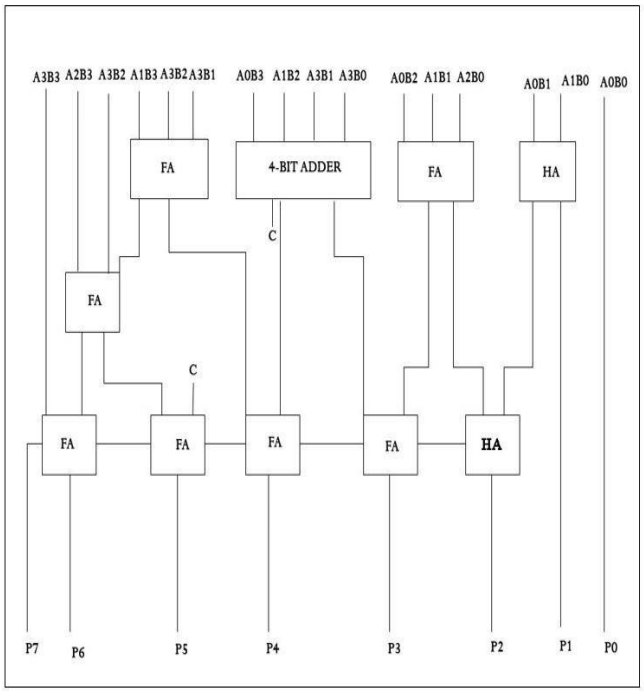


Fig. 4 4x4 Vedic Multiplier

To reduce the delay, a 4x4 Vedic multiplier is implemented using half adder, full adder and the proposed 4-bit adder as shown in the Fig. 4. Here, few full adders are replaced with the half adders so that the critical path delay is reduced to a greater extent. So, the designed multiplier is much more efficient than existing Vedic multiplier. The higher bit Vedic multiplier architectures like 8-bit, 16-bit, 32-bit etc. can be built using these 4-bit Vedic multipliers. The Fig.3.2 depicts two inputs consisting of 4-bit size that results by producing an output P resulting of 8-bit size.

D. 8X8 Vedic Multiplier using 4X4 Vedic Multiplier

1) 8-bit ripple carry adder

A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into next stage as shown in Fig. 5.

The A and B are 8 bits each.$A=A_0\ A_1\ A_2\ A_3\ A_4\ A_5\ A_6\ A_7$

$B=B_0\ B_1\ B_2\ B_3\ B_4\ B_5\ B_6\ B_7$

A and B are added and the corresponding sum and carry is obtained.Here, $S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8$ is the sum.

C_8 is the carry out.

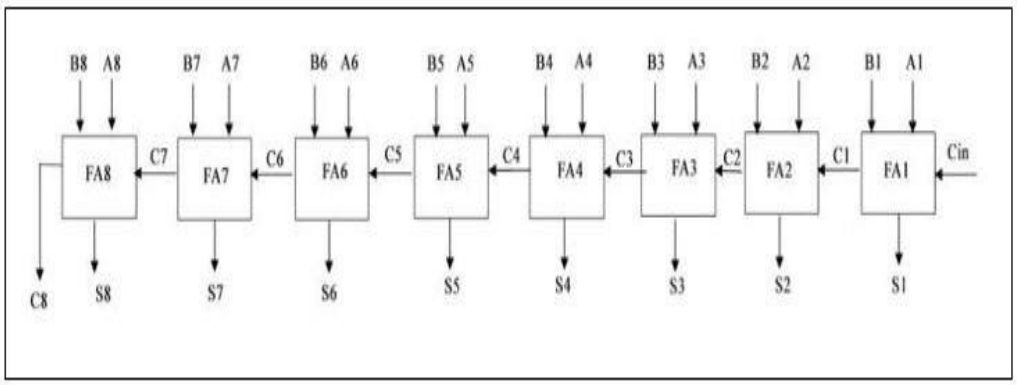


Fig. 5 8-bit Ripple Carry addder

2) 8X8 Vedic Multiplier

As shown in Fig. 6, the 8X8 Vedic Multiplier consists of 8-bit ripple carry adders and 4x4 Vedic Multipliers. So, 8bit inputs- a [0-7], b [0-7] are given and a 16-bit product s [15:0] is obtained.

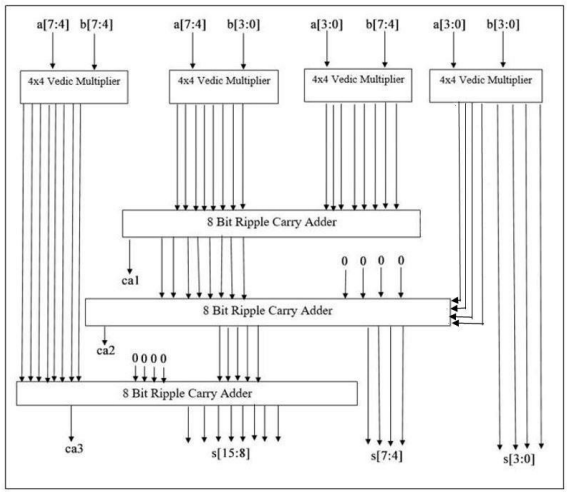


Fig. 6 8x8 Vedic Multiplier

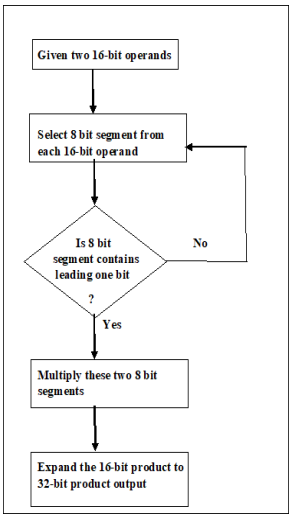


Fig. 7 Flowchart of Approximate Multiplier

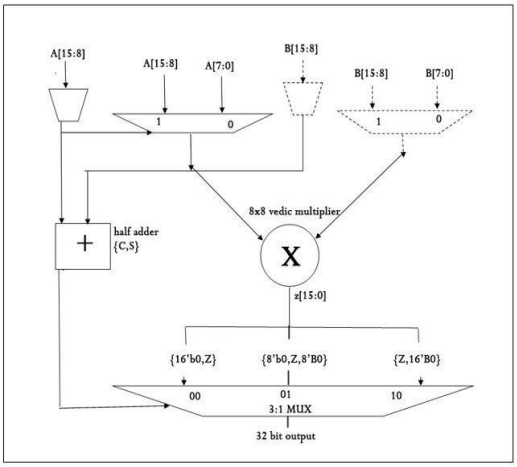


Fig. 8 8 Bit Approximate Vedic Multiplier

The structure of the proposed 8 Bit Selection Architecture of approximate multiplier is shown in Fig. 8. The architecture consists of two "8" bit selection units for each 16-bit operands, a multiplier unit, a 3 to 1 mux as output unit and a half adder which gives the selection bit for the output mux. Here the approximate multiplier takes only "8" consecutive bits for multiplication from each "16" bit operands. The 8-bit segment is selected only from one of two or three fixed bit positions of a positive number depending on where is its leading one bit. This technique gives a higher accuracy than simply truncating the LSBs. In this approach the 8-bit segments are selected from each operand from the leading one positions and it is then steered into an 8 × 8 multiplier (which is here a Vedic multiplier) and then the 2*8 output obtained from the multiplieris expanded to 2*16 output bits.

IV. DESIGN AND SIMULATION OF APPROXIMATE 8-BIT VEDIC MULTIPLIER

A. Simulation

The work deals with designing Approximate multiplier with 8-bit selection architecture and which also implements Vedic multiplication. So, the outputs are considered and simulated such that required operations of multiplier are verified. To obtain the delay report of project a simulating tool name XILINX ISE SUITE 14.7 is used, whereas to obtain the power report CADENCE simulating tool is used. Once all the required building blocks are designed and verified; these blocks are integrated to design the Approximate multiplier.

B. Simulation Waveforms

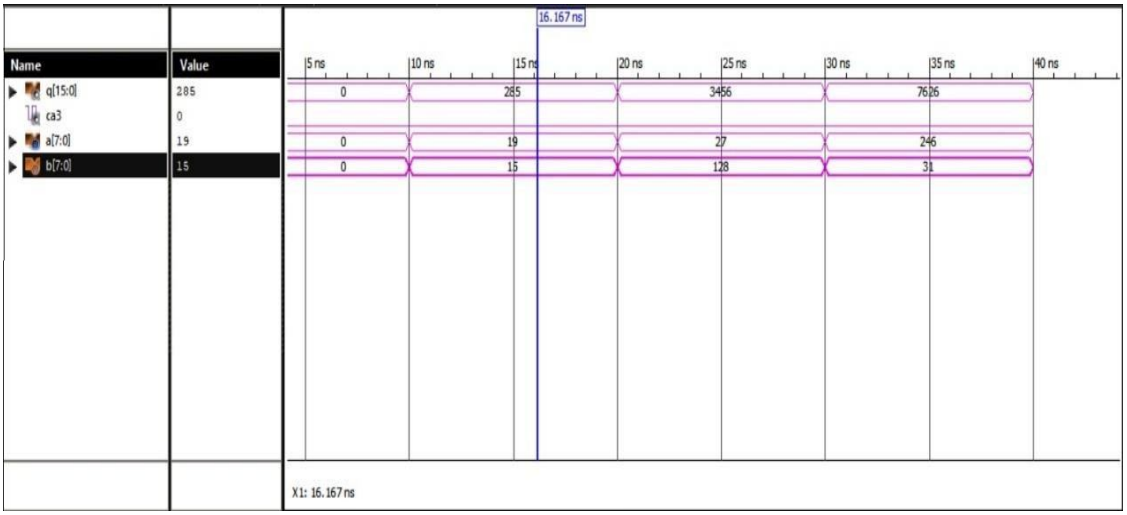


Fig. 9 Waveform of 8x8 Vedic Multiplier

```
ISim R.20131013 (signature 0x8ef4fb42)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
        0a= 0     b= 0     ca3=0     q=  0
       10a= 19    b= 15    ca3=0     q=  285
       20a= 27    b=128    ca3=0     q= 3456
       30a=246    b= 31    ca3=0     q= 7626
Stopped at time : 40 ns : in File "C:/Users/anish/OneDrive/Desktop/mp 119/Project 4-2/bit8 vedic/bit8 vedic tb.v" Line 60
ISim>
```

From the simulation result, we can see the output of 8x8 bit Vedic multiplier for given 8-bit inputs a=19, b=15 is 285. Hence, the obtained outputmatches expected output.

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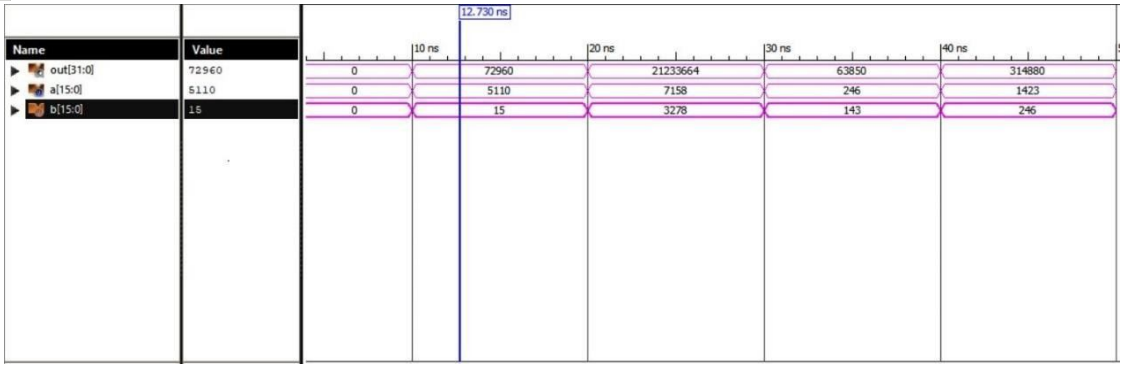


Fig. 10 Waveform of approximate 8-bit Vedic multiplier

```
ISim P.20131013 (signature 0x8ef4fb42)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
          0a=  0        b=  0          out=     0
         10a= 5110      b=  15         out=   72960
         20a= 7158      b= 3278        out= 21233664
         30a=  246      b=  143        out=   63850
         40a= 1423      b=  246        out=  314880
Stopped at time : 50 ns : in File "C:/Users/anish/Desktop/raspro/approx_multi/approx_multi_tb.v" Line 62
ISim>
```

From the simulation result, we can see the output of the approximate 8-bit Vedic multiplier for the given input a=5110, b=15 is 72960 whereas the expected output is 76650. Hence, approximate multiplier produces approximate output instead of exact output and such a slight error in output is negligible for computation-intensive applications which are robust to small errors in computation.

V. RESULTS AND DISCUSSIONS

A. *Delay Report of 4x4 Vedic Multiplier*

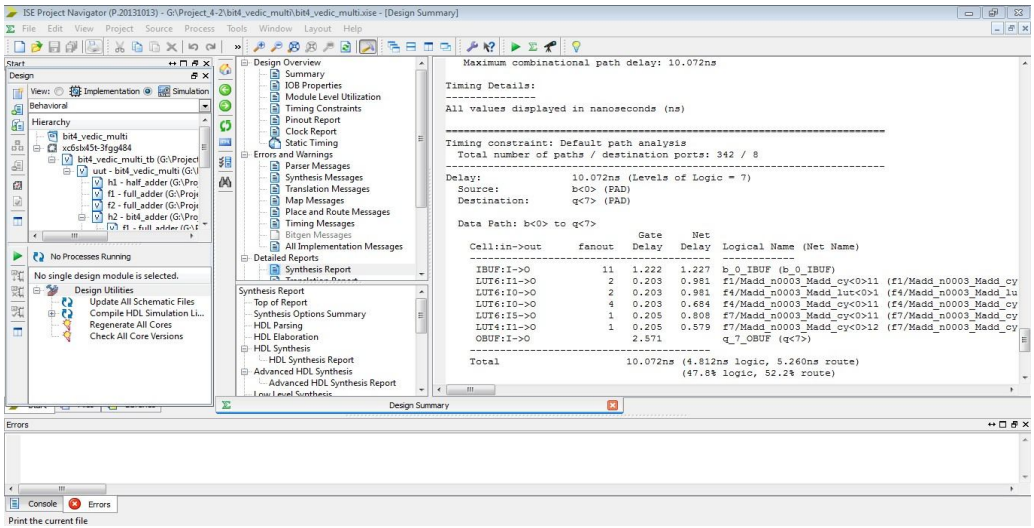


Fig. 11 Delay Report of 4x4 Vedic Multiplier

Fig. 11 shows the delay report of 4x4 Vedic Multiplier. Delay obtained for 4x4 Vedic Multiplier is 10.072 ns. Hence it can be concluded that the performance of proposed Vedic multiplier seems to be highly efficient in terms of speed when compared to conventional multipliers and it is evident that the proposed design is more efficient than existing Vedic multiplier.

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B. Delay Report of 8-bit Ripple Carry Adder

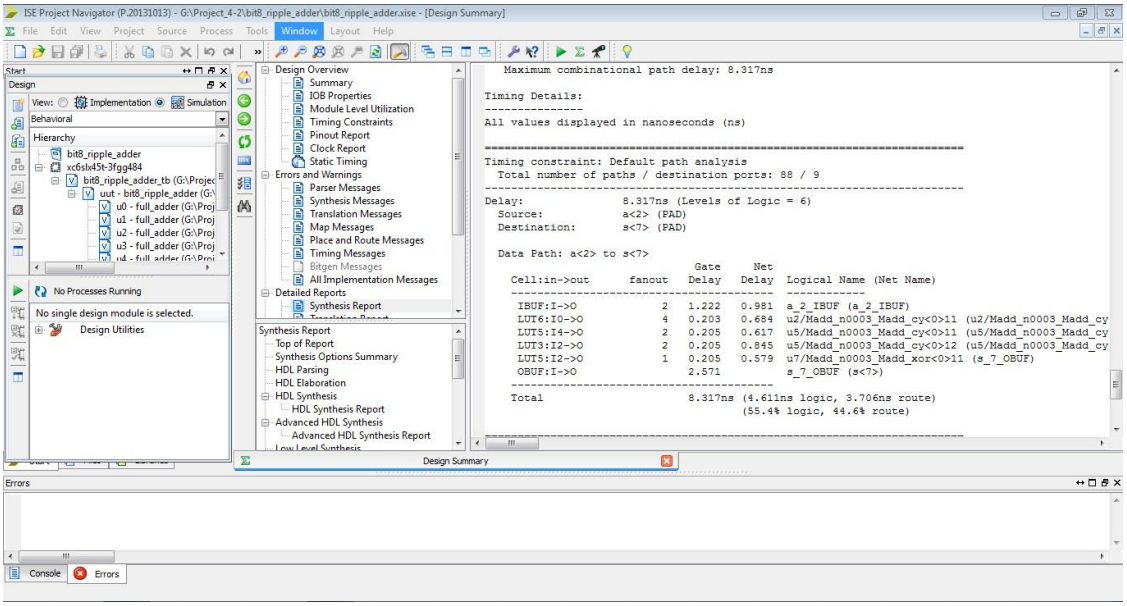


Fig. 12 Delay Report of 8-bit Ripple Carry Adder

The delay report of the 8-bit Ripple Carry Adder is shown in Fig. 12 and the delay obtained is 8.317ns. In ripple carry adder, each stage of the adder must wait until the previous stage has calculated and propagates its carry signal. Therefore, the total delay of the ripple carry adder is proportional to the number of bits. Faster adders are often required for bit widths of 16 or greater.

C. Delay Report of 8X8 Vedic Multiplier

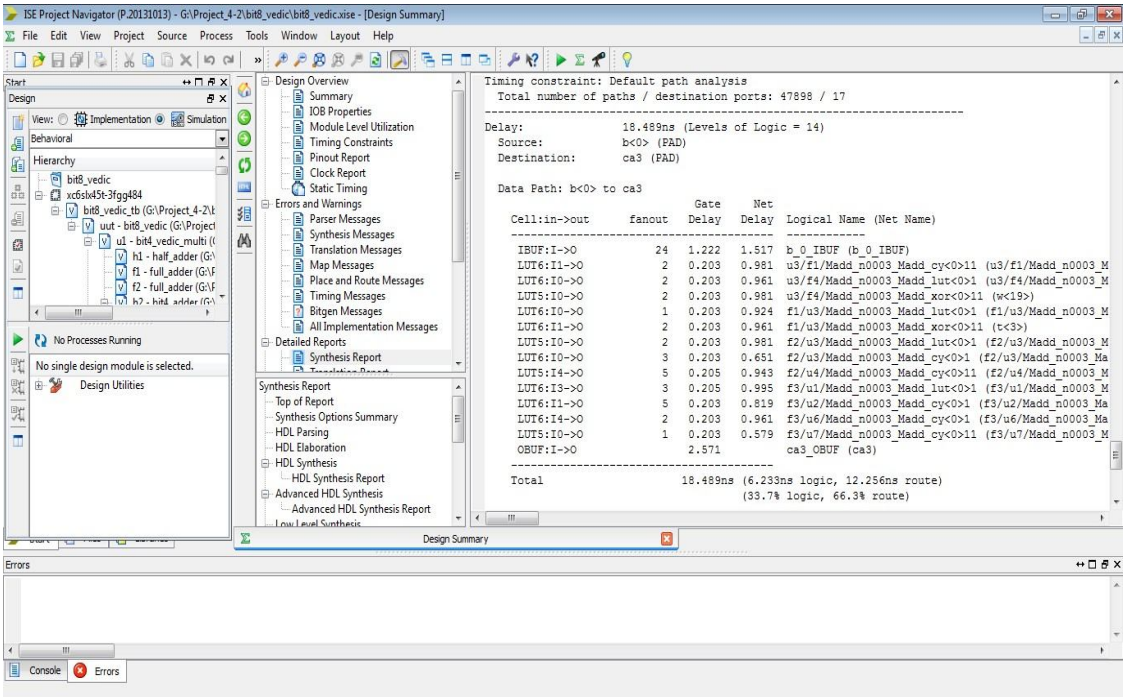


Fig. 13 Delay Report of 8X8 Vedic Multiplier

Fig. 13 shows the delay report of 8x8 Vedic Multiplier and Delay obtained is 18.489ns. Thus, proposed Vedic multiplier can be used to develop a high-speed complex number multiplier with reduced delay.

D. Delay Report of 8-bit Vedic Multiplier

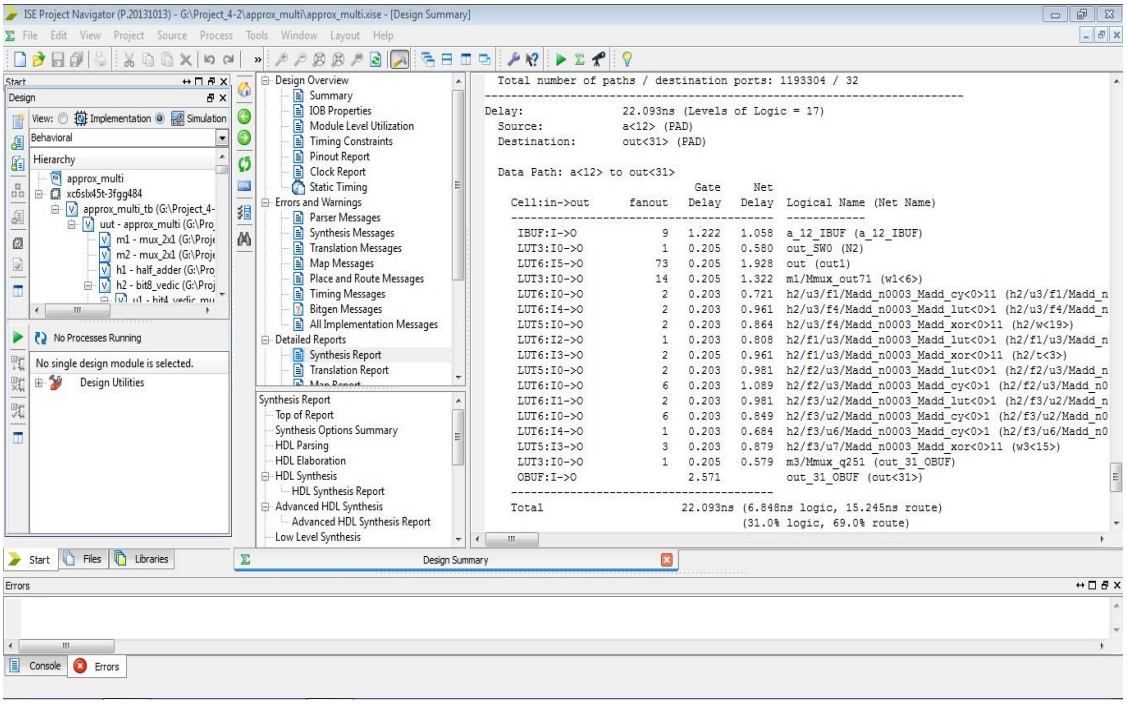
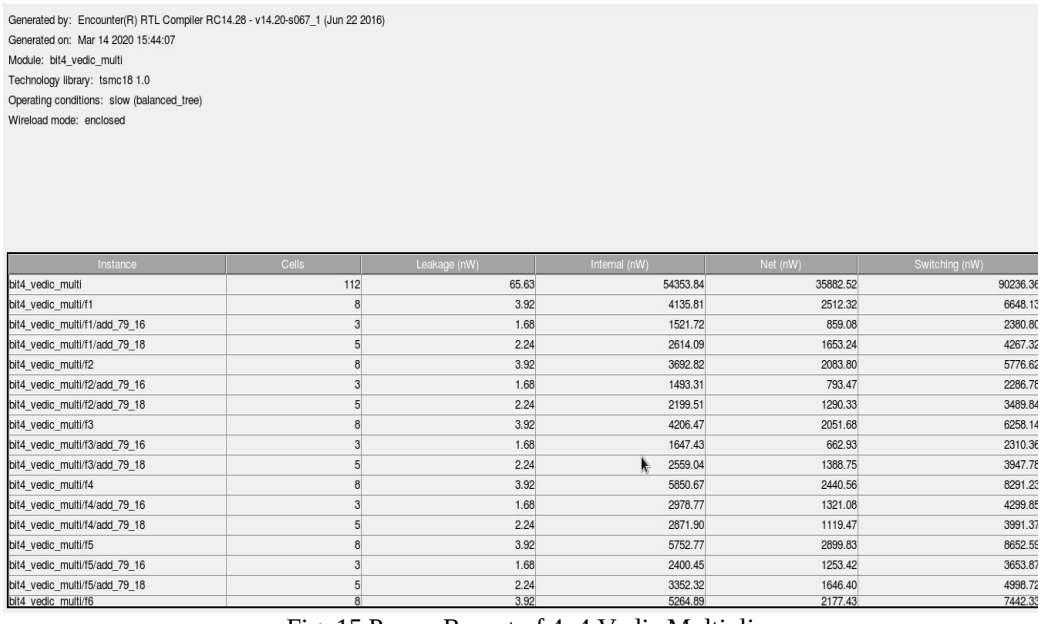


Fig. 14 Delay Report of 8-bit Vedic Multiplier

Delay obtained for the Approximate 8-bit Vedic Multiplier is 22.093ns. Thus, the bit reduction using 8 bit selection reduces the computation complexity which leads to a reduced delay and also the reduced delay Vedic architecture further reduces the delay.

E. Power Report of 4x4 Vedic Multiplier



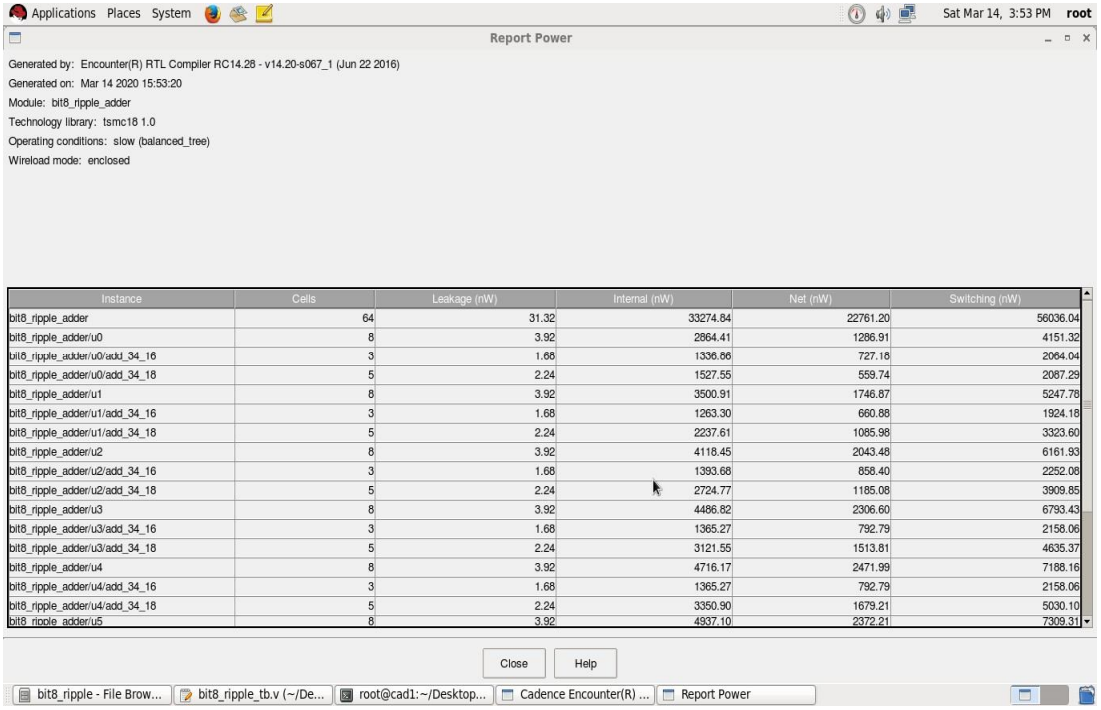
Generated by: Encounter(R) RTL Compiler RC14.28 - v14.20-s067_1 (Jun 22 2016)
Generated on: Mar 14 2020 15:44:07
Module: bit4_vedic_multi
Technology library: tsmc18 1.0
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
bit4_vedic_multi	112	65.63	54353.84	35882.52	90236.36
bit4_vedic_multi/f1	8	3.92	4135.81	2512.32	6648.13
bit4_vedic_multi/f1/add_79_16	3	1.68	1521.72	859.08	2380.80
bit4_vedic_multi/f1/add_79_18	5	2.24	2614.09	1653.24	4267.32
bit4_vedic_multi/f2	8	3.92	3692.82	2083.80	5776.62
bit4_vedic_multi/f2/add_79_16	3	1.68	1493.31	793.47	2286.78
bit4_vedic_multi/f2/add_79_18	5	2.24	2199.51	1290.33	3489.84
bit4_vedic_multi/f3	8	3.92	4206.47	2051.68	6258.14
bit4_vedic_multi/f3/add_79_16	3	1.68	1647.43	662.93	2310.36
bit4_vedic_multi/f3/add_79_18	5	2.24	2559.04	1388.75	3947.78
bit4_vedic_multi/f4	8	3.92	5850.67	2440.56	8291.23
bit4_vedic_multi/f4/add_79_16	3	1.68	2978.77	1321.08	4299.85
bit4_vedic_multi/f4/add_79_18	5	2.24	2871.90	1119.47	3991.37
bit4_vedic_multi/f5	8	3.92	5752.77	2899.83	8652.59
bit4_vedic_multi/f5/add_79_16	3	1.68	2400.45	1253.42	3653.87
bit4_vedic_multi/f5/add_79_18	5	2.24	3352.32	1646.40	4998.72
bit4_vedic_multi/f6	8	3.92	5264.89	2177.43	7442.33

Fig. 15 Power Report of 4x4 Vedic Multiplier

Fig. 15 shows the power report of a 4x4 Multiplier. The power consumed for 4x4 Multiplier is 0.180538mW. Here multiplication is based on Urdhva Triyakbhyam algorithm, which can reduce the power, delay, and hardware requirements for multiplication of numbers.

F. Power Report of 8-bit Ripple Adder

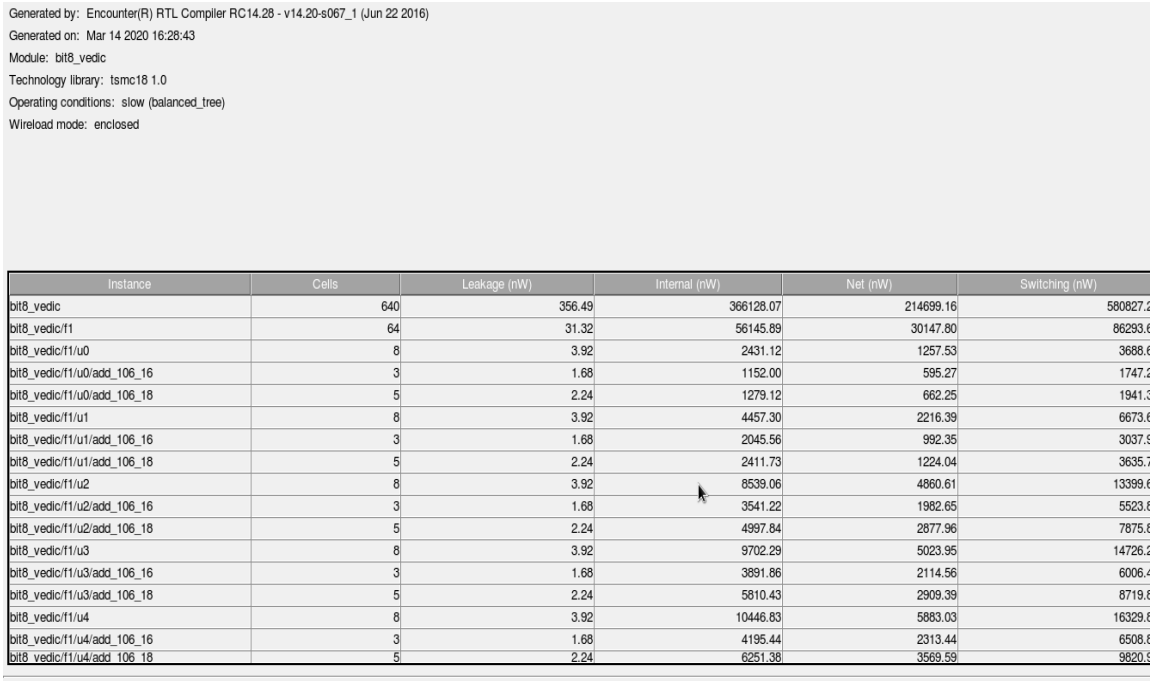


Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
bit8_ripple_adder	64	31.32	33274.84	22761.20	56036.04
bit8_ripple_adder/u0	8	3.92	2864.41	1286.91	4151.32
bit8_ripple_adder/u0/add_34_16	3	1.68	1336.86	727.18	2064.04
bit8_ripple_adder/u0/add_34_18	5	2.24	1527.55	559.74	2087.29
bit8_ripple_adder/u1	8	3.92	3500.91	1746.87	5247.78
bit8_ripple_adder/u1/add_34_16	3	1.68	1263.30	660.88	1924.18
bit8_ripple_adder/u1/add_34_18	5	2.24	2237.61	1085.98	3323.60
bit8_ripple_adder/u2	8	3.92	4118.45	2043.48	6161.93
bit8_ripple_adder/u2/add_34_16	3	1.68	1393.68	858.40	2252.08
bit8_ripple_adder/u2/add_34_18	5	2.24	2724.77	1185.08	3909.85
bit8_ripple_adder/u3	8	3.92	4486.82	2306.60	6793.43
bit8_ripple_adder/u3/add_34_16	3	1.68	1365.27	792.79	2158.06
bit8_ripple_adder/u3/add_34_18	5	2.24	3121.55	1513.81	4635.37
bit8_ripple_adder/u4	8	3.92	4716.17	2471.99	7188.16
bit8_ripple_adder/u4/add_34_16	3	1.68	1365.27	792.79	2158.06
bit8_ripple_adder/u4/add_34_18	5	2.24	3350.90	1679.21	5030.10
bit8_ripple_adder/u5	8	3.92	4937.10	2372.21	7309.31

Fig. 16 Power Report of 8-bit Ripple Adder

Fig. 16 shows the power report of the 8-bit ripple adder. The power consumed for 8 Bit Ripple Carry Adder is 0.1121mW. The advantage of the ripple carry adder is low power consumption when compared to another adder

G. Power Report of 8x8 Vedic Multiplier

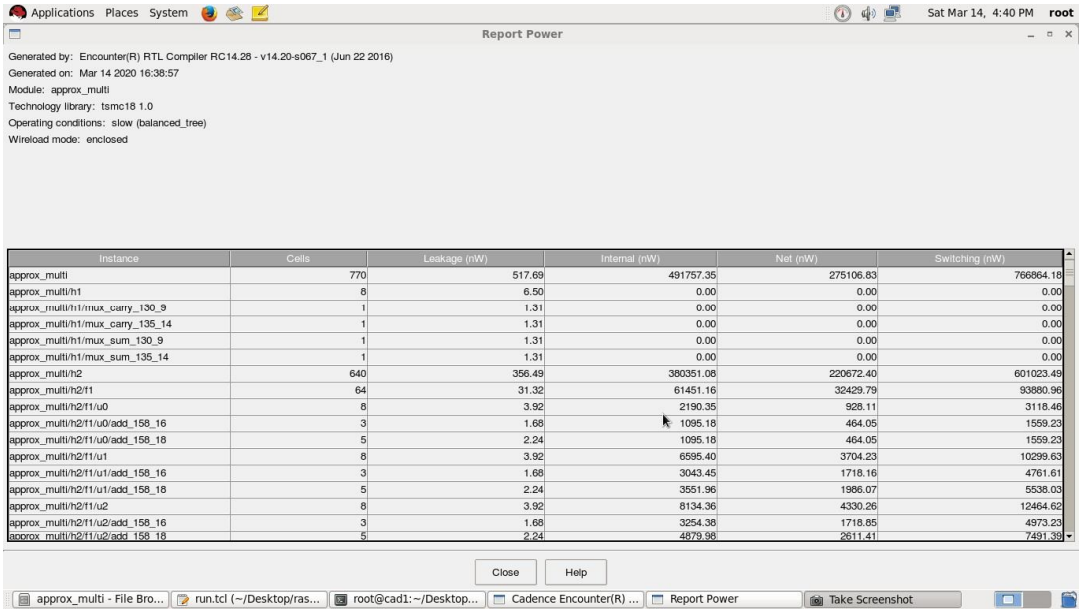


Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
bit8_vedic	640	356.49	366128.07	214699.16	580827.2
bit8_vedic/f1	64	31.32	56145.89	30147.80	86293.6
bit8_vedic/f1/u0	8	3.92	2431.12	1257.53	3688.6
bit8_vedic/f1/u0/add_106_16	3	1.68	1152.00	595.27	1747.2
bit8_vedic/f1/u0/add_106_18	5	2.24	1279.12	662.25	1941.3
bit8_vedic/f1/u1	8	3.92	4457.30	2216.39	6673.6
bit8_vedic/f1/u1/add_106_16	3	1.68	2045.56	992.35	3037.9
bit8_vedic/f1/u1/add_106_18	5	2.24	2411.73	1224.04	3635.7
bit8_vedic/f1/u2	8	3.92	8539.06	4860.61	13399.6
bit8_vedic/f1/u2/add_106_16	3	1.68	3541.22	1982.65	5523.8
bit8_vedic/f1/u2/add_106_18	5	2.24	4997.84	2877.96	7875.8
bit8_vedic/f1/u3	8	3.92	9702.29	5023.95	14726.2
bit8_vedic/f1/u3/add_106_16	3	1.68	3891.86	2114.56	6006.4
bit8_vedic/f1/u3/add_106_18	5	2.24	5810.43	2909.39	8719.8
bit8_vedic/f1/u4	8	3.92	10446.83	5883.03	16329.8
bit8_vedic/f1/u4/add_106_16	3	1.68	4195.44	2313.44	6508.8
bit8_vedic/f1/u4/add_106_18	5	2.24	6251.38	3569.59	9820.9

Fig. 17 Power Report of 8x8 Vedic Multiplier

Fig. 17 shows the report of the 8x8 Vedic Multiplier. The power consumed for 8X8 VedicMultiplier is 1.16201mW.

H. Power Report of Approximate 8 Bit Vedic Multiplier



Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
approx_multi	770	517.69	491757.35	275106.83	766864.18
approx_multi/h1	8	6.50	0.00	0.00	0.00
approx_multi/h1/mux_carry_130_9	1	1.31	0.00	0.00	0.00
approx_multi/h1/mux_carry_135_14	1	1.31	0.00	0.00	0.00
approx_multi/h1/mux_sum_130_9	1	1.31	0.00	0.00	0.00
approx_multi/h1/mux_sum_135_14	1	1.31	0.00	0.00	0.00
approx_multi/h2	640	356.49	380351.08	220672.40	601023.49
approx_multi/h2/f1	64	31.32	61451.16	32429.79	93880.96
approx_multi/h2/f1/u0	8	3.92	2190.35	928.11	3118.46
approx_multi/h2/f1/u0/add_158_16	3	1.68	1095.18	464.05	1559.23
approx_multi/h2/f1/u0/add_158_18	5	2.24	1095.18	464.05	1559.23
approx_multi/h2/f1/u1	8	3.92	6595.40	3704.23	10299.63
approx_multi/h2/f1/u1/add_158_16	3	1.68	3043.45	1718.16	4761.61
approx_multi/h2/f1/u1/add_158_18	5	2.24	3551.96	1986.07	5538.03
approx_multi/h2/f1/u2	8	3.92	8134.36	4330.26	12464.62
approx_multi/h2/f1/u2/add_158_16	3	1.68	3254.38	1718.85	4973.23
approx_multi/h2/f1/u2/add_158_18	5	2.24	4879.98	2611.41	7491.39

Fig.18 Power Report of Approximate 8 Bit Vedic Multiplier

The powers consumed for the Approximate 8-bit Vedic Multiplier is 1.5342mW. As the significant reduction in the proposed architecture offers a great advantage in the reduction of total power consumption

Table 1- Synthesis Results

Module	Maximum Combination Delay(ns)	Total Power(mW)
Full adder	5.422	0.01368594
4-bit adder	5.473	0.03325859
4X4 Vedic Multiplier	10.072	0.18053835
8-bit ripple carry adder	8.317	0.1121034
8x8 Vedic Multiplier	18.489	1.16201092
Mux	6.211	0.26936871
Mux+8X8 Vedic Multiplier	22.093	1.53424605

The Table 1 shows the outcome of various stages of the of the proposed multiplier So finally, after the overall synthesis and simulation of the approximate 8-bit Vedic Multiplier. Maximum Combinational delay is 22.093 ns and the total power consumedis 1.5342mW.

Table 2- Comparison of the implemented design with reference design

Design	Bits	Area (No of slices)	Delay (ns)	Power (W)
Approximate 8-bit Vedic multiplier	16	153	22.093	0.001534
Iterative logarithmic multiplier	16	381	41.555	0.15687

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Here we compare our design for the number of slices, delay, and power consumption. The data for comparison is taken from the reference paper. Thus, the proposed approximate 8-bit Vedic multiplier is more energy efficient than the other conventional multipliers. Hence the potential applications of this approximate multiplier fall mainly in areas where there is no strict requirement on accuracy or wheresuper-low power consumption and high-speed performance are more important than theaccuracy.

VI. CONCLUSIONS

Area, power consumption and increased delay are the constituent factors in VLSI design that degrades the performance of any circuit. This proposed architecture of an energy efficient multiplier in which the area, delay and power consumption are reduced to a great extent on comparing with the present works. A technique for the multiplication of 8-bit operands with the help of Vedic multiplier is described. The proposed architecture is based on "Urdhva Triyakbhyam" sutra of Vedic mathematics which is a general multiplication technique for multiplication. This algorithm makes the parallel generation of partial products and removes unwanted multiplication steps and hence results in faster multiplication. Also, with this algorithm the increase in delay and power consumption is less with the increase in number of bits. This proposed technique works in two steps. In the first step the equation for each bit of the resultant is computed. In the second step that equation is executed with the required multipliers and Ripple Carry Adders. The reduction of number of bits which takes part in multiplication reduces the complexity of the multiplication process and thus improves the efficiency. The number of, half adders and full adders used in the proposed multiplier architecture is much less than the conventional multiplier architectures. The significant reduction in the proposed architecture offers a great advantage in the reduction of area and therefore the total power consumption. Thus, the proposed 8-bit multiplier is more energy efficient than the other conventional multipliers. Also, the bit reduction using 8 bit selection reduces the computational complexity which leads to a reduced delay and also the reduced delay Vedic architecture further reduces the delay. The potential applications of this approximate Multiplier fall mainly in areas where there is no strict requirement on accuracy or where super-low power consumption and high-speed performance are more important than the accuracy. The 8-bit approximate Vedic multiplier can be used for various digital signal processing applications where complex computations are to be performed.

VII. FUTURE SCOPE

Future scope of the work includes improving the performance of the approximate Vedic multiplier by using Enhanced Static Segment Method for segment-based multiplication, to provide good accuracy at notably low energy consumption considerable reduction in area overhead and use of carry look-ahead adder in design of Vedic multiplier which in turn reduces the propagation delay by introducing more complex hardware.

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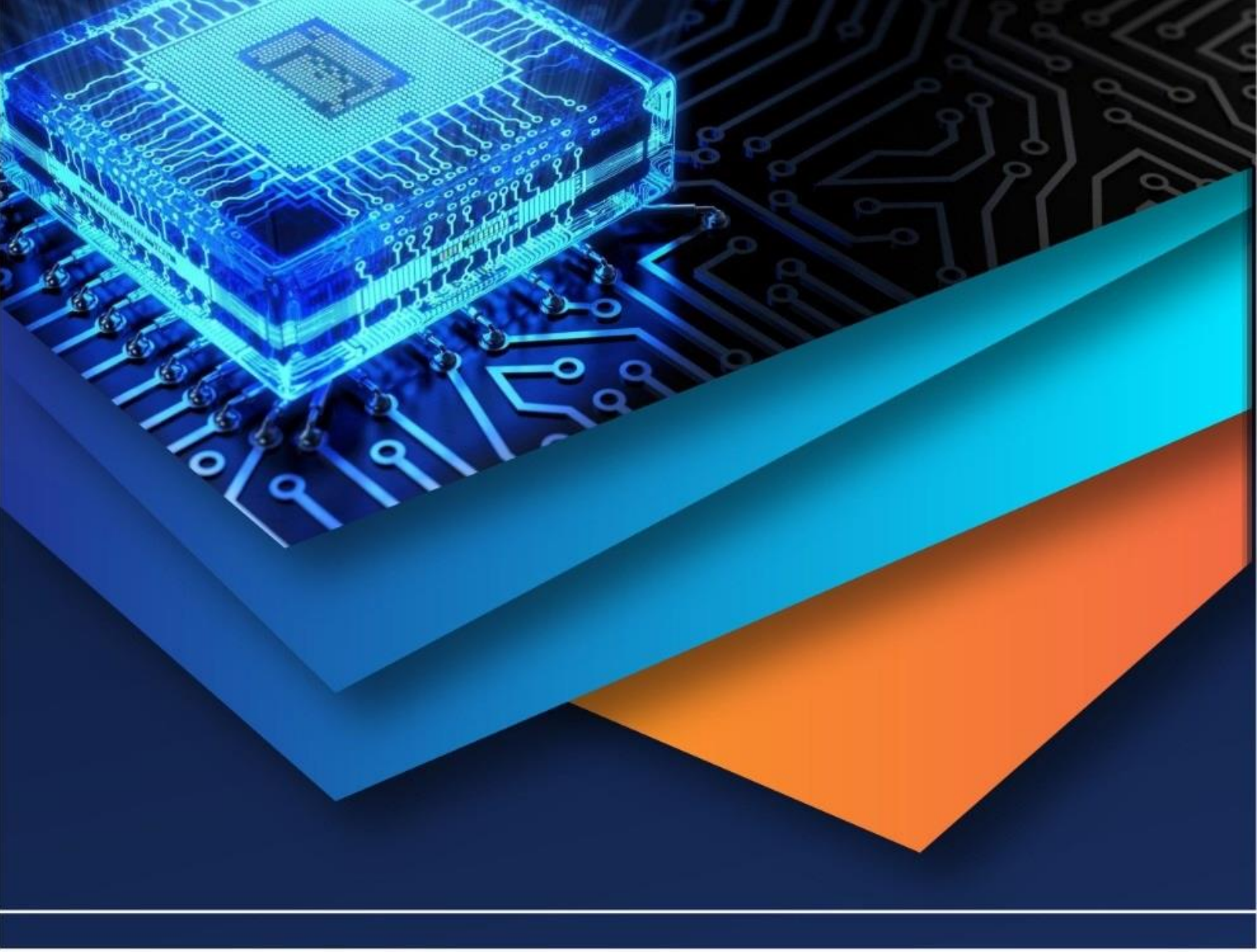


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