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Energy Efficient Compact Approximate Multplier for Error-Resilient Applications

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Abstract: ***This study focuses on enhancing system performance through approximate computing by proposing efficient 8-transistor and 20-transistor 4:2 compressors for approximate multipliers. These designs leverage CMOS technology with constant and conditional approximation techniques to minimize errors while eliminating the need for an error recovery module. The 20-transistor compressor achieves higher accuracy at a slight area cost, while the proposed multiplier demonstrates a 50% reduction in area and a 93% improvement in power-delay-product compared to exact multipliers.***
Keywords: Approximate computing, Compressor, Multiplier, Image Multiplication, Partial Products.

I. INTRODUCTION

The study we proposed in this paper builds upon the work presented in [8], expanding and improving upon its findings. This work introduces 8-transistor and 20-transistor approximate 4:2 compressors based on majority logic (ML) to improve the efficiency of arithmetic circuits. These compressors are designed for use in approximate multipliers, reducing circuit complexity and power consumption while maintaining acceptable accuracy. Compared to the conventional 12-transistor design, the proposed 8-transistor compressor minimizes hardware requirements, while the 20-transistor version improves accuracy. The new designs significantly reduce the number of partial products and exact compressors in multipliers, eliminating 15 AND gates from the partial product reduction tree (PPRT). Only one exact compressor is used, leading to a 49% area reduction and 93% lower energy consumption compared to an exact multiplier. The study also evaluates the performance of these compressors in image multiplication applications, demonstrating their advantages in error-tolerant computing. A comprehensive analysis of existing designs highlights trade-offs in power, area, and accuracy, making the proposed compressors a promising choice for high-performance, low-power circuits.

II. PROPOSED APPROXIMATE COMPRESSORS

This study presents 8-transistor and 20-transistor approximate 4:2 compressors based on majority logic (ML) to improve arithmetic circuit efficiency. ML, a fault-tolerant digital logic paradigm, enables reduced gate count while maintaining accuracy. The proposed compressors optimize partial product reduction in multipliers, reducing circuit complexity and power consumption. The 8-transistor design minimizes hardware, while the 20-transistor version enhances accuracy. The compressors eliminate 15 AND gates from the partial product reduction tree (PPRT), using only one exact compressor. This results in a 49% reduction in area and 93% lower energy consumption compared to exact multipliers. The study evaluates performance in image multiplication, demonstrating the proposed compressors' suitability for error-tolerant applications. A comparative analysis highlights trade-offs in accuracy, power, and area, positioning these designs as efficient solutions for high-performance, low-power circuits.

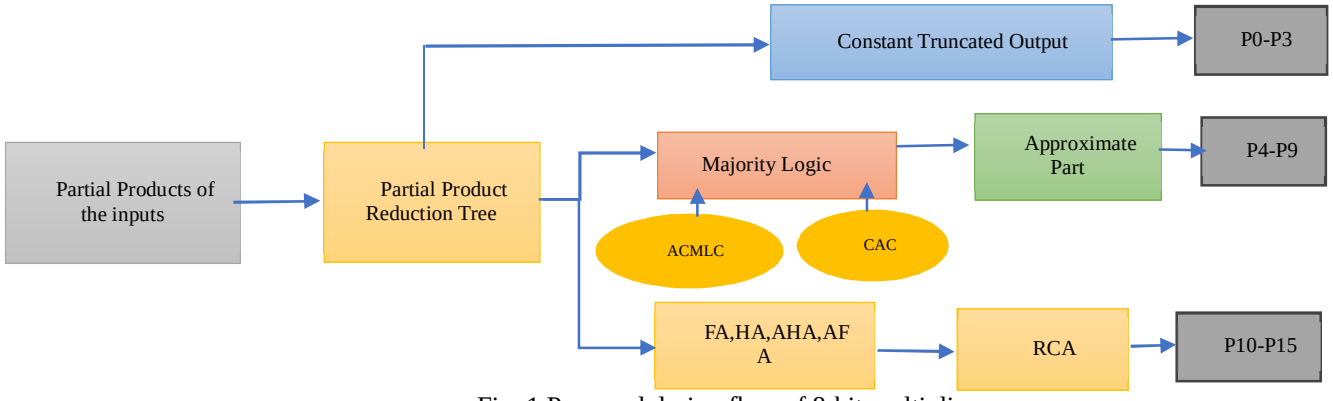

Fig. 1 Proposed design flow of 8-bit multiplier

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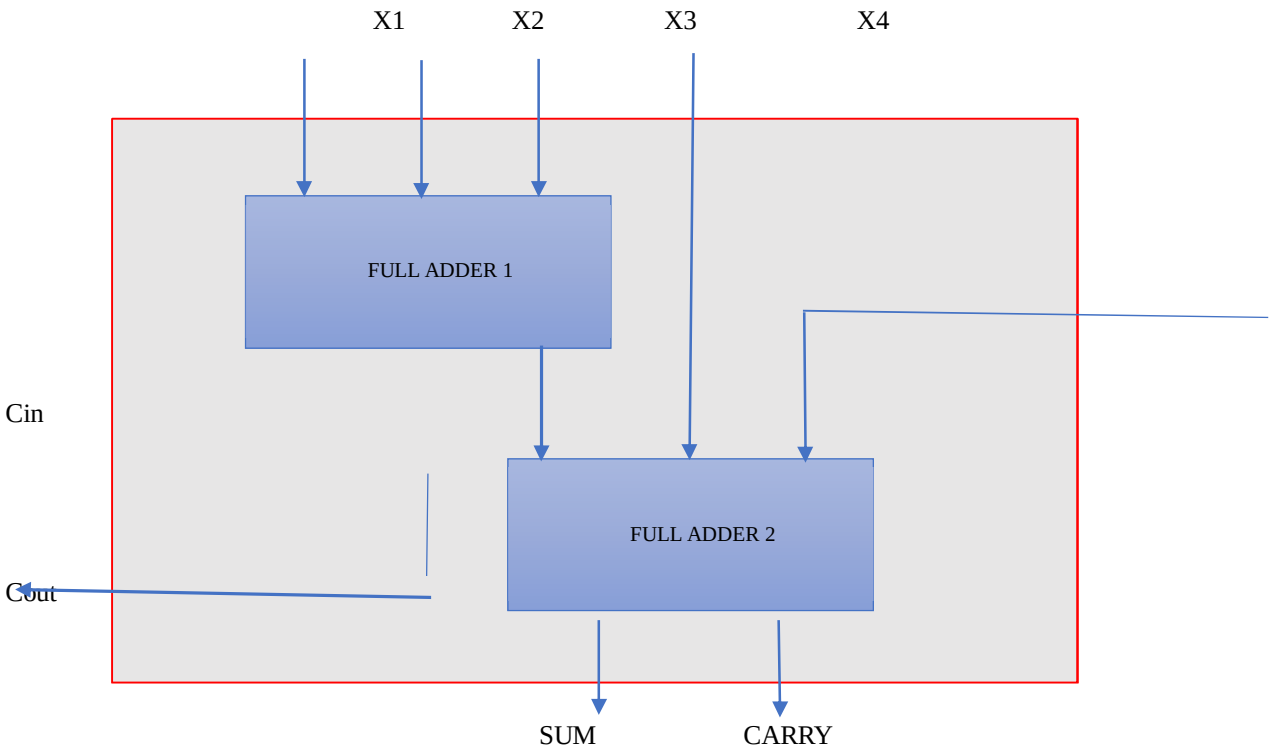


Fig. 2 Proposed Exact Compressor

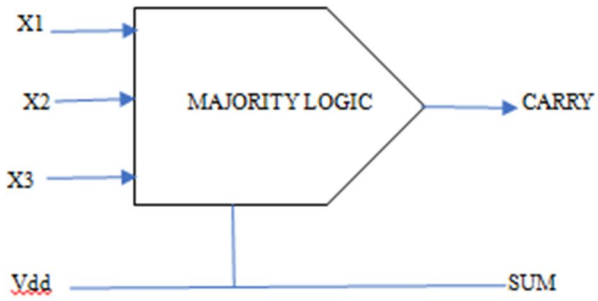


Fig. 3 Proposed ACMLC

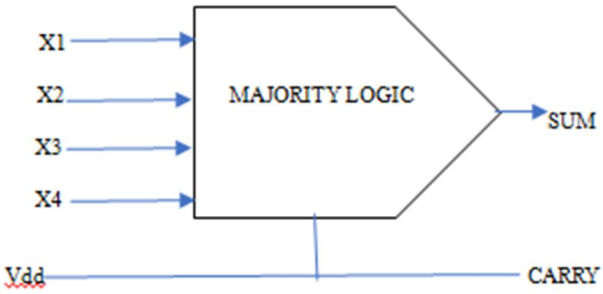


Fig. 4 Proposed CAC

X1	X2	X3	SUM	CARRY
0	0	0	0	1
0	0	1	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Table 1 Truth table of ACMLC

X1	X2	X3	X4	SUM	CARRY
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	1

Table 2 Truth table of CAC

A. 4:2 Approximate Condition based ML-Compressor and Compensator Approximate Compressor

This study introduces two novel approximate compressor architectures, the Approximate Condition-Based Majority Logic Compressor (ACMLC) and the Compensator Approximate Compressor (CAC), to enhance arithmetic circuit efficiency. These designs build upon majority logic (ML) compressors, which utilize simplified logic functions to improve speed, reduce power consumption, and optimize hardware complexity.

The ACMLC improves existing ML-based compressors by incorporating a two-stage approximation approach. Unlike conventional ML compressors that ignore one input, ACMLC refines the carry logic to reduce negative errors while maintaining circuit simplicity. It modifies the carry output conditions to ensure a more balanced error distribution, resulting in only three negative errors, compared to four in prior designs. The carry and sum outputs for ACMLC are given as:

$$\text{Carry}_{\text{ACMLC}} = (X1 \cdot X3) + X2$$
$$\text{Sum}_{\text{ACMLC}} = V_{DD}$$

To further improve accuracy, the CAC architecture is introduced as a compensator for ACMLC-based circuits. CAC refines the carry logic and sum functions to minimize the overall error distance while maintaining high performance. With only seven errors (all with an error distance of 1) and just one negative error, CAC significantly outperforms previous ML-based compressors. The carry and sum outputs for CAC are given as:

$$\text{Carry}_{\text{CAC}} = \text{VDD}$$
$$\text{Sum}_{\text{CAC}} = (X1 \cdot X2).(X3+X4)+(X3 \cdot X4)$$

The proposed multiplier architecture integrates ACMLC and CAC compressors to optimize the partial product reduction tree (PPRT), eliminating 15 AND gates and requiring only one exact compressor. This results in a 49% area reduction and 93% lower energy consumption compared to exact multipliers. Additionally, the elimination of an error recovery module (ERM) further simplifies the design.

A comparative analysis with state-of-the-art compressors highlights the proposed architectures' unique trade-offs in accuracy, power consumption, and area efficiency. The proposed compressors demonstrate higher performance in image multiplication applications, showcasing their suitability for error-tolerant computing. These innovations pave the way for compact, high-speed, and energy-efficient arithmetic circuits in emerging computing applications.

B. Approximate 8-Bit Multiplier

This study presents a high-efficiency approximate multiplier leveraging two novel approximate compressor architectures: the Approximate Condition-Based Majority Logic Compressor (ACMLC) and the Compensator Approximate Compressor (CAC). These designs enhance majority logic (ML) compressors, reducing hardware complexity and power consumption while maintaining high accuracy.

The proposed approximate multiplier consists of three components: truncation, approximation, and exact computation, optimizing the partial product reduction tree (PPRT). Truncation is applied to at least four least significant bit (LSB) columns, reducing gate count while ensuring computational accuracy. Instead of traditional truncation, a constant-value assignment method (as per [13]) fixes the four rightmost LSB bits at p0p1p2p3 = 0110, eliminating ten AND gates from the first stage.

The approximate component integrates five ACMLC-based half adders (HAs) and an exact full adder (FA). The 3-input ACMLC-based compressor effectively eliminates one partial product (PP) per stage, further removing five AND gates. Additionally, eight unused AND gates from the first stage are repurposed to construct a compressor-based chain in the second stage, further reducing the overall circuit area.

In the final stage, the proposed CAC compressor is deployed in the last column to transfer Carry = 1 to the exact computation unit, simplifying the exact compressor circuit. A single exact compressor with constant input (Cin = 1) is used in the entire multiplier, enhancing accuracy while maintaining low power consumption.

By integrating ACMLC and CAC, the proposed multiplier achieves 49% area savings and 93% lower energy consumption compared to an exact multiplier. The combination of approximate and exact computation enhances accuracy while eliminating the need for an error recovery module (ERM).

A comparative analysis with state-of-the-art compressors highlights superior power efficiency, area reduction, and computational accuracy. The proposed design is well-suited for error-tolerant applications, such as image processing, where approximate computing techniques offer significant performance advantages.

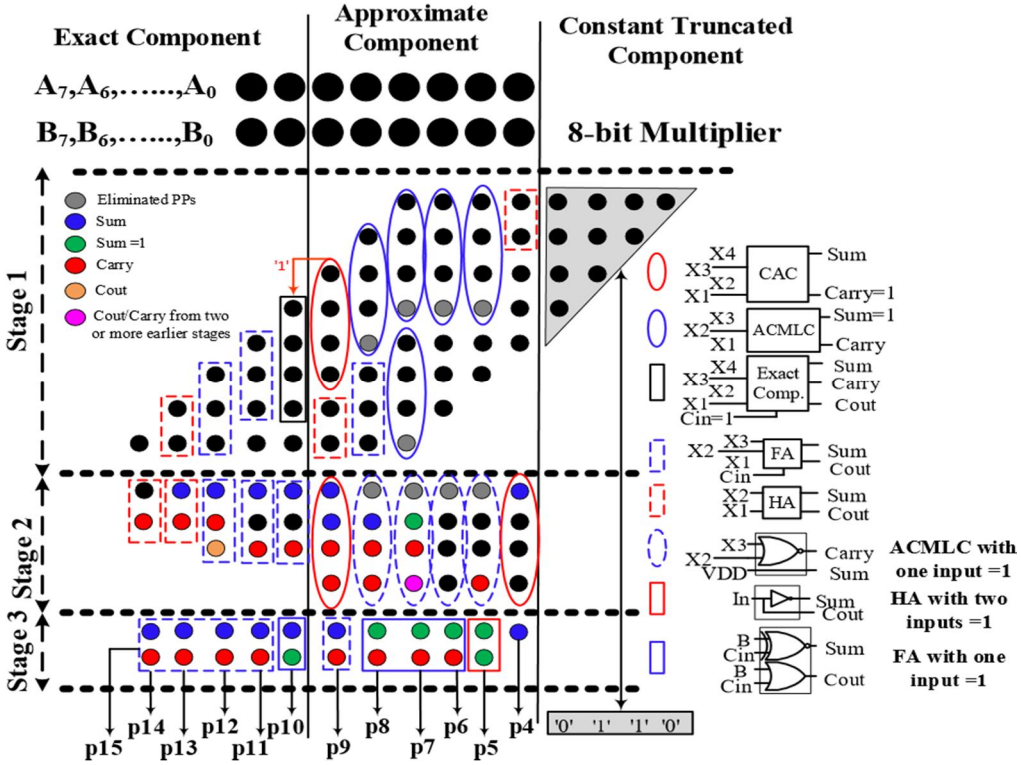


Fig. 5 Approximate 8-bit multiplier[8]

This study introduces a high-efficiency approximate multiplier utilizing two novel compressor architectures: the Approximate Condition-Based Majority Logic Compressor (ACMLC) and the Compensator Approximate Compressor (CAC). These designs optimize majority logic (ML) compressors, reducing hardware complexity and power consumption while maintaining high computational accuracy.

The proposed multiplier consists of three key stages:

1) Stage 1 - Partial Product Reduction

- Utilizes five ACMLC-based half adders (HAs) and an exact full adder (FA).
- A 3-input ACMLC compressor removes one partial product (PP) per stage, eliminating five AND gates per column.
- Eight unused AND gates from Stage 1 are repurposed in Stage 2 for compression, reducing overall circuit area.
- Truncation technique: Instead of traditional truncation, a constant-value assignment fixes four least significant bits (LSBs) to p0p1p2p3 = 0110, eliminating ten additional AND gates.

2) Stage 2 - Enhanced Compression Using CAC

- The first and last columns in Stage 2 employ CAC compressors, increasing compression accuracy.
- Four additional ACMLC compressors are introduced, ignoring input X4, further reducing hardware complexity.
- The original 64 AND gates required for an 8-bit multiplier are reduced to 49 gates, saving area and power.
- Two exact HAs and three exact FAs are included to maintain accuracy.
- The Carry output from CAC in Stage 2 is forwarded to the final stage.

3) Stage 3 - Final Addition and Ripple Carry Optimization

- Traditional ripple carry adders (RCAs) require a large number of compressors. The proposed design minimizes this by setting:
- Sum = 1
- Carry = 1
- The approximate component in the final stage includes:
- One HA with two constant inputs (1,1) functioning as an inverter.
- Three FAs with a constant input of '1', implemented using XOR and OR gates.

C. Final Results

- By combining ACMLC and CAC, the proposed multiplier achieves:
- 49% area reduction vs. exact multipliers.
- 93% lower energy consumption.
- 12.6% smaller transistor count vs. ML-based multipliers.
- Total transistors: 786 (compared to 900 in ML-based and 1530 in exact multipliers).

III. RESULTS

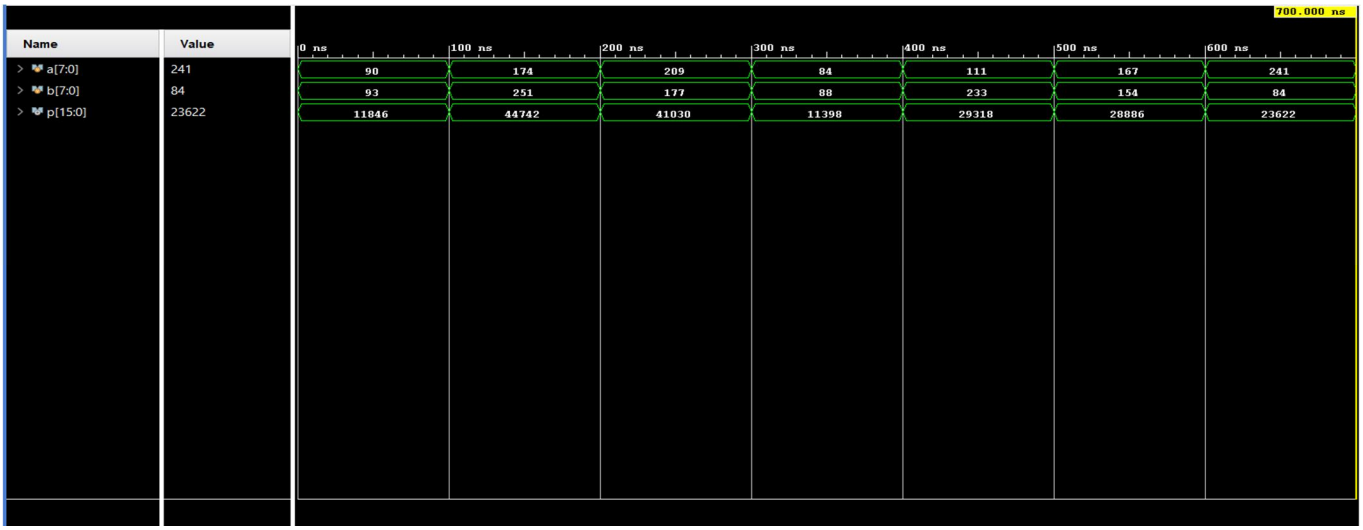


Fig. 6a Multiplication Output

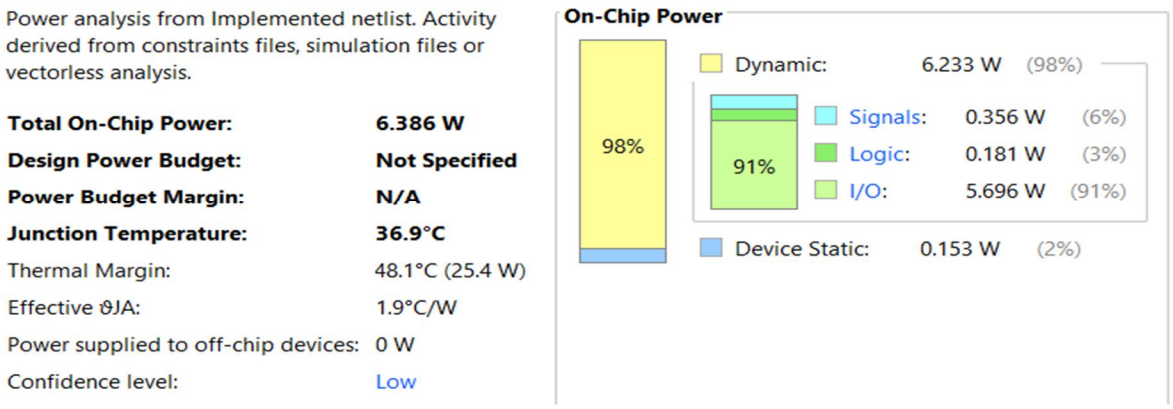


Fig. 6b Power Output

Name	Slice LUTs (134600)	Slice (33650)	LUT as Logic (134600)	Bonded IOB (400)
proposed_ACMLC_and_CAC	31	10	31	32

Fig. 6c LUT Count Output

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	6	5	12	a[6]	p[14]	9.262	3.914	5.348	∞	input port clock
Path 2	∞	6	5	12	a[6]	p[15]	9.260	3.918	5.341	∞	input port clock
Path 3	∞	6	5	12	a[6]	p[13]	8.810	3.917	4.893	∞	input port clock
Path 4	∞	5	4	12	a[6]	p[11]	8.593	3.800	4.793	∞	input port clock
Path 5	∞	5	4	12	a[6]	p[12]	8.329	3.788	4.541	∞	input port clock
Path 6	∞	5	4	11	a[5]	p[9]	7.596	3.600	3.996	∞	input port clock
Path 7	∞	4	3	12	a[6]	p[10]	6.948	3.507	3.441	∞	input port clock
Path 8	∞	4	3	7	a[3]	p[4]	6.942	3.667	3.275	∞	input port clock
Path 9	∞	3	2	5	a[1]	p[6]	6.687	3.348	3.339	∞	input port clock
Path 10	∞	4	3	7	a[3]	p[7]	6.603	3.468	3.135	∞	input port clock

Fig. 6d Time Delay Output

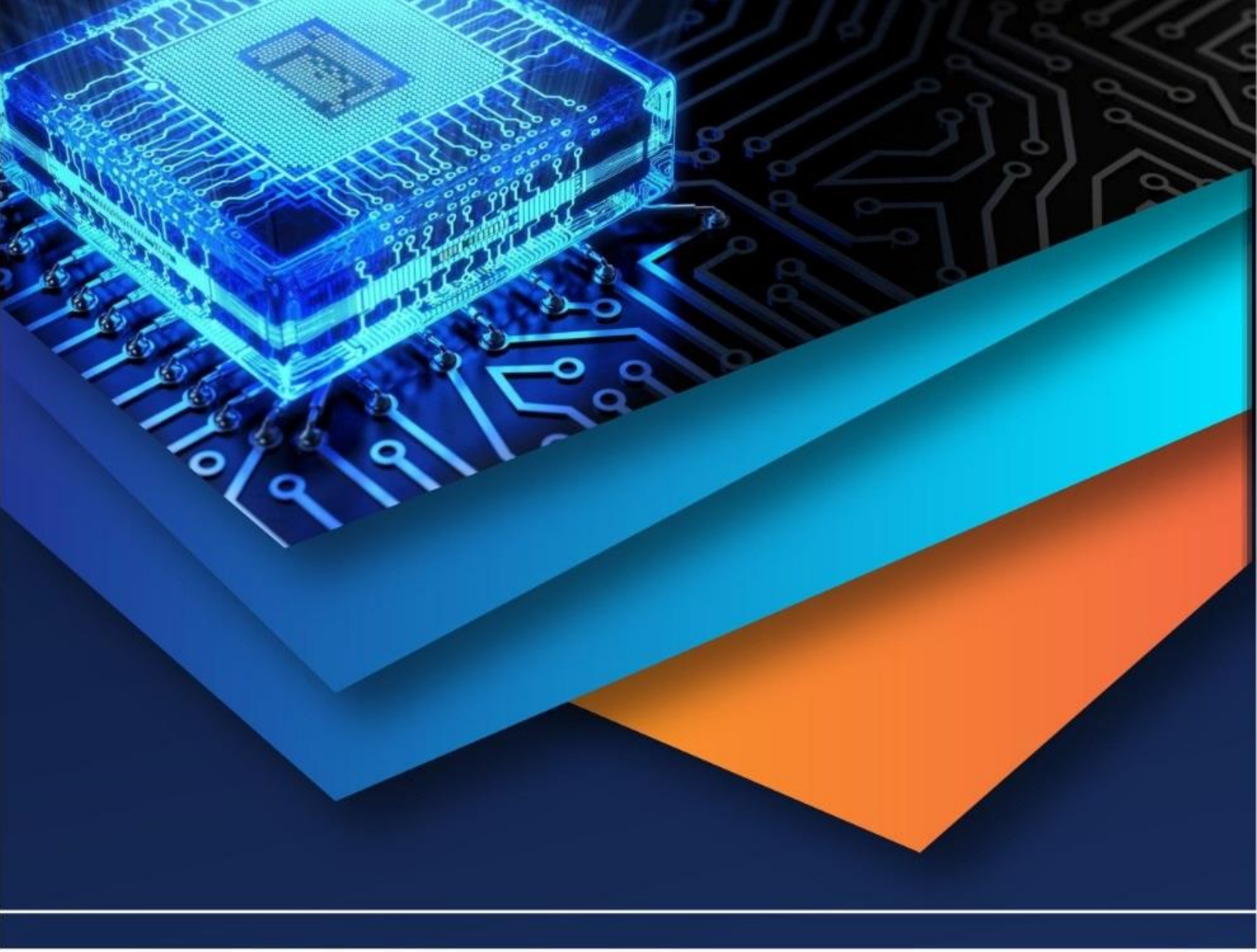
The proposed ACMLC-based multiplier with CAC integration demonstrates efficiency in power, area, and computation. The simulation results confirm correct multiplication outputs, validating its functionality. Power analysis reveals a total on-chip power consumption of 6.386 W, with 98% dynamic power and a junction temperature of 36.9°C. The design is resource-efficient, utilizing only 31 LUTs, 10 slices, and 32 bonded IOBs, indicating minimal hardware overhead. Timing analysis shows the highest total delay at 9.262 ns, with logic delay around 3.914 ns, suggesting a balanced trade-off between speed and complexity. By leveraging ACMLC-based compressors and CAC, the design eliminates redundant AND gates, reducing transistor count by 49% compared to an exact multiplier. This optimization leads to significant area and power savings while maintaining accuracy. Overall, the proposed multiplier effectively balances performance and efficiency, making it a compelling alternative to traditional and ML-based multipliers.

IV. CONCLUSION

In this paper, we proposed an 8-transistor ACMLC compressor, a 20-transistor CAC, and an approximate 8-bit multiplier for accurate and efficient image multiplication. The compressor has small footprint and low power consumption at the expense of a relatively high error rate. To compensate for the negative errors, we propose CAC, exhibiting seven errors, with only one being negative. We propose an ACMLC/CAC-based approximate multiplier to exploit the proposed compressors' unique characteristics. Relative to an exact multiplier, the proposed multiplier exhibits 50% area reduction and 93% power savings. The proposed multiplier exhibits superior performance across most evaluated metrics compared to state-of the-art approximate multipliers. The Pareto results reveal that despite their lower accuracy, ML-based proposed circuits are promising for low-power and energy dissipation applications.

REFERENCES

[1] W. Liu, C. Gu, M. O'Neill, G. Qu, P. Montuschi, and F. Lombardi. Security in Approximate Computing and Approximate Computing for Security: Challenges and Opportunities. Proceedings of the IEEE, 2020.
[2] W. Liu, F. Lombardi, and M. Schulte. Approximate Computing: From Circuits to Applications [Scanning the Issue]. Proceedings of the IEEE, 2020.
[3] A. Momeni, J. Han, P. Montuschi, and F. Lombardi. Design and Analysis of Approximate Compressors for Multiplication. IEEE Trans. on Computers (TC), 2015.
[4] S. Venkatachalam and S. Ko. Design of Power and Area Efficient Approximate Multipliers. IEEE Trans. on Very Large-Scale Integration Systems (TVLSI), 2017.
[5] M. Ha and S. Lee. Multipliers With Approximate 4–2 Compressors and Error Recovery Modules. IEEE Embedded Systems Letters (ESL), 2018.
[6] O. Akbari, M. Kamal, A. Afzali-Kusha, and M. Pedram. Dual-quality 4:2 compressors for utilizing in dynamic accuracy configurable multipliers. IEEE Trans. on Very Large-Scale Integration Systems (TVLSI), 2017.
[7] F. Sabetzadeh, M.H. Moaiyeri, and M. Ahmadinejad. A Majority-Based Imprecise Multiplier for Ultra-Efficient Approximate Image Multiplication. IEEE Trans. on Circuits and Systems I (TCAS I), 2019.
[8] IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. XX, NO. X, JANUARY 2024



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