



iJRASET

International Journal For Research in
Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 14 **Issue:** X **Month of publication:** October 2026

DOI: <https://doi.org/10.22214/ijraset.2026.85163>

www.ijraset.com

Call: ☎ 08813907089

E-mail ID: ijraset@gmail.com

ESP32 Based LVDC Fault Location using IOT

Parinita M. Muneshwar¹, Sapna J. Bamniya², Sukruti L. Bhoyar³, Om E. Bhogekar⁴, Darshan D. Shende⁵, C. S. Kamble⁶
^{1, 2, 3, 4, 5}UG Students, Department of Electrical Engineering

⁶Department of Electrical Engineering, Priyadarshini College of Engineering, Hingna Road, Nagpur-440019, Maharashtra, India

Abstract: This paper describes the circuit and firmware of a ground-fault locator for a 24 V line that uses no resistor ladder and no analog measurement. Four transmit optocouplers energise four phase lines one at a time. A 4×4 matrix of series diode and switch pairs connects each phase line to four distance columns, and each column drives a receive optocoupler's LED. An ESP32 reads the four receive outputs as digital levels, so the phase is given by the energised line and the distance by the conducting column.

The 24 V and 3.3 V domains use separate grounds and are joined only through optocouplers, which was confirmed from the netlist. The ESP32 also creates its own WiFi access point and serves a status page from its LittleFS flash file system, so no router or internet connection is needed.

Analysis of the schematic gives 9.5 mA of transmit LED current, 4.7 mA of receive LED current, a receive logic-low level of about 0.2 V against a limit near 0.8 V, a 32 ms matrix scan, and a worst-case display latency of about 1.1 s. The design is validated analytically; bench measurements on a built prototype remain future work.

Keywords: Ground Fault Location, Optocoupler Isolation, Diode Matrix, ESP32, Access Point, LittleFS, Embedded Web Server.

I. INTRODUCTION

Finding the position of a ground fault on a cable is difficult when the cable is buried, because repair crews must otherwise dig along the whole route. Methods for locating faults in shielded power cables are surveyed in IEEE Std 1234 [1], and the classical resistive methods are covered in power-system texts such as [2].

A public Arduino and IoT project [3] models the cable as a chain of series resistors. A ground fault changes the resistance seen by the source, an ADC measures the resulting voltage, and a cloud service shows the result. This approach has three drawbacks for a 24 V line. The ADC of a 3.3 V controller cannot accept the sense voltage without an attenuator, and the ESP32 ADC is non-linear near the ends of its range [4]. The distance resolution depends on resistor tolerance. The controller also shares a ground with the line, and the display needs an internet connection.

The design in this paper removes all three. Phase and distance are encoded by which crossing of a matrix conducts, so the readout is digital. Optocouplers carry every signal across the barrier between the 24 V line and the ESP32. The ESP32 hosts the user interface itself, as a web page on its own WiFi network. The main contributions are: (i) a schematic for a 4×4 diode-matrix locator with eight optocouplers; (ii) a check from the netlist that the two ground domains are separate; (iii) an access-point web interface served from LittleFS; and (iv) an analytical evaluation of currents, logic levels, timing and resource use.

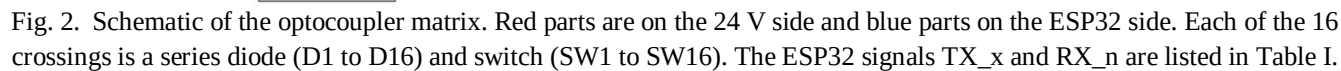
II. SYSTEM ARCHITECTURE

Fig. 1 shows the system. A 24 V supply feeds four transmit optocouplers (U1 to U4), one per phase line. The phase lines enter a 4×4 matrix. Its four columns each end at a receive optocoupler (U5 to U8). The ESP32 (U9) drives the LEDs of U1 to U4 and reads the outputs of U5 to U8, and it drives an IZC character LCD (J1). A phone or computer joins the ESP32 WiFi network and opens the status page.

The four phase lines are named PH_A, PH_B, PH_C and PH_N, the four columns DIST1 to DIST4, and the ESP32 signals TX_A to TX_N and RX_1 to RX_4. The same names appear in the schematic of Fig. 2 and in the exported netlist.



Fig. 2 shows the matrix part of the circuit. The ESP32 and LCD connections are listed in Table I instead of being drawn, so that the schematic stays easy to read.



A. Transmit Stage

Each TX optocoupler (U1 to U4, PC817 class) has its LED driven from an ESP32 pin through a 220 Ω resistor (R1 to R4) to GND_ESP. Its phototransistor collector is tied to +24 V and its emitter forms the phase line. Neglecting the pin output drop, the LED current is

$$I_{TX} = (V_{DD} - V_F) / R_{TX} \quad (1)$$

With $V_{DD} = 3.3$ V, $V_F = 1.2$ V and $R_{TX} = 220$ Ω , $I_{TX} = 9.5$ mA, well under the 40 mA absolute maximum of an ESP32 pin [4]. Only one TX pin is high at a time.

B. Matrix and Series Diodes

Phase line p connects to column d through a series diode and switch. The diode (1N4148) has its anode on the phase line. In the bench model each switch is a push button that stands for a ground fault at that phase and distance. If SW_{pd} is closed and phase p is energised, current flows from the phase line through the diode and switch into column d. The detection rule is

$$F(p, d) = [\text{phase p on}] \wedge [RX_d \text{ low}] \quad (2) \text{ where } F(p,$$

$d) = 1$ means a ground fault on phase p at distance d.

The diodes stop false readings when several switches are closed. Suppose SW at (p, d), (p', d) and (p', d') are all closed, with only phase p energised. Without diodes, current could run from column d back through phase line p' and out through column d', so $RX_{d'}$ would read low although no switch is closed at (p, d'). The diode in each branch blocks current from a column back into a phase line. The unenergised phase lines also float, because their TX phototransistors are off.

C. Receive Stage

Each column ends in a 4.7 k Ω resistor (R5 to R8) that sets the current through the LED of a receive optocoupler (U5 to U8). The LED cathode returns to GND_24V. The receive phototransistor has its emitter on GND_ESP and its collector on a net RX_n , which has its own 10 k Ω pull-up (R9 to R12) to 3.3 V and goes to an ESP32 input. The RX LED current is

$$I_{RX} = (V_L - V_{F,LED} - V_D - V_{CE,sat}) / R_{RX} \quad (3)$$

With $V_L = 24$ V, $V_{F,LED} = 1.2$ V, $V_D = 0.7$ V, $V_{CE,sat} = 0.2$ V and $R_{RX} = 4.7$ k Ω , $I_{RX} = 4.7$ mA. The power in each of R5 to R8 is 0.10 W, inside a 0.25 W rating.

The pull-up current when the receive transistor is off is small, and when it is on the transistor must sink it. The ESP32 internal pull-up (nominally 45 k Ω) is in parallel with R_{PU} , so

$$I_{PU} = V_{DD} / (R_{PU} \parallel R_{int}) = 0.40 \text{ mA} \quad (4)$$

An RX optocoupler with a current transfer ratio CTR_{RX} of at least 50 % produces at least $0.5 \times 4.7 \text{ mA} = 2.3 \text{ mA}$, which is 5.8 times I_{PU} . The logic-low level is then about $V_{CE,sat} = 0.2$ V, below the input-low limit of roughly $0.25 V_{DD} = 0.8$ V for an ESP32 pin [4].

D. Isolation and Grounding

The schematic uses two ground nets. GND_24V holds the return of the 24 V supply and the cathodes of the RX LEDs. GND_ESP holds the ESP32, the LCD, the TX LED cathodes and the RX emitters. A script over the exported netlist lists the parts that have pins on both nets, and the result is U5, U6, U7 and U8 only. Each of these is an optocoupler whose LED is on GND_24V and whose emitter is on GND_ESP, so no copper path joins the two grounds. A PC817-class part has a collector-emitter rating of 80 V and a nominal isolation voltage of 5 kV_{rms} [5]. The TX optocouplers also cross the barrier, with the collector at +24 V and the LED on GND_ESP.

The TX stage must supply I_{RX} , so the required transfer ratio is

$$CTR_{TX} \geq I_{RX} / I_{TX} = 0.49 \quad (5)$$

This is met by the 50 % minimum of common PC817 grades, with little margin. Because the RX stage needs only 0.40 mA to switch (4), a lower TX collector current reduces I_{RX} but does not stop detection.

TABLE I
ESP32 PIN MAP AND PASSIVE VALUES

Signal	ESP32 pin	Part / value
TX_A, TX_B, TX_C, TX_N	GPIO 25, 26, 27, 33	R1 to R4, 220 fi
RX_1 to RX_4	GPIO 16, 17, 18, 19	R9 to R12, 10 kfi
SDA, SCL (J1 LCD)	GPIO 21, 22	IZC, 0x27
Column resistors	none	R5 to R8, 4.7 kfi
Crossing diodes	none	D1 to D16, 1N4148

IV. FIRMWARE AND WEB INTERFACE

A. Matrix Scan

For each phase, the firmware sets the TX pin high, waits 3 ms for the optocoupler to settle, reads the four RX pins (low means conducting), and sets the pin low again. Each phase is read twice and the two readings are combined with a logical AND so that one noisy read cannot produce a fault. The first phase with a conducting column is reported, and within it the nearest column. The full 4×4 state is also stored for the web page.

B. Access Point and Web Server

The ESP32 is set to access-point mode with a WPA2 password, address 192.168.4.1 and at most four clients. A small DNS server answers every name with the ESP32 address, so a phone that joins the network is sent to the status page. The page is a single HTML file kept in LittleFS [6], [7] and sent by the built-in web server. Any unknown path returns a redirect to the page.

The page requests /api/status once per second. The reply is a JSON object holding the fault flag, phase, distance in kilometres, uptime, column and row names, the 4×4 matrix state, and the last ten events. The page draws a status banner, the matrix with conducting crossings highlighted, and the event list. The interface is read-only, so it cannot change the state of the line.

V. ANALYTICAL EVALUATION

A. Timing

One read of a phase takes 3 ms of settling and 1 ms of release. With two reads for each of four phases the scan time is

$$T_{\text{scan}} = 4 \times 2 \times (3 + 1) \text{ ms} = 32 \text{ ms} \quad (6) \text{ The scan}$$

starts every 100 ms. A fault is therefore known to the ESP32, and shown on the LCD, within $T_{\text{det}} \leq 100$

+ 32 = 132 ms. The browser polls once per second, so the worst-case time until the web page shows it is

$$T_{\text{UI}} \leq T_{\text{det}} + 1 \text{ s} \approx 1.13 \text{ s} \quad (7)$$

B. Resource Use

The matrix needs $N + M$ signals for N phases and M distances, against $N \times M$ for one input per crossing. For 4×4 this is 8 pins instead of 16. The page file is 6.3 kB and the status reply is under 1 kB, so one client adds roughly 0.5 kB/s of traffic.

TABLE II
SUMMARY OF ANALYTICAL RESULTS

Quantity	Value
TX LED current, I_{TX}	9.5 mA
RX LED current, I_{RX}	4.7 mA
Power in R5 to R8	0.10 W each
Pull-up current, I_{PU}	0.40 mA
RX current margin	5.8×
RX logic-low level	$\approx 0.2 \text{ V}$
Matrix scan time	32 ms
Worst-case display delay	$\approx 1.13 \text{ s}$
GPIO pins for matrix	8 (vs. 16)
Parts on both grounds	U5 to U8 only

VI. DISCUSSION

An earlier circuit-simulation model of this matrix tied all four RX collectors to one shared pull-up. That merges the four rows into one signal, so the distance could not be read. Each RX output now has its own pull-up (R9 to R12), and the model also used a single ground symbol, which hid the isolation question. The two ground nets and the netlist check were added for this reason.

The matrix gives discrete distances. Finer resolution needs more columns and more RX optocouplers, which grows the part count as $2 \times M$ for the sense side. The design detects ground faults only, and line-to-line and open-circuit faults would need other elements. If faults appear on two phases at once, the firmware reports the first phase, although the page shows the whole matrix. The LCD backpack is powered from 5 V, so its SDA and SCL pull-ups may reach 5 V, which an ESP32 pin does not tolerate. A level shifter or a 3.3 V supply for the backpack avoids this.

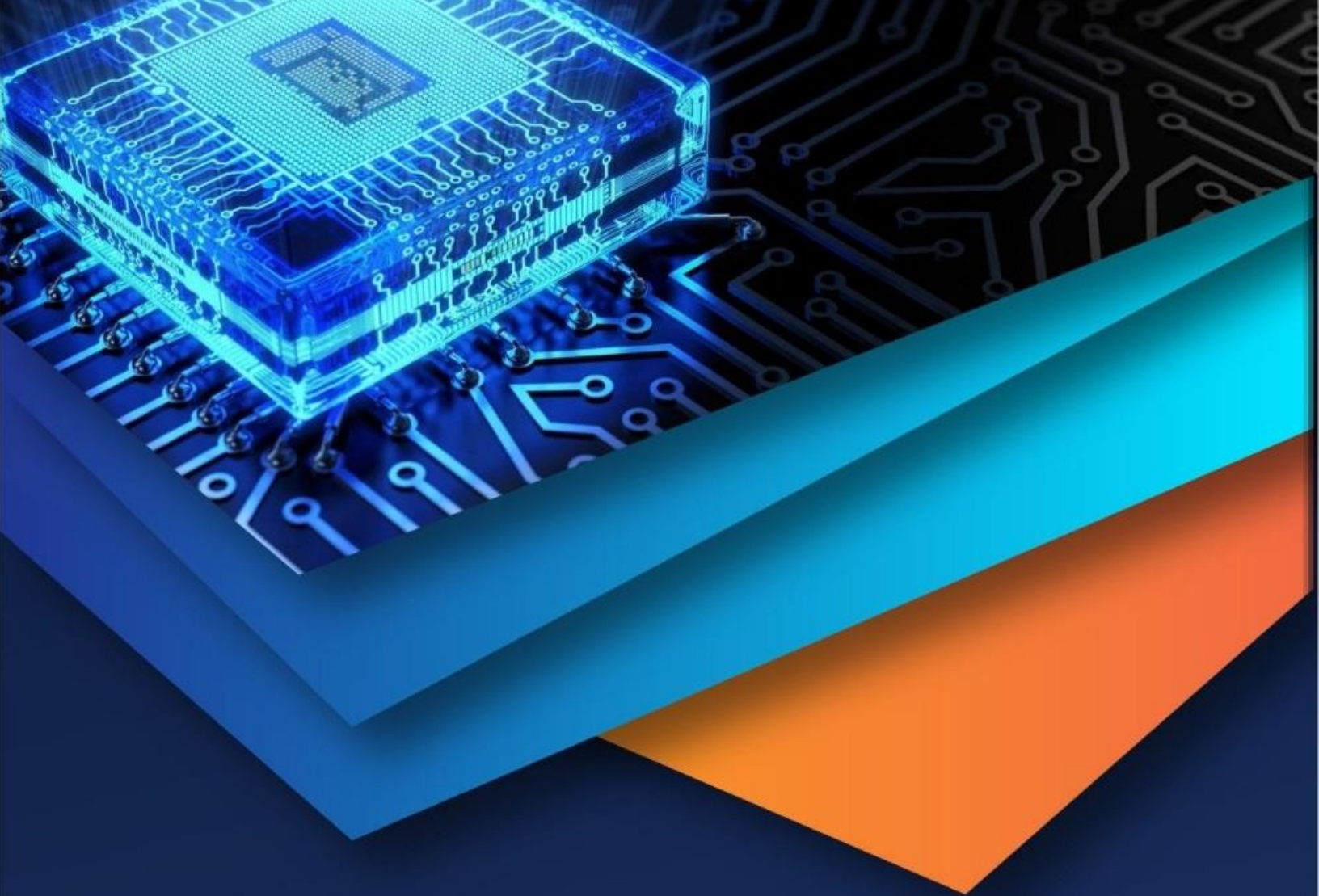
All results here come from the schematic and nominal datasheet figures. The CTR, diode drop and pull-up values may differ on a real board. The next step is a bench test with a 24 V supply that records the RX levels, the TX collector current and the display delay.

VII. CONCLUSION

A 24 V ground-fault locator was designed with eight optocouplers and a 4×4 diode matrix, read digitally by an ESP32 that also serves its own WiFi status page from LittleFS. The analysis gives 9.5 mA and 4.7 mA LED currents, a $5.8\times$ margin on the receive stage, a 32 ms scan, and a display delay of about 1.1 s, with the two ground nets joined only through optocouplers. Bench measurements, a line-to-line extension and a larger matrix are the next steps.

REFERENCES

- [1] IEEE Guide for Fault-Locating Techniques on Shielded Power Cable Systems, IEEE Std 1234, 2019.
- [2] J. J. Grainger and W. D. Stevenson, Jr., Power System Analysis. New York, NY, USA: McGraw-Hill, 1994.
- [3] eather0056, "Line-to-ground and line-to-line fault detection over IoT," GitHub repository. [Online]. Available: <https://github.com/eather0056/LINE-TO-GROUND-AND-LINE-TO-LINE-FAULT-DETECTION-OVER-IOT>
- [4] Espressif Systems, ESP32 Series Datasheet. Shanghai, China: Espressif Systems.
- [5] Sharp Corporation, PC817 Series Optocoupler Datasheet. Osaka, Japan: Sharp Corp.
- [6] Espressif Systems, "Arduino core for the ESP32." GitHub repository. [Online]. Available: <https://github.com/espressif/arduino-esp32>
- [7] littlefs-project, "littlefs: A little fail-safe filesystem designed for microcontrollers." GitHub repository. [Online]. Available: <https://github.com/littlefs-project/littlefs>



10.22214/IJRASET



45.98



IMPACT FACTOR:
7.129



IMPACT FACTOR:
7.429



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089  (24*7 Support on Whatsapp)