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Flipped Voltage Follower based LDOs for Precise Clocking Circuits: A Comparative Study

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***Abstract:** This work presents a comparative study between basic Flipped Voltage Follower (FVF), Cascoded FVF (CAFVF) and Buffered FVF (BFVF) Low Dropout Regulators (LDO) along with simulation results in tsmcN40 PDK.The designs support a load current of 5u-10mA with a on-chip capacitive load of 100fF, for a dropout of 700 mV (From 1.8V to 1.1V). This work also employs both miller conmpensation and non-dominant pole cancellation techniques in BFVF to get better phase margin and PSRR. Line regulation of 3.3 mV/V and load regulation of 20.4 uV/mA was obtained for 10mA load current, with less than 0.5 uS response time in BFVF.*
***Index Terms:** FVF, LDO, Fast response, CAFVF, BFVF*

I. INTRODUCTION

The motivation for developing Low Noise LDO for clocking circuits stems from the critical need for precise and stable timing signals in electronic systems. Clocks are fundamental in synchronizing various components within a circuit, and any noise or instability in the power supply can directly affect the performance of these clock signals. Noise in the power supply can introduce jitter and phase noise into the clock signal, which can degrade the overall performance of the system, leading to errors and reduced reliability.

Low noise LDOs are specifically designed to minimize power supply-induced variations, providing a clean and stable voltage to clock circuits. This ensures that the clock signals remain accurate and consistent, which is essential for high- performance computing, telecommunications, and data pro- cessing applications. FVF based LDOs have less reponse time compared to traditional LDOs and good noise performance. Another advantage is that it doesn't require large load capac- itor and can work sufficiently well with as low capacitance as 40pF.

II. LITERATURE SURVEY

Literature review on different LDO architectures is made first and then FVF is choosen as it has fast transient response, minimum load and line regulation, appreciable PSRR and very low RMS noise. In [1], the methods for slow loop feedback in FVF are described and tri-loop architecture is implemented, PSRR max of -10dB is achieved. This also uses a Super Source Follower (SSF) , a load cap of 300pF is used and UGB of 400 MHz is achieved. Paper [5] explains in detail all the FVF architectures available and their advantage and disadvantage. It also discusses the design aspects of the CAFVF and BFVF, along with stability and bandwidth expansion methods. In [9] , overshoot and undershoot damper along with Negative Capacitive Circuit (NCC) are used to achieve -76 dB PSRR at 1 MHz and 131 mV/V line regulation. In [14], tri-loop architecture is implemented with SSF based LSFVF, which achieved 600MHz UGB, line regulation of 37.1 mV/V and load regulation of 1.1 mV/mA. It had voltage variation of 82 mV at T_{edge}.

In [6], difference between on-chip and off-chip topologies in LDO architectures are explained and design considerations for on-chip capacitor architectures are elucidated. Also enhance- ment of stability and PSRR using multiple error amplifiers and frequency compensation stage are mentioned with brief introduction to different topologies like differentiator, trans- impedance and voltage subtractor.

In [15], the methods of increasing bandwidth of FVF loop are discussed. The effect of introducing Source Follower, Super Source Follower and Voltage Combiner are explained and results are shown. In [8], N-type FVF is implemented with SSF and cascoded current sources and PSRR of -84dB is achieved at 1 MHz. It also has very less noise of 17.2 nV/sqrt(Hz) is obtained by using low load capacitance of 50 pF.

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III. BASIV FVF AND CASCODED FVF

The basic FVF structure is shown in Figure 1. The control

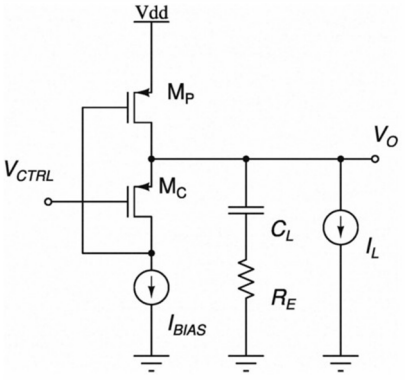


Fig. 1. Basic FVF structure.

voltage is generated from op-amp and is shown in Figure 2. The output of regulator is descreibed by below equations:

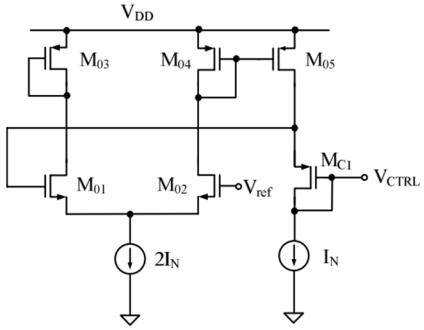


Fig. 2. Control voltage generator.

$$V_{ctrl} = V_{ref} - V_{SG(MC1)} \quad (1)$$

$$V_O = V_{ctrl} - V_{GS(C)} \quad (2)$$

$$V_O = V_{ctrl} + V_{SG(C)} \quad (3)$$

$$V_O = V_{ref} - V_{SG(MC1)} + V_{SG(C)} \quad (4)$$

From above equations, it can be concluded that if $V_{SG(MC1)}$ and $V_{SG(C)}$ are equal,

$$V_O = V_{ref} \quad (5)$$

One of major drawbacks of basic FVF LDO is minimum loading requirement . When the I_L is minimum ,the overdrive voltage of M_P will reduce & M_C will be pushed to trio region thus altering the output voltage . This can be avoid by using bleeding current at the output which will continuou source current from LDO but at the cost of increased pow consumption. Cascoded FVF is the improved version of FVF design to mitigate minimum loading requirement. The schematic shown in Figure 3. M_B acts as common gate amplifier which

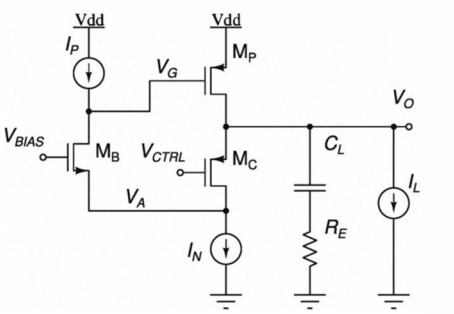


Fig. 3. Cascoded FVF structure.

will increase the gate voltage of M_P making it to supply only required current even at minimum load and keeps M_C in saturation across varying load . Also V_A is fixed to keep the current sink I_N in saturation at all times, shown in (6)

$$VA = VBIAS - V_{GS(M_{BIAS})} \quad (6)$$

Even though minimum loading requirement is mitigated in CAFVF , the pole present at the gate of M_P is still at lower frequency i.e., low fast loop bandwidth due to high impedance appearing at the node as well as large aspect ratio of M_P leading to high parasitic capacitance . Also it has no control on undershoot or overshoot.

IV. BUFFERED FVF

BFVF is a combination of CAFVF and a level shifter which contains a source follower that can push the pole at gate of the power transistor to high frequency thus increasing the bandwidth. Also it has control on both overshoot and undershoot. Schematic is shown in Figure 4

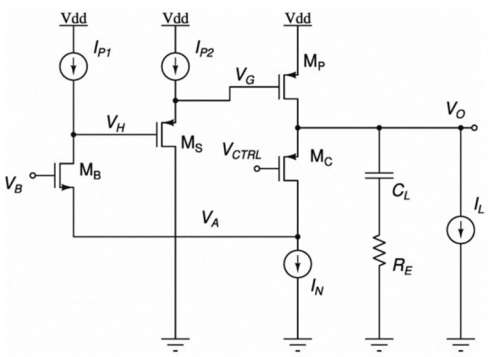


Fig. 4. Buffered FVF structure.

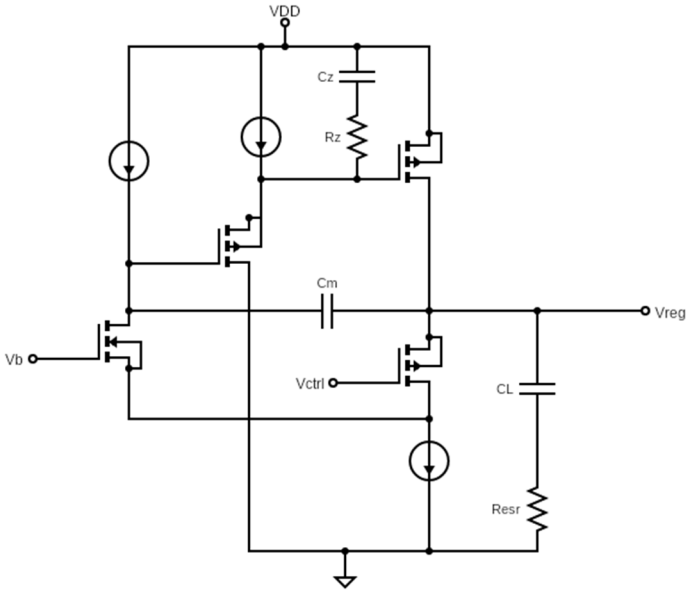


Fig. 5. Improved Buffered FVF structure.

pole is now V_H , which makes it constant pole which doesn't vary with load current, thus more easy to compensate using miller compensation. Output is the first non-dominant pole, and can be cancelled by introducing a solid zero at V_G, which should occur just before non-dominant pole. The improved schematic is shown in Figure 5. The values of C_m, C_z and R_z has to be decided accordingly. C_m is miller capacitance and C_z and R_z are used for zero insertion.

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V. SIMULATION RESULTS

The simulation results for FVF is shown in Figure 6 Line

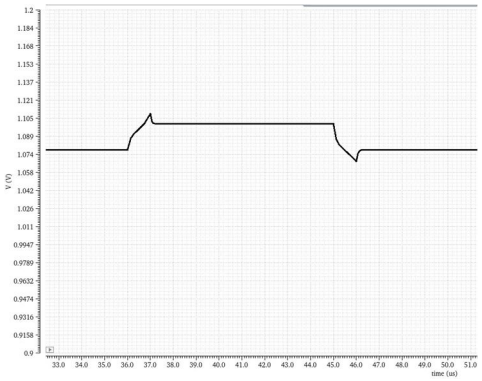


Fig. 6. FVF transient response.

regulation and load regulation was more, and moreover more bleeding current as high as 2 mA was required to make it work when supply reached 1.98, else fast loop was failing. The output for CAFVF is shown in Figure 7. Although output is stable, the undershoot is more and can't be controlled by any bias current in circuit. This is mainly due to miller capacitance, which directly couples the output to gate transistor of pass transistor.

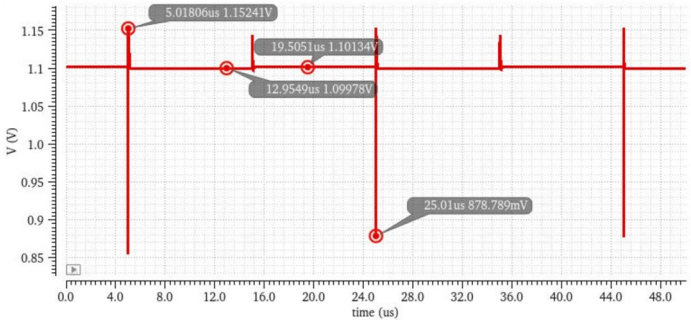


Fig. 7. CAFVF transient response.

Moving onto BFVF, the results are shown in Figure 8 The observations from BFVF simulations are :

1) Load regulation is 204uV/10mA.
2) Line regulation is 1.2mV/360mV.
3) Output was settling between 1.107 - 1.114V across corners.
4) Overshoot and undershoot are very minimal. Small ringing found at overshoot but all outputs are settling.

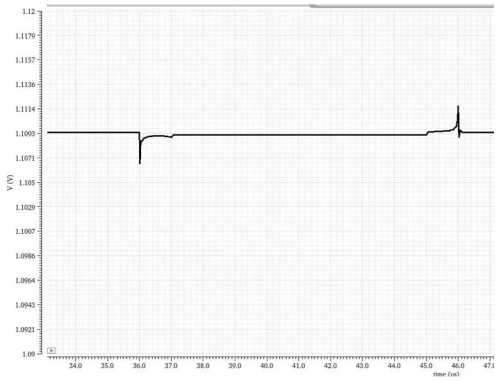


Fig. 8. BFVF transient response.

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5) PM is maintained at 45 degree, which is sufficient for stability.

6) The DC PSRR is -45dB, but as frequency approaches the unity gain, PSRR increases and variation from supply couples to output. The maximum PSRR observed was - 9.375dB at 35.48 MHz.

7) For a fixed frequency of 10 MHz, the RMS noise was between 15 to 25 nV/sqrt(Hz).

The PSRR response is shown in Figure 9

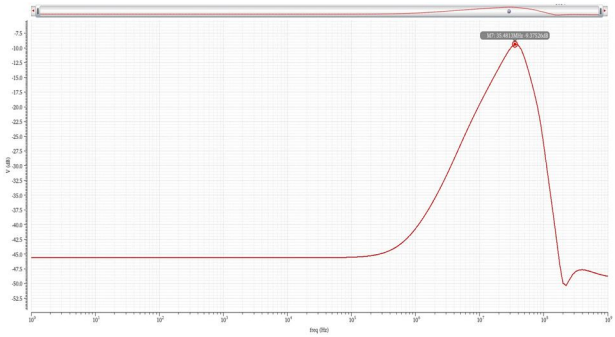


Fig. 9. BFVF PSRR response.

Design was verified across PVT corners and results are shown in Figure 10

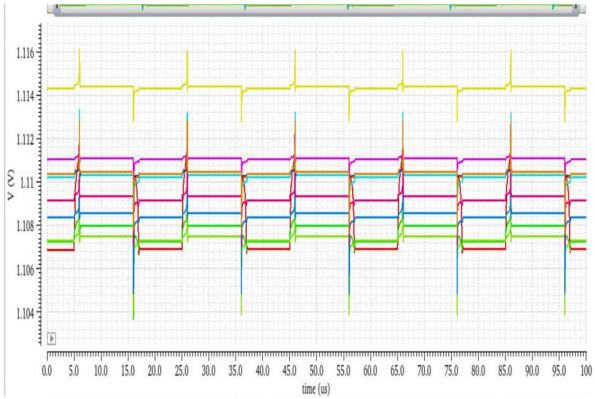


Fig. 10. BFVF across corners.

To check robustness, monte-carlo simulation was run and results are shown in Figure 11. It can be observed that for a 200 point run, min and max are 1.105V to 1.115V, with a standard deviation of 1.768mV, and all test points passed.

VI. CONCLUSION AND FUTURE SCOPE

The conclusion drawn from three designs are elucidated in Table I

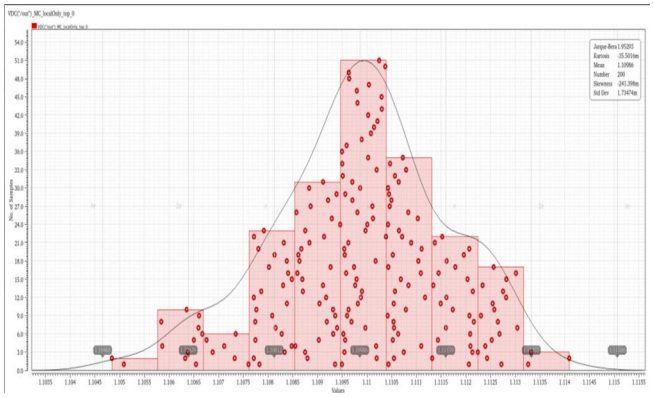


Fig. 11. Monte Carlo Analysis.

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TABLE I
COMPARATIVE ANALYSIS

Para-meters	Architectures		
	FVF	*CAFVF*	*BFVF*
Min current	High	Zero	Zero
Poles	Two	Three	Four
Dom. pole node	V_G	V_G	V_H
Line regulation	Not settling	More	Less
Load regulation	High	Low	Low
V_{spike}	Low	High	Low
PSRR	Worst	Moderate	Good
UGB	High	Moderate	Moderate
Loop gain	Low	Moderate	High

The target output voltage was 1.1V with 3% variation, that means output can vary from 1.067 to 1.133V. The actual output varied between 1.107 to 1.114V across all corners, which is well within the target. DC Load regulation is 20.4uV/mA. DC line regulation is much less than 1mV/V and transient line regulation is 3.33mV/V. PSRR of -9.3 dB maximum was observed and overshoot and undershoot were in control, both being less than 2.5mV. The future scope of the project can be listed as below :

1) Different approach to be taken for frequency compensation, as miller capacitance will worsen the PSRR
2) PSRR has to be reduced still, by applying different methods and techniques
3) Techniques to decrease the load capacitor further has to be studied and implemented
4) Layout to be implemented and verify post-layout simulation results
5) The design has to be tested with a real load inside the chip, rather than simulations

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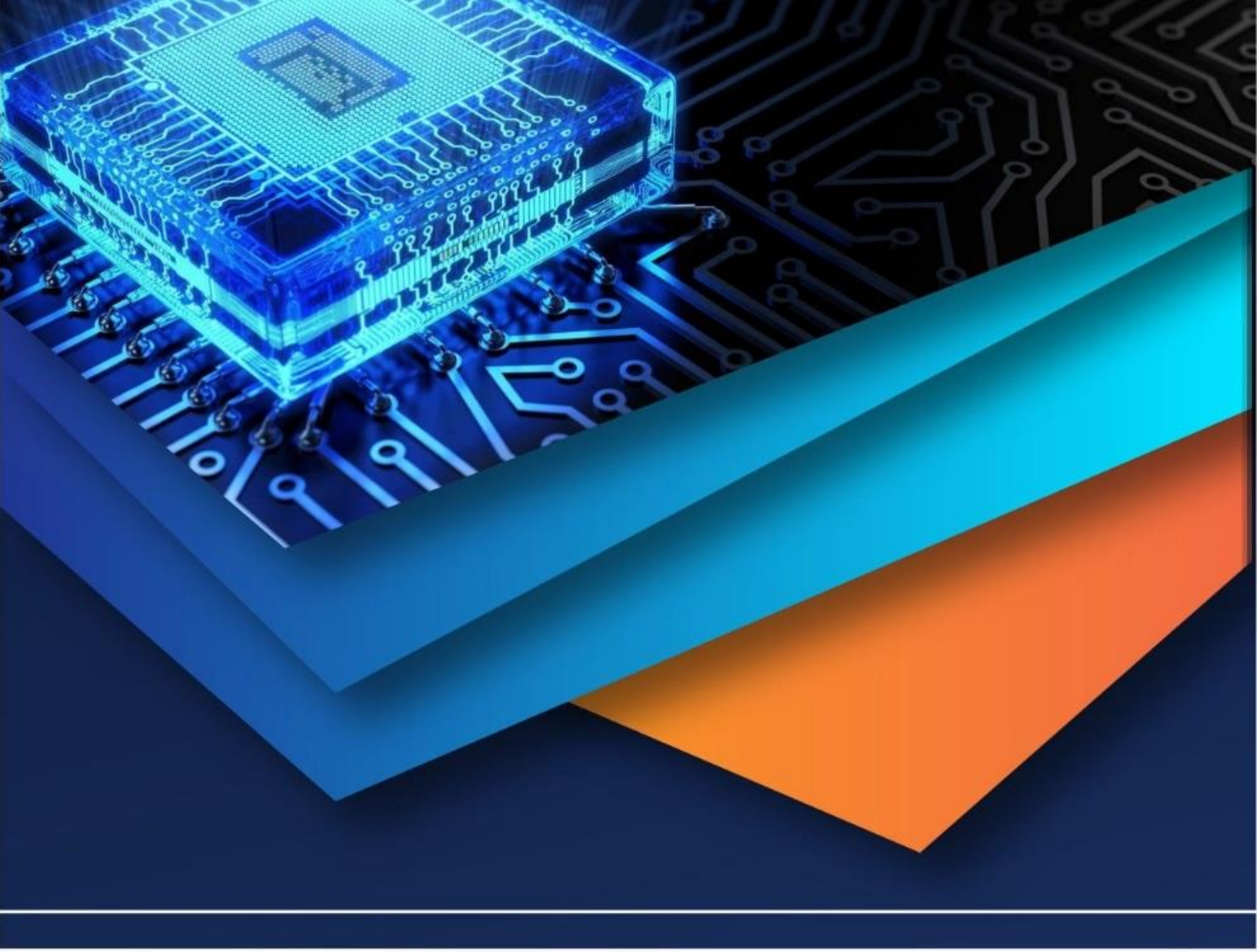
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