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# FPGA Implementation of Digital Modulation Schemes Using Verilog HDL

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***Abstract:*** ***This paper describes the design and development of an FPGA-based digital Modulation Scheme for high-resolution Communication Application. We are focusing on implementation of Verilog based code simulation for fundamental and widely used digital modulation techniques such as Binary Amplitude-shift keying (BASK), Binary Frequency-shift keying (BFSK), Binary Phase-shift keying (BPSK) and Quadrature Phase Shift Keying(QPSK). In this work the idea of sinusoidal signals that have been generated is plain sailing in nature and based on fundamentals of signal sampling and quantization. Such concept of sinusoidal signals generation is not unfamiliar but somehow simplified using sampling and quantization in time and amplitude domain, respectively. The whole simulation is done on Modelsim and Xilinx-ISE using VERILOG Hardware descriptive language. The work has been accomplished on Thirty two bit serial data transmission with self-adjustable carrier frequency and bit duration length.***

***Keywords: QPSK, BPSK, BASK, BFSK, DDS, Phase Shifting, Sampling***

## I. INTRODUCTION

In general communication modulation is “the process of varying one or more properties of a periodic waveform i.e., the carrier-signal, for transmitting a modulating signal that contains information”. Modulation of a sine waveform is used to transform a baseband message signal into a pass band signal. A device that performs modulation is known as a modulator. A device that performs the inverse operation of modulation is known as a demodulator. A device that performs operations as modulator and demodulator is known as modem. The digital modulators major work is to transfer a digital bit stream over an analog band pass channel, for example over the wireless network (where a limit of band pass filter ranges in frequency is between 150 and 3400 Hz), or over a limited radio frequency band. Digital modulation facilitate frequency division multiplexing (FDM), where several low pass information signals are transferred simultaneously over the same shared physical medium, using separate pass band channels (several different carrier frequencies). And the line coding, is to transfer a digital bit stream over a base band channel, typically a non-filtered copper wire such as a serial bus or a wired local area network as it is one of the aim of digital modulators. The aim of digital modulation methods is to transfer a narrow band digital signal, in this scheme, as a bit stream over another digital transmission system. Despite simple transmitter and receiver architecture of Digital modulators and its modulation technique is still commonly used in wireless communication such as WPAN (Wireless Personal Area Network). Amplitude shift keying (ASK) is data transfer technique with different amplitude of carrier frequency. As it is sensitive to propagate the channel variation, thus it is has been widely used in low- power wireless transceiver for system simplicity. For low power consumption, wireless communication systems exist in implantable medical devices, ingestible capsule endoscopy and multichannel neural recording. The ASK modulation/demodulation scheme, for both RF-band and baseband transceiver, was presented. This design is realized on future mobile memory I/O interface for energy efficient. However, BPSK is as well as showing better Bit. These digital modulation techniques were implemented on FPGA device. Simulation results consist of bit error rate of digital signals of modulators, source consumption of BASK, BFSK, BPSK and QAM FPGA-based, bit rate of BASK and BPSK on Xilinx ISE suite complier using verilog language. Thus digital modulators were implemented on FPGA. In addition to, bit error rate of BASK and BPSK modulation techniques was compared using Xilinx. In this paper, for BPSK and BASK modulation, FPGA based modulator is presented. Finally, simulation results are obtained.

Whereas BPSK, QPSK, 16-QAM and 64-QAM are the permitted modulation schemes. Our work includes multimode inter leaver design with all possible modulation scheme permitted. The inter leaver comprises of two blocks: address generator and inter leaver memory. The former is FSM based and the later is implemented using internal memory of FPGA. The FSM based address generator operates at higher frequency and can provide better FPGA resource utilization. Use of internal memory always provides better results in terms of memory access time, power consumption and real estate occupancy of circuit board compared to external memory.

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Two approaches have been adopted to model the inter leaver memory: using dedicated internal memory and using distributed internal memory. Comparative analysis between the two techniques in terms FPGA resource utilization and maximum operating frequency shows that the former technique out performs the later except the use of dedicated internal memory. The estimated power consumption of both techniques is equal and found to be 56mW. In addition our approach supports on the fly computation of inter leaver addresses. The Digital Signal Processing and the Channel Coding Stages where implemented within a FPGA (Spartan 3 line, from Xilinx) to take advantage of the massive parallel computation power of these devices and to have the possibility to scale up to ASIC devices.

## II. RELATED WORKS

FPGA Implementation of High Throughput Digital QPSK Modulator using Verilog HDL, K.Anitha1, Umesharaddy2, B.K.Sujatha. This paper proposes a Quadrature Phase Shift Keying (QPSK) using two different methods. QPSK is one of the forms of Phase Shift Keying (PSK) modulation scheme. Generally a conventional QPSK modulator with Direct Digital Synthesizer (DDS) and arithmetic multiplier separates base band signal into I and Q phase which consumes low throughput with complexity in hardware implementation. Hence to generate high throughput QPSK modulator, the first proposal uses an up and down accumulator for carrier generator instead of DDS and arithmetic multiplier is modified as BOOTH multiplier. The second proposed method will produce the QPSK signal which is based on stored QPSK phase data in ROM which eliminates completely the DDS and multiplier blocks of the modulator. Performance comparison of the BPSK and QPSK Modulation Techniques on FPGA, S.O.POPESCU, A.S. GONTEAN The paper presents the comparison performance in terms of error performance between two modulation techniques, the BPSK and QPSK modulation. Both modulations were implemented on the Spartan 3E Starter Kit board. In order to compare the error performance of the two modulation techniques, it is necessary to express the error performance in terms of the average energy per bit (Eb). A brief description of theoretical aspects of the BPSK and QPSK modulations is also illustrated in the paper. This paper focuses on error performance of the BPSK and QPSK modulation techniques. Both modulations had been implemented on FPGA. FPGA Implementation of BASK-BFSK-BPSK Digital Modulators , C. Erdoğan, I. Myderrizi, and S. Minaei Field-programmable gate-array (FPGA) implementations of binary amplitude-shift keying (BASK), binary frequencyshift keying (BFSK), and binary phase-shift keying (BPSK) digital modulators are presented. The proposed designs are aimed at educational purposes in a digital communication course.

They employ the minimum number of blocks necessary for achieving BASK, BFSK, and BPSK modulation, and for full integration with the other functional parts of the Altera Development and Education (DE2) FPGA board. The input carrier signal and the bit stream (modulating signal) are user controllable. These digital modulators were developed and compiled to a Verilog Hardware Description Language (HDL) netlist, and were later implemented into an Altera DE2 FPGA board. The functionality of these digital modulators was demonstrated through simulations using the Quartus II simulation software, and experimental measurements of the real-time modulated signal via an oscilloscope.

BER Analysis for Digital Modulation Schemes Under Symmetric Alpha-Stable Noise, Fan Yang and Xi Zhang A number of important digital modulation schemes including differential phase-shift keying (DPSK), differentially encoded binary phase-shift keying (DEBPSK) and offset quadrature phase-shift keying (OQPSK), are widely used in military communications applications. Conventionally, the additive white Gaussian noise (AWGN) channel is employed to model many noisy environments. However, AWGN model is less accurate if the wireless-channel noise process is impulsive in nature. As shown in the previous literatures, symmetric alpha-stable (SαS) process is a more accurate model to characterize realistic wireless environments.

## III. PROPOSED MODULATION SCHEME DEVELOPMENT

The objective of this paper is to implement fully DDS based digital BASK, BFSK, BPSK & QPSK modulators that employ the minimum number of digital blocks suitable for software-defined radio systems and are implemented individually into the Spartan 3 FPGAs. The input carrier signal and message signal is generated using DDS, for more scalability or flexibility. Furthermore, the implemented FPGA designs can be used in a digital communication system to Demonstrate BASK, BFSK, QPSK and BPSK digital modulation techniques.

Digital modulation and demodulation can be implemented on FPGA and received considerable attention. Here modulation is done without multiplication of binary massage signal with sinusoidal carrier signal. Instead of multiplication, for each case, sample of different carrier signal was saved in ROM. The proposed method produces the BPSK/QPSK signal which is based on sine cos equations. This method eliminates completely the DDS and multiplier blocks of the modulator. The modulator design has been made generic so that it can be used as either BPSK or QPSK by use of single operational switch.

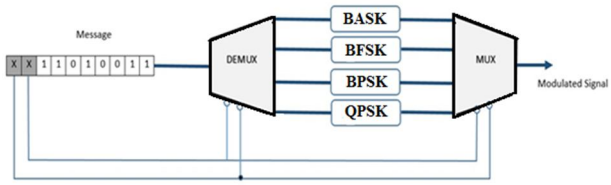
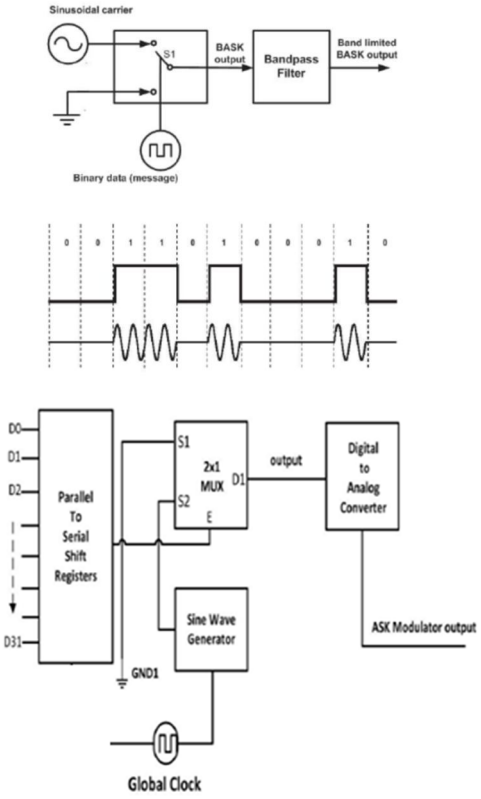



Fig1: Proposed Modulation Scheme

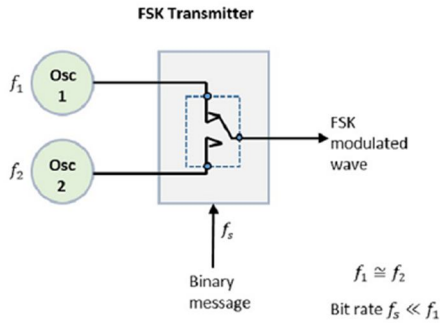
In BASK, the amplitude of the sinusoidal carrier signal is changed according to the message level ("0" or "1"), while keeping the phase and frequency constant. The following figure represents the block diagram of BASK.



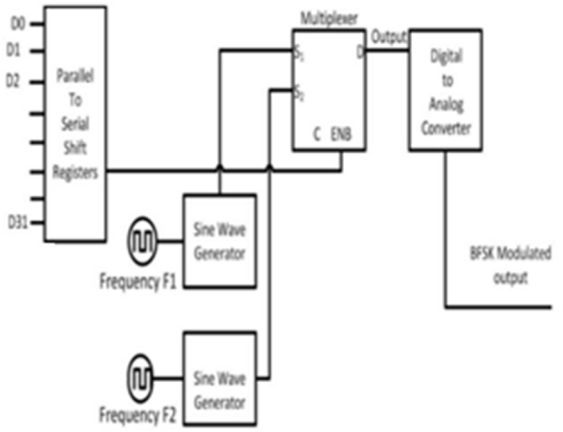

*A. BFSK*

Frequency-shift keying (FSK) is analogous to fundamental frequency modulation technique in which digital information is transmitted through deviating the frequency of the carrier signal. The carrier frequency is shifted in according to the input data stream; phase and amplitude of the carrier are maintained constant.

The FSK modulator block diagram comprises of two oscillators with a clock and the input binary sequence. Following is its block diagram.



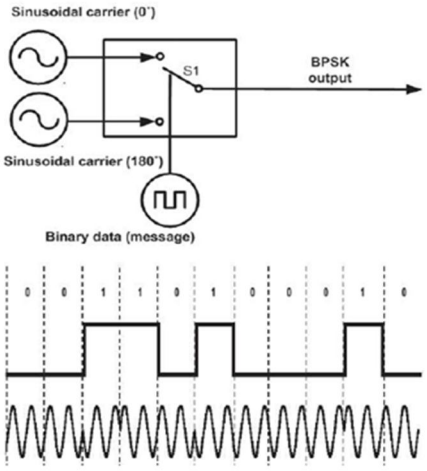
The two oscillators, producing a higher and a lower frequency signals, are connected to a switch along with an internal clock. To avoid the abrupt phase discontinuities of the output waveform during the transmission of the message, a clock is applied to both the oscillators, internally. The binary input sequence is applied to the transmitter so as to choose the frequencies according to the binary input.



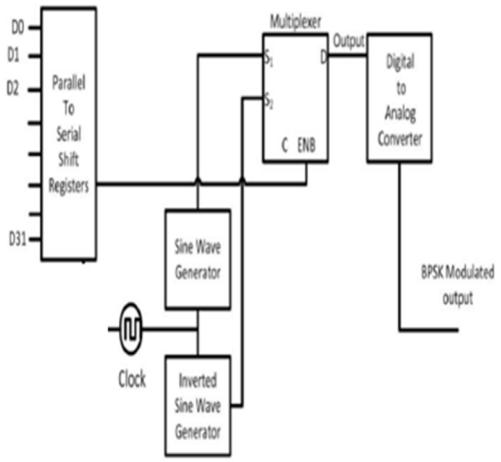

BPSK Binary Phase Shift Keying

In a BPSK modulation process, the phase of the sinusoidal carrier signal changes according to the message level (“0” or “1”) w/ith amplitude and frequency constant. BPSK is one of the simplest PSK modulation techniques. It uses two phases (0 and 180 degrees). Figure 1 shows BPSK modulation. A BPSK signal can be expressed is described by (1). Where binary message as m (t) = 0 or 1, Bit duration as T, Amplitude as A, and Carrier Frequency fc.

$$S(t) = A\ Sin\ [2\pi f_c t + m(t)\pi], 0 \le t \le T$$



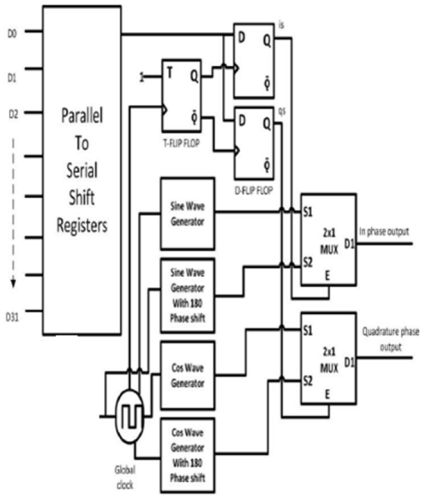

The most straightforward type of PSK is called binary phase shift keying (BPSK), where “binary” refers to the use of two phase offsets (one for logic high, one for logic low). We can intuitively recognize that the system will be more robust if there is greater separation between these two phases—of course it would be difficult for a receiver to distinguish between a symbol with a phase offset of 90° and a symbol with a phase offset of 91°. We only have 360° of phase to work with, so the maximum difference between the logic-high and logic-low phases is 180°. But we know that shifting a sinusoid by 180° is the same as inverting it; thus, we can think of BPSK as simply inverting the carrier in response to one logic state and leaving it alone in response to the other logic state. To take this a step further, we know that multiplying a sinusoid by negative one is the same as inverting it. This leads to the possibility of implementing BPSK using the following basic hardware configuration:




However, this scheme could easily result in high-slope transitions in the carrier waveform: if the transition between logic states occurs when the carrier is at its maximum value, the carrier voltage has to rapidly move to the minimum voltage. High-slope events such as these are undesirable because they generate higher-frequency energy that could interfere with other RF signals. Also, amplifiers have limited ability to produce high-slope changes in output voltage. If we refine the above implementation with two additional features, we can ensure smooth transitions between symbols. First, we need to ensure that the digital bit period is equal to one or more complete carrier cycles. Second, we need to synchronize the digital transitions with the carrier waveform. With these improvements, we could design the system such that the 180° phase change occurs when the carrier signal is at (or very near) the zero-crossing.

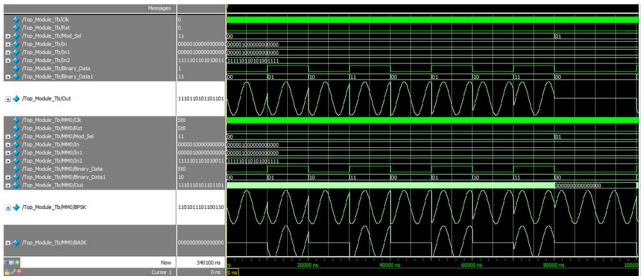
*B. QPSK*

Quadrature phase shift keying (QPSK), we need to introduce the following important concept: There is no reason why one symbol can transfer only one bit. It's true that the world of digital electronics is built around circuitry in which the voltage is at one extreme or the other, such that the voltage always represents one digital bit. But RF is not digital; rather, we're using analog waveforms to transfer digital data, and it is perfectly acceptable to design a system in which the analog waveforms are encoded and interpreted in a way that allows one symbol to represent two bits.




QPSK is a modulation scheme that allows one symbol to transfer two bits of data. There are four possible two-bit numbers (00, 01, 10, 11), and consequently we need four phase offsets. Again, we want maximum separation between the phase options, which in this case is 90°.

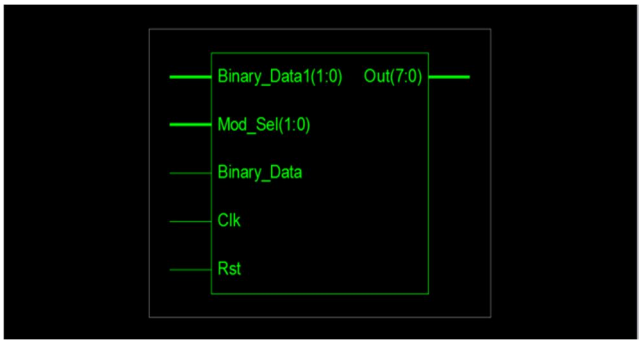
## IV. SIMULATION RESULTS



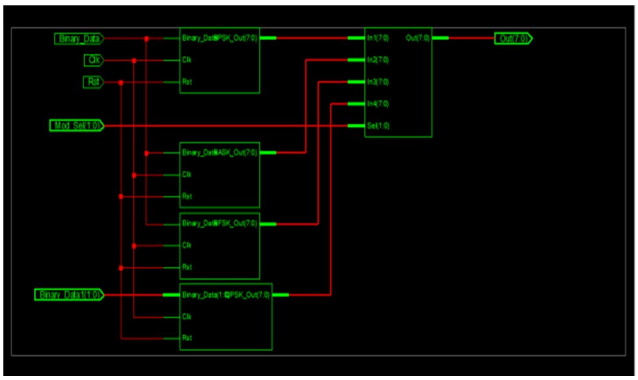
Combined Modulation Scheme Output



Individual Modulation Scheme output




RTL Schematic of Main Design



RTL Inner View of MAIN Module

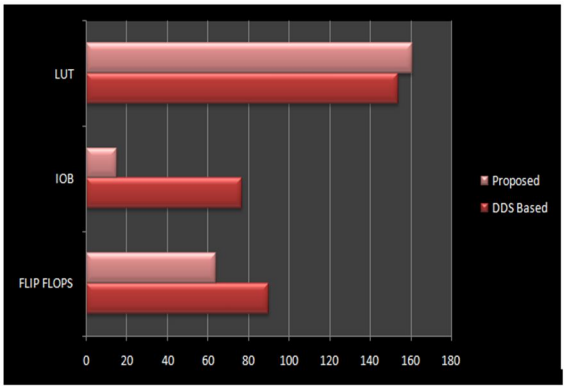
## V. COMPARISON AND ANALYSES

The Proposed Modulation design concepts are built in Verilog HDL, generated with Xilinx for various bit sizes, and the latency and area are compared. As seen in Fig., Modulation Scheme without ROM has the smallest area and has the shortest latency when compare to Conventional Modulation Scheme as the number of bits increases. The results demonstrate that using proposed design for inclusion achieves the suggested Design's overall minimum area.

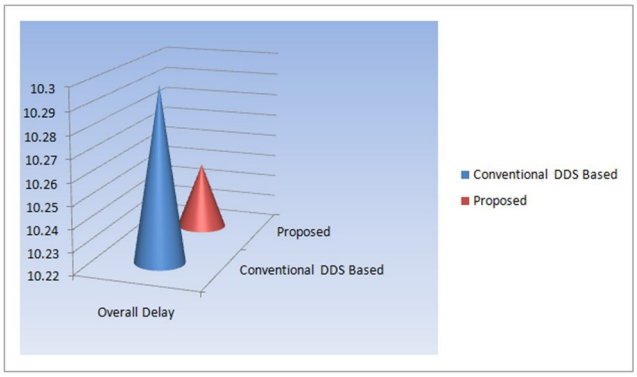
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| Method Name | | Area in Number of LUT | | Delay | | |
|---|---|---|---|---|---|---|
| Spartan 3 XC 3S 5000-4FG1156 | Gates | FLIP FLOPS | IOB | Delay | Gate or Logic Delay | Path or Route Delay |
| Existing | 1,98,813 | 90 | 77 | 10.298ns | 6.896ns | 3.402ns |
| Proposed | 2159 | 64 | 15 | 10.250ns | 6.896ns | 3.354ns |

Comparison Chart




Area Analysis



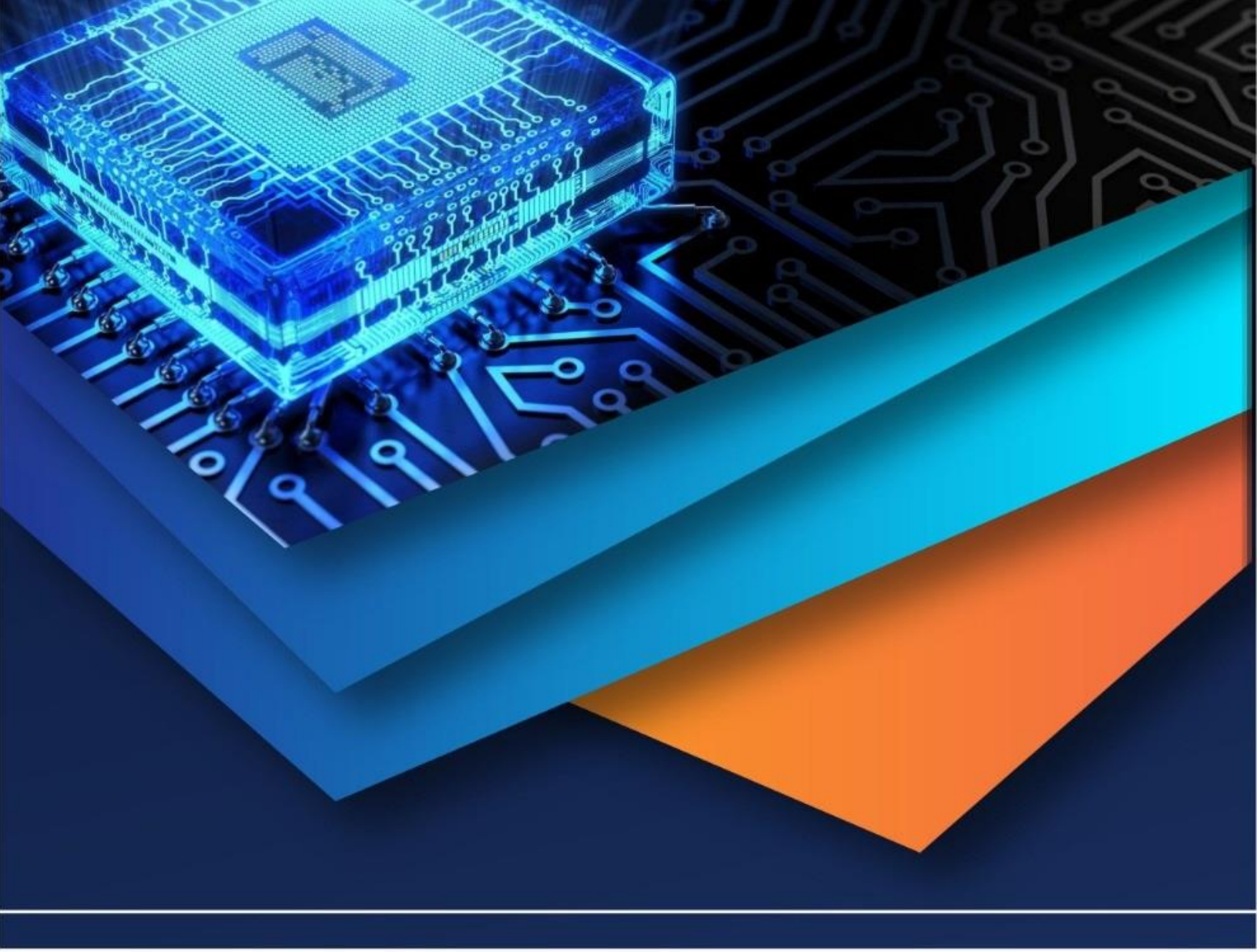

Delay Analysis

## VI. CONCLUSION

The work can be concluding that the implemented four types of modulators in the Simulation environment like BASK, BFSK, BPSK & QPSK using system generator on FPGA. The will be like to extend my current work by implementing all modulation techniques thus whole digital laboratory can be done on a single kit. FPGA implementations of BASK, BFSK, BPSK & QPSK digital modulators could be demonstrated. The main advantage of the implementations is the minimum numbers of digital blocks used for performing digital modulations, the ability to integrate with modules in FPGA boards, and the user controllability of the input signal's frequencies. The implemented FPGA designs are suitable for realization of the digital baseband-modulation part of software-defined radio systems. In addition, usage of this kind of implementation for educational purposes in digital communications laboratories or courses clearly emphasizes the correlation between different courses in electronics engineering. BASK, BFSK, BPSK & QPSK system (modulation) is designed using Verilog HDL and implemented on Spartan-3 FPGA kit.

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