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# Generation of SVPWM on FPGA to Control 3-Phase Inverter

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***Abstract:*** ***Space Vector Pulse Width Modulation (SVPWM) is a high-performance modulation strategy for voltage source inverters, offering improved DC link voltage utilization and lower harmonic content compared to traditional PWM techniques. This work presents the design and FPGA-based realization of an SVPWM algorithm implemented on a Basys-3 development board using a Xilinx Artix-7 FPGA and Verilog hardware description language. The proposed architecture exploits the parallel processing capability and deterministic execution of FPGA hardware to perform essential SVPWM operations, including Clarke transformation, sector determination, dwell time computation, and real-time pulse generation. Three-phase switching signals are generated using sector-dependent switching sequences covering all six space vector regions. The correctness of the generated PWM-A, PWM-B, and PWM-C signals is verified through simulation and validated experimentally using on-board LEDs for visual confirmation of switching transitions. Hardware results demonstrate accurate six-sector space vector synthesis, low latency, and reliable real-time operation. The proposed FPGA-based SVPWM implementation is therefore well suited for high-performance inverter applications such as motor drives and renewable energy systems.***

***Keywords: Space Vector Pulse Width Modulation (SVPWM), FPGA, Basys-3, Artix-7, Verilog HDL, Voltage Source Inverter, Three-Phase PWM.***

## I. INTRODUCTION

Three-phase voltage source inverters form the core of modern power electronic systems used in industrial motor drives, renewable energy interfaces, electric vehicles, and automation systems. The quality of inverter output voltage and current is strongly dependent on the modulation strategy used to control semiconductor switching devices. Conventional sinusoidal pulse width modulation (SPWM), although simple to implement, suffers from limited DC-link voltage utilization and increased harmonic distortion at higher modulation indices. To overcome these drawbacks, Space Vector Pulse Width Modulation (SVPWM) has emerged as an advanced modulation technique that treats the three-phase inverter as a single rotating voltage vector in a two-dimensional stationary reference frame. By optimally selecting inverter switching states, SVPWM achieves higher DC bus utilization, reduced harmonic distortion, and improved output voltage quality. Despite its advantages, real sanctioned implementation of SVPWM demands precise sector identification, accurate dwell-time computation, and deterministic switching signal generation within every sampling period. Software-based controllers such as microcontrollers and DSPs often struggle to meet these requirements at high switching frequencies due to sequential execution and timing jitter. Field Programmable Gate Arrays (FPGAs) provide an attractive hardware platform for SVPWM implementation because of their massive parallelism, fixed execution latency, and high-speed digital processing capability. This work presents the design, implementation, and experimental validation of a fully FPGA-based SVPWM controller using Verilog HDL on a Xilinx Artix-7 FPGA (Basys-3 platform). The proposed architecture executes Clarke transformation, sector identification, dwell-time calculation, and PWM synthesis in real time, ensuring accurate six-sector voltage vector generation suitable for high-performance inverter applications.

## II. OBJECTIVES

The primary objective of this research is to design and experimentally validate a real-time FPGA-based SVPWM controller for three-phase voltage source inverters.

The specific objectives are:

*1)* To develop a modular SVPWM architecture using Verilog HDL suitable for FPGA implementation.
*2)* To implement Clarke transformation and sector identification using fixed-point arithmetic.
*3)* To generate accurate dwell times ($T_1$, $T_2$, $T_0$) for all six space-vector sectors.
*4)* To synthesize symmetric PWM switching sequences for PWM-A, PWM-B, and PWM-C.

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*5)* To validate correct SVPWM operation through simulation and hardware implementation on the Basys-3 FPGA.
*6)* To demonstrate improved DC-link voltage utilization and stable real-time switching behavior.

## III.METHODOLOGY

The he proposed methodology follows a structured, hardware-oriented design approach for implementing Space Vector Pulse Width Modulation (SVPWM) on an FPGA platform. The complete SVPWM process is realized using Verilog HDL and executed in real time on a Xilinx Artix-7 FPGA (Basys-3). The methodology integrates mathematical modeling, fixed-point hardware design, simulation verification, and experimental validation.

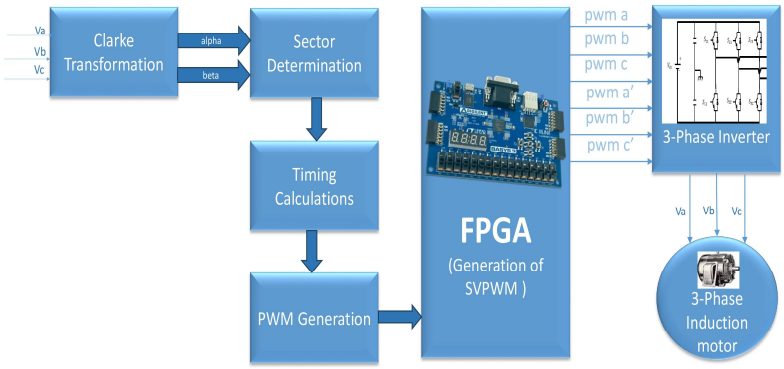



Fig. 1 Block Diagram

### A. *Reference Signal Generation*

The methodology begins with the generation of balanced three-phase reference voltages representing the desired inverter output. These reference signals are digitally synthesized within the FPGA using lookup tables (LUTs), ensuring precise phase displacement of 120° between the phases. Digital generation eliminates the need for external analog circuitry and minimizes noise sensitivity.

The generated reference voltages $V_a$, $V_b$, and $V_c$serve as the input to the SVPWM control logic and continuously rotate to emulate a three-phase sinusoidal system. .

### B. *Clarke Transformation*

To simplify space-vector analysis, the three-phase reference voltages are transformed into a two-axis stationary reference frame using Clarke transformation. This transformation converts the three-phase quantities into orthogonal components $V_d$

$$\therefore \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}$$

$$\therefore |\bar{V}_{ref}| = \sqrt{V_d^2 + V_q^2}$$

$$\alpha = \tan^{-1}\left(\frac{V_d}{V_q}\right) = \text{wt}=2\pi\text{ft}\text{ , where f = fundamental frequency.}$$

and Vq.The Clarke transformation is implemented using fixed-point arithmetic and optimized multipliers available in the FPGA DSP slices. This hardware-efficient realization ensures high-speed computation with minimal latency, enabling real-time operation at high switching frequencies.

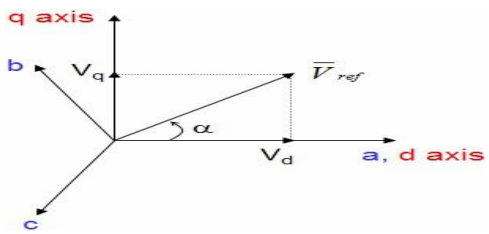



Fig. 2 Clarke Transformation

*C. Sector Identification*

The stationary reference frame components $V_\alpha$ and $V_\beta$ are analyzed to determine the angular position of the reference voltage vector within the space-vector hexagon. The hexagon is divided into six sectors, each spanning 60 electrical

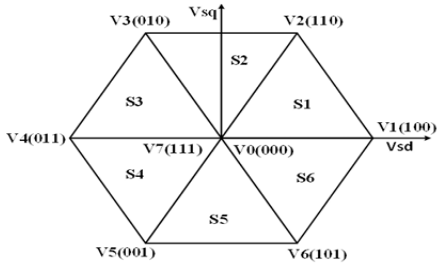



*Fig 3: space vector diagram*

degrees.Comparator-based decision logic is used to identify the active sector based on the signs and relative magnitudes of $V_\alpha$ and $V_\beta$. This parallel hardware approach ensures fast and deterministic sector detection without iterative calculations. For hardware validation, the identified sector is mapped to onboard LEDs of the FPGA, providing real-time visual confirmation of correct sector transitions.

*D. Dwell Time Computation*

Once the sector is identified, the two adjacent active voltage vectors corresponding to that sector are selected. The dwell times $T_1$ and $T_2$ for these active vectors, along with the zero-vector duration $T_z$, are calculated within each switching period.These computations are performed using fixed-point arithmetic to maintain computational efficiency and numerical stability. The calculated dwell times determine the duty cycles of the inverter phase legs and ensure accurate synthesis of the reference voltage vector. Pipelined arithmetic structures are employed to maintain continuous timing updates at high switching frequencies.

*E. Symmetric Switching Sequence Generation*

To minimize switching losses and harmonic distortion, a symmetric switching sequence is employed within each switching cycle. The switching pattern starts and ends with zero vectors, while the active vectors are applied symmetrically around the midpoint of the switching period.

$$T_Z . V_{ref} = T_1 . V_1 + T_2 . V_2$$

$$T_1 = T_Z . a . \sin(\pi/3 - \alpha)/\sin(\pi/3) \quad ; \quad T_0 = T_Z - (T_1 + T_2)$$

$$T_2 = T_Z . a . \sin(\alpha)/\sin(\pi/3) \quad ; \quad a = V_{ref}/Vdc . 2/3$$

The general switching sequence follows:

$$V_0 \rightarrow V_x \rightarrow V_y \rightarrow V_7 \rightarrow V_y \rightarrow V_x \rightarrow V_0$$

where $V_x$ and $V_y$ are the active vectors associated with the identified sector. Sector-dependent switching tables stored in FPGA registers are used to generate the correct switching order for all six sectors.

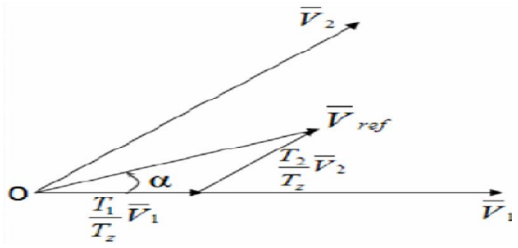



Fig. 4 $V_{ref}$ in sector 1 phase diagram

*F. Signal Generation*

Based on the computed dwell times and selected switching sequence, three synchronized PWM signals PWM-A, PWM-B, and PWM-C are generated using high-resolution counters and comparators. The PWM signals are center-aligned to reduce low-order harmonics and improve waveform symmetry.

Each PWM output directly controls one inverter leg, ensuring balanced three-phase voltage synthesis. Dead-time insertion logic is incorporated to prevent shoot-through conditions in the inverter switches.

*G. FPGA Implementation and Validation*

The complete SVPWM architecture is implemented on the Basys-3 FPGA using Verilog HDL and synthesized using the Xilinx Vivado Design Suite. Functional verification is carried out through simulation to validate sector identification, dwell-time accuracy, and PWM waveform generation.

Experimental validation is performed by mapping PWM outputs and sector indicators to the onboard LEDs of the FPGA. The observed LED blinking patterns confirm correct real-time switching behavior, smooth sector transitions, and continuous reference vector rotation.

## IV. RESULTS

The proposed SVPWM architecture was implemented on the Basys-3 FPGA board (Xilinx Artix-7 XC7A35T-1CPG236C) using Verilog HDL. The design generated three synchronized PWM outputs—PWM-A, PWM-B, and PWM-C corresponding to all six sectors of the space-vector hexagon. The FPGA operated at a 100-MHz system clock, and all computations, including sector identification, dwell-time calculation, and switching-state generation, were executed in fixed-point arithmetic.

The PWM outputs exhibited stable duty-cycle variation across all sectors, with no observable glitches or metastability during real-time operation. The deterministic timing behavior of the FPGA ensured consistent switching frequency and precise dwell-time resolution. These results verify that the implemented SVPWM module is functionally correct and suitable for integration with a three-phase inverter for further hardware-level motor-drive testing.

*A. Waveform analysis for six sectors*

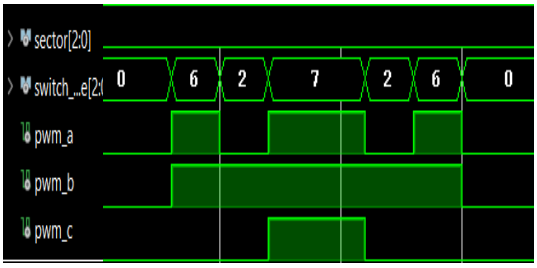



*Fig. 5 Sector1*

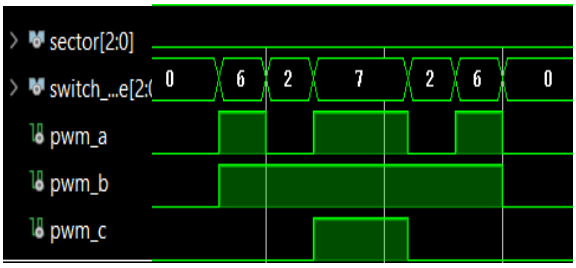



*Fig. 6*

- The switching sequence follows 0 → 2 → 6 → 7 → 6 → 2 → 0, corresponding to Sector-2 operation.
- Active vectors V2 and V6 are applied symmetrically around the switching midpoint.
- PWM-B shows the longest ON duration, while PWM-A and PWM-C switch for shorter intervals.
- Smooth transitions confirm correct timing of T1, T2, and T0.

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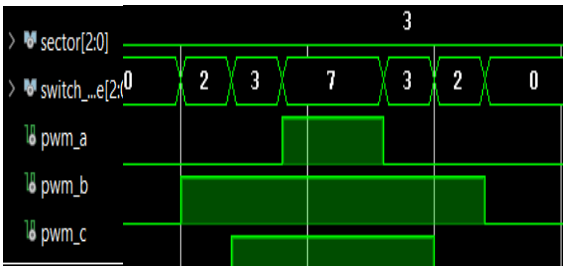



Fig.7 Sector3

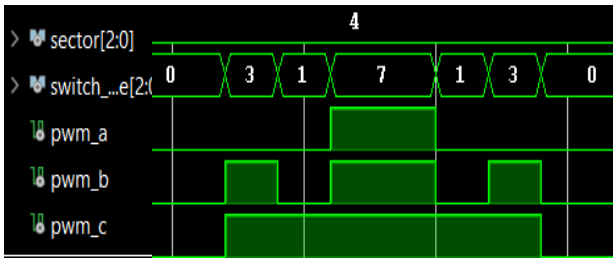



Fig. 8 Sector4

- The inverter follows the switching sequence 0 → 2 → 3 → 7 → 3 → 2 → 0.
- Active vectors V2 and V3 dominate the switching interval.
- PWM-B and PWM-C have higher duty cycles compared to PWM-A.
- Symmetrical zero-vector placement ensures reduced harmonic distortion.

- The switching pattern 0 → 1 → 3 → 7 → 3 → 1 → 0 confirms correct vector selection.
- Active vectors V1 and V3 generate the desired voltage reference.
- PWM-C maintains the longest ON duration, followed by PWM-B, while PWM-A has the shortest.
- Balanced PWM overlap validates proper phase voltage synthesis

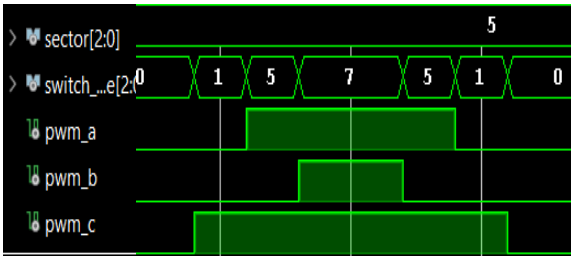



Fig. 9 Sector5

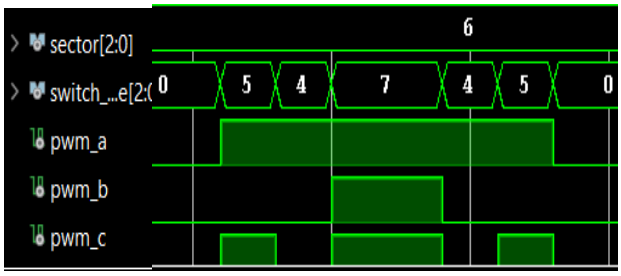



Fig. 10 Sector6

- The switching sequence 0 → 1 → 5 → 7 → 5 → 1 → 0 is observed.
- Active vectors V1 and V5 are applied symmetrically.
- PWM-C and PWM-A show higher ON durations compared to PWM-B.
- The waveform demonstrates stable inverter switching without glitches.

- The inverter follows the sequence 0 → 4 → 5 → 7 → 5 → 4 → 0.
- Active vectors V4 and V5 dominate the switching period.
- PWM-A and PWM-C exhibit longer ON durations, while PWM-B switches for a shorter interval.
- The waveform confirms smooth transition back to Sector-1, ensuring continuous SVPWM operation

*B. LED Blinking observation in FPGA:*

To validate the correctness of the switching logic, the sector-wise PWM activity was mapped to the on-board LEDs. Each LED pattern represented the active sector and its corresponding switching sequence. The LED transitions confirmed that the FPGA correctly identified all six sectors and produced the expected timing intervals T1, T2, and T0 for each switching cycle. The observed LED blinking patterns matched the theoretical SVPWM sequence, demonstrating accurate reference-vector tracking and proper modulation symmetry.

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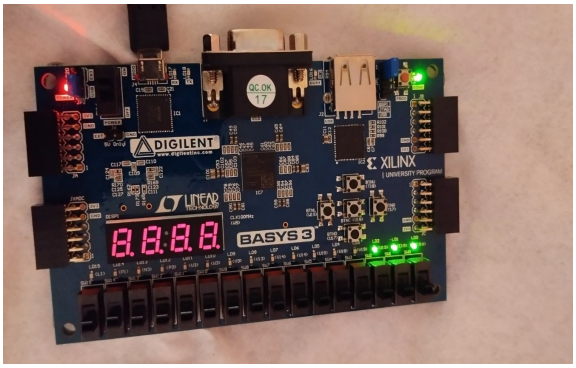



Fig 11 LED blinking in BASYS 3 xilinx Artrix-7 FPGA

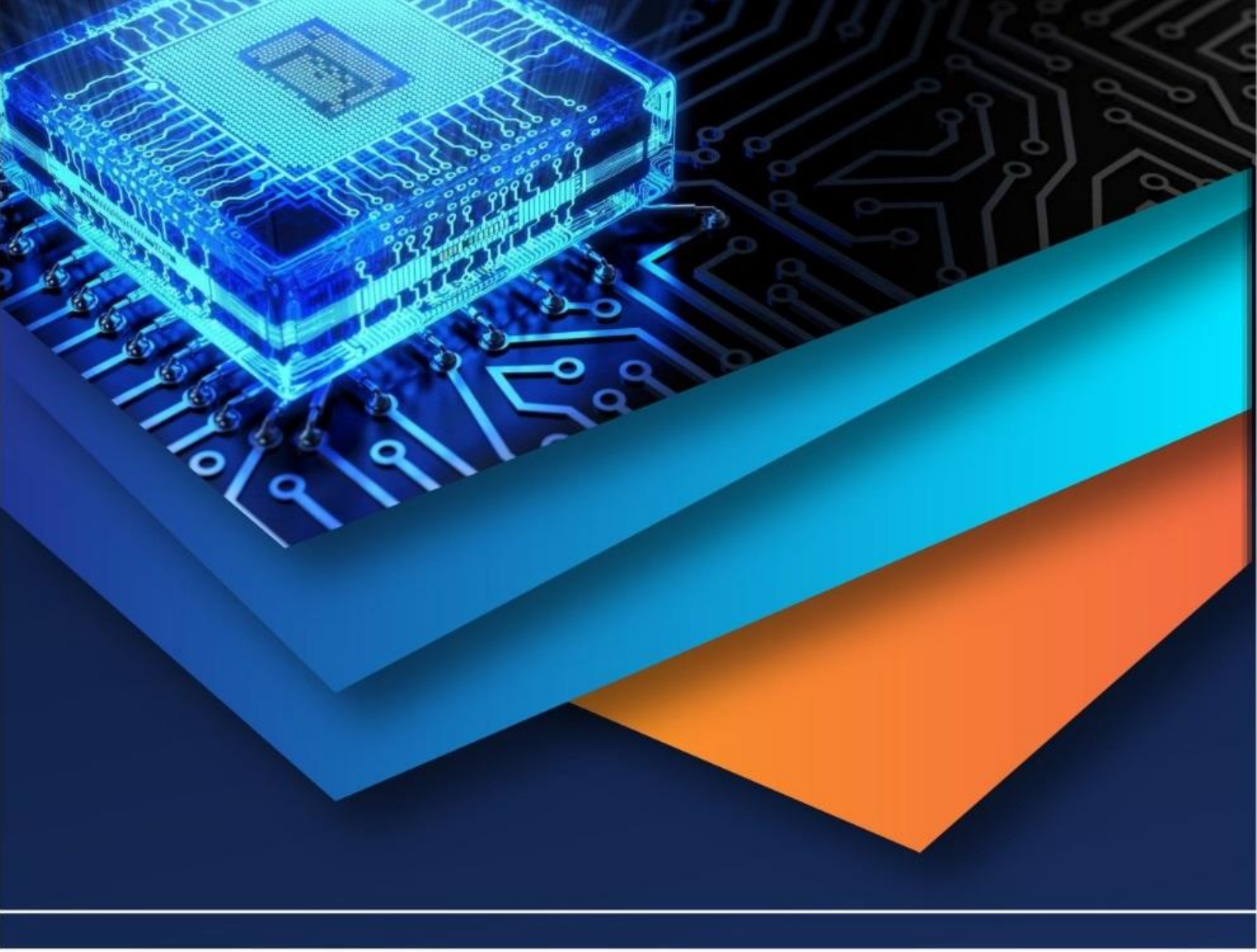
## V. CONCLUSIONS

The FPGA-based implementation of Space Vector Pulse Width Modulation (SVPWM) successfully demonstrates accurate generation of three-phase PWM-A, PWM-B, and PWM-C signals across all six space vector sectors. Hardware realization of sector identification, voltage vector selection, and switching sequence generation ensures deterministic execution with low latency and high switching accuracy. Real-time validation using on-board FPGA LEDs effectively confirms correct switching behavior and smooth sector transitions. The close agreement between simulation and experimental results verifies the correctness of the proposed SVPWM architecture. Improved DC-link voltage utilization and reduced harmonic distortion are achieved compared to conventional sinusoidal PWM techniques. Symmetrical switching sequences contribute to smoother phase voltage waveforms and stable inverter operation. The FPGA-based design exhibits reliable real-time performance and supports high switching frequencies. Overall, the results confirm the suitability of FPGA platforms for high-performance SVPWM applications in motor drive and power conversion systems.

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