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High Speed and Area Efficient Scalable n-Bit Digital Comparator

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Abstract: ***The digital comparator is a crucial design element in various applications, including scientific computations. It is optimized for general-purpose computer architecture, memory addressing logic, queue buffers, and test circuits. High-speed comparators are essential for arithmetic operations, data sorting, and decision-making processes in digital systems. Area efficiency is crucial in integrated circuit design, as it minimizes the physical space a comparator occupies on a chip, reducing manufacturing costs and optimizing performance. The term "scalable" means the comparator can be adapted to handle different word lengths (n-bit), making it versatile for various applications. This project proposes an area-efficient n-bit digital comparator with high operating speed and low-power dissipation. The comparator structure consists of two modules: the Comparison Evaluation Module (CEM) and the Final Module (FM). The CEM involves the regular structure of repeated logic cells used for parallel prefix tree structure, while the FM validates the final comparison based on results from the CEM. The design is implemented using Tanner EDA in 45nm technology.***

I. INRODUCTION

Digital comparator is a fundamental design element used in various applications, including scientific computations and test circuits. It is the key component in general-purpose computer architecture for memory addressing logic, queue buffers, and test circuits. The design of comparator logic requires optimization in terms of area, power, and speed. Some designs use dynamic logic for low-power consumption, but these have limitations due to low-speed and poor noise margin. Other designs use flat adder components and custom logic circuits for wider bit operands, but they provide slower response and area-intensive arrangements. Hierarchical prefix tree structure-based comparator improves scalability and reduces comparison delay, but may be prohibitive for wide input operands due to prolonged delay and power consumption. Parallel prefix tree structure can be improved by using two input multiplexers at each level and generate-propagate logic at the first level. However, the comparator structure has high power consumption since every cell remains active regardless of the applied operand values.The design of high-speed and low power binary comparators has gained significant attention in recent years. These digital systems are used for data comparison in arithmetic or logical operations, determining whether one number is greater than, equal, or less than another. Digital comparators are commonly used in combinational systems and can be connected in cascade arrangement to perform comparisons of longer lengths.

When comparing two binary numbers, the most significant bits (MSBs) are compared first. If these MSBs are equal, the next significant bits are compared. If not, the comparison ceases. The comparator produces three outputs: L, E, and G, which correspond to less than, equal, and greater than comparisons. This makes it essential for digital systems to have reliable and efficient data comparison tools.A magnitude digital comparator is a circuit that compares two digital or binary numbers, A and B, to determine their relative magnitudes. It uses three binary variables to indicate the outcome of the comparison, such as A>B, A<B, or A<B.

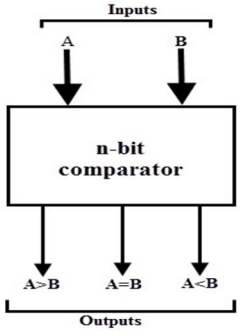


Fig .1 : N-bit digital comparator

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Magnitude comparators are crucial in microcontrollers and CPUs for data comparison, arithmetic operations, and decision-making. They are implemented in numerous devices, including auto-turn-off devices. A comparator is a decision-making tool that can be executed in multiple control devices. It accepts two binary numbers (A and B) and outputs equality (A=B) or logic 1 in two conditions (A>B or A< B).Binary comparators are essential in various circuits like microprocessors, communications systems, encryption devices, image processing, and 3D graphics. They are used to compare two n-bit bit numbers, determining their greater or equal value. Comparators are classified into Analog and Digital comparators, with the digital comparator being the primary focus. High-performance systems rely heavily on these comparators for performance and power consumption optimizations. Comparators are critical in determining the greater or equal value of two inputs.

II. EXISTING SYSTEM

This paper presents a new design for a high-speed and area-efficient N-bit digital comparator. The design is tailored for N-bit digital comparison, achieving remarkable speed without compromising area efficiency. It uses advanced circuit techniques to minimize propagation delays, enabling rapid and reliable comparisons. The design incorporates scalable elements, making it adaptable to various bit-width requirements. Low-power design principles enhance energy efficiency. Simulation results show superior performance in speed and area utilization compared to existing designs. This N-bit digital comparator is promising for applications in high-speed digital signal processing and arithmetic units.

Abdel-Hafeez,S., Gordon-Ross,A., and Parhami,B have developed a scalable digital CMOS comparator using a parallel prefix tree. This design allows for high-speed operation using conventional digital CMOS cells and reduces dynamic power dissipation by eliminating unnecessary transitions. The comparator is composed of locally interconnected CMOS gates with a maximum fan-in and fan-out of five and four, respectively. The design maintains high speed and power efficiency over a wide range and uses a reconfigurable VLSI topology for analytical derivation of input-output delay.

Vijaya Krishna Boppana, N. V., & Ren, S proposed a low-power and area-efficient 64-bit digital comparator, based on radix-4 trees. It offers lower power consumption and smaller area, making it ideal for low-power portable devices. Resource sharing is crucial, with 64 XE blocks contributing to the worst power consumption. The design can also be used for 64-bit adders and encryption devices. Lam, H.M., & Tsui, C.Y proposed a mux-based high-performance single-cycle CMOS comparator architecture, utilizing a hierarchical two-stage structure and a dynamic MUX for improved delay. The 64-bit comparator has less delay and is suitable for high-speed applications.

Saravanakumar proposes an ASIC implementation of a parallel binary comparator using Carry Look Ahead (CLA) technique. This design achieves low power and high-speed operation, especially in low-input data activity environments. The comparator is designed using VHDL code and synthesized using ALTERA QUARTUS - II. Experimental evaluation shows a reduction in delay and gate count for a 16-bit design.

Kumar, K.R.Reddy, P. M. Sadanandam, M. Kumar, A. S., & M.Raju proposed a 2T XOR gate-based full adder using the GDI technique to reduce power, improve speed, and optimize area through transistor count. The focus is on low power VLSI (Very Large Scale Integration) due to the increasing transistor count on chips. High power consumption increases the temperature of the IC and affects battery durability in portable devices. The GDI approach provides optimized conditions for the full adder design. The work is carried out in 180nm technology using LTspice tool for time delay and Xilinx 14.7 ISE for power analysis. The analysis shows that the proposed method is better than conventional CMOS.

Naseri.H & Timarchi.S propose novel circuits for XOR/XNOR and simultaneous XOR–XNOR functions, optimized for low power consumption and delay. They also propose six hybrid 1-bit full-adder circuits based on full-swing XOR–XNOR or XOR/XNOR gates. The proposed circuits have various merits in terms of speed, power consumption, power delay product (PDP), driving ability, and other factors. The researchers propose a new transistor sizing method using a numerical computation particle swarm optimization algorithm to optimize circuits. Manasi Vaidya designed a 2-bit magnitude comparator using CMOS, reducing complexity and increasing computation speed in digital devices like ADC and memory chips. The design was done using Full Adder circuit in Mentor Graphics Eldo net tool and 180nm technology file. Simulations were conducted on 0.6V, 0.8V, 1V, and 1.2V, finding the least dissipated power at 48.82pW in 0.6V but the longest delay at 53.098ns. The comparator design was compared with other logic styles. Panda, A. K., Palisetty, R., & Ray, K.C have developed an Area-Efficient Parallel-Prefix Binary Comparator for CLCG based PRBG methods. The 32-bit comparator consumes less power and less LUT area compared to magnitude and mux-based comparators. The merging circuit technique in prefix computation stages significantly reduces the area of the binary comparator. The 32-bit comparator is designed with Verilog HDL and implemented on a Spartan3E FPGA device for hardware performance.

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Reto Zimmermann's study on low-power logic styles reveals that complementary CMOS is superior to complementary pass-transistor logic (CPL) in terms of speed, area, power dissipation, and power-delay products. CMOS logic gates offer robustness, generality, and ease-of-use, making it the preferred choice for implementing combinational circuits with low voltage, low power, and small power-delay products.

Oguz Ergin's study focuses on designing fast, energy-efficient CMOS comparators for high-performance microprocessors. These comparators, used in datapath components, are often energy-inefficient due to mismatches. Ergin proposes two new circuits that primarily dissipate energy on matches, resulting in significant savings in power dissipation. The designs are evaluated using SPICE simulations and micro-architectural level statistics. This approach can improve the performance of high-performance microprocessors.

III. PROPOSED SYSTEM

The conventional comparison principle involves comparing operands A and B with unequal most significant bit (MSB) bits. The first unequal bits are used to determine the comparison outcome, and remaining bits are ignored. The comparison process starts from the (N-1)th bit and progresses to the (N-2)th bit if the MSB bits are equal.

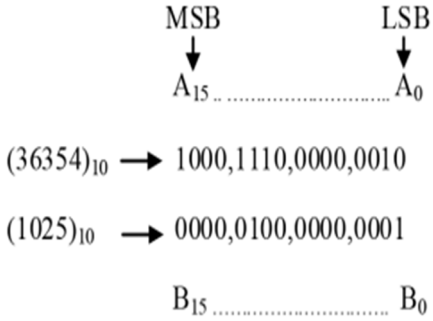


Fig 3.1 : Comparison between two 16 bit operands

The comparison process compares bit pairs from operands until an unequal pair is reached towards the LSB bit position, as depicted in Figure.

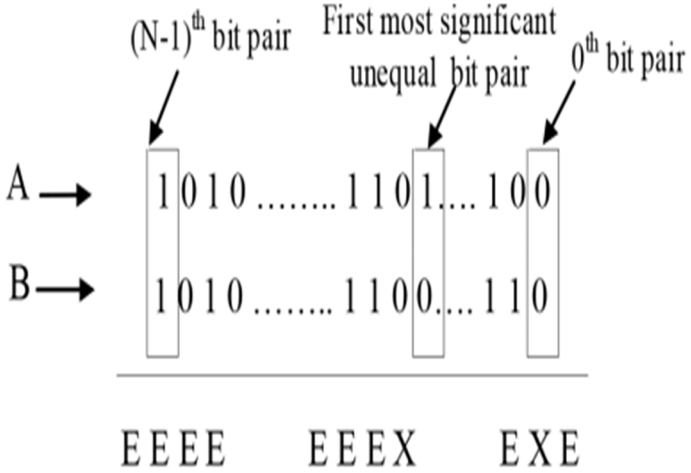


Fig 3.2 : Comparison between two N-bit operands

The unequal bit pair (X) and equal bit pair (E) are realised as

$$X = A \oplus B \quad (1)$$

$$E = A \odot B \quad (2)$$

The proposed N-bit digital binary comparator uses a flowchart and bitwise comparison to compare two N-bit input operands A and B. If the operands are equal, the comparator drives the output logic AEB to logic 1, otherwise, it checks the pre-encoder output bits from MSB to LSB.

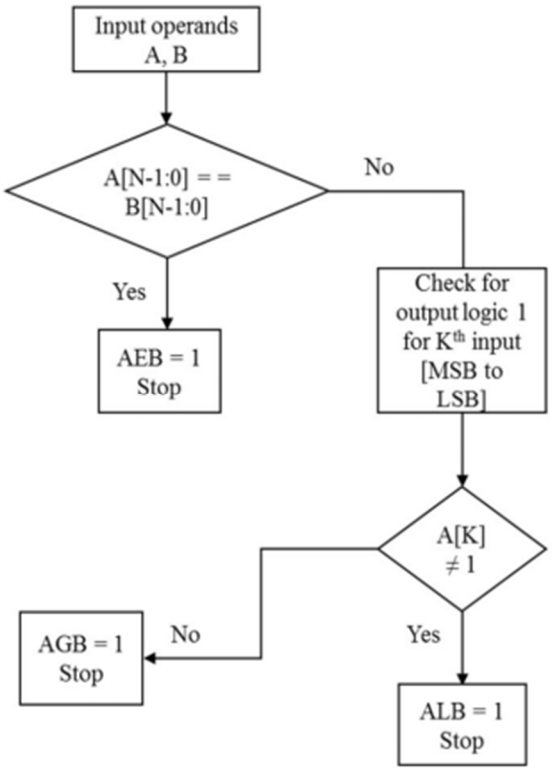


Fig 3.3 : Flowchart of the N-bit digital comparator

The output logic AGB or ALB is then driven to logic 1, reducing superfluous switching activities and limiting the dynamic power consumption of the existing comparator.

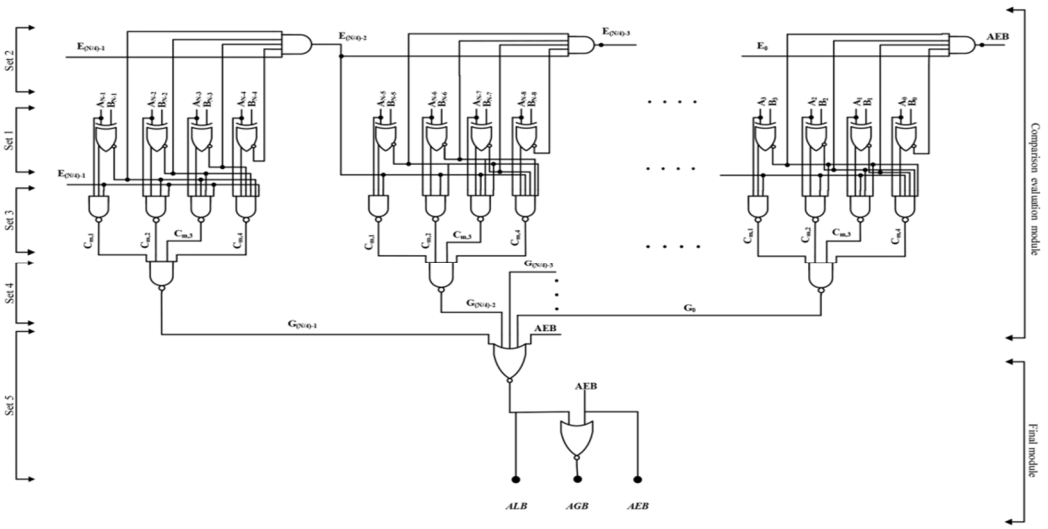


Fig 3.4 : Block diagram of N-bit digital comparator

The proposed structure for comparing two N-bit binary operands is divided into the comparison evaluation module (CEM) and final module (FM). The CEM uses a parallel prefix tree structure for bitwise comparison. To explore the regularity of the comparator, two operands are applied into 4 bit partitions. The comparison process is divided into five sets, with CEM containing sets 1–4 and FM containing only set 5. This structure serves as a high-level and low-level architecture.The design involves placing sets in four hierarchal prefix orders based on their functionality. Each set's output serves as input for another set, except for set 1, which's outputs are used by sets 2 and 3.

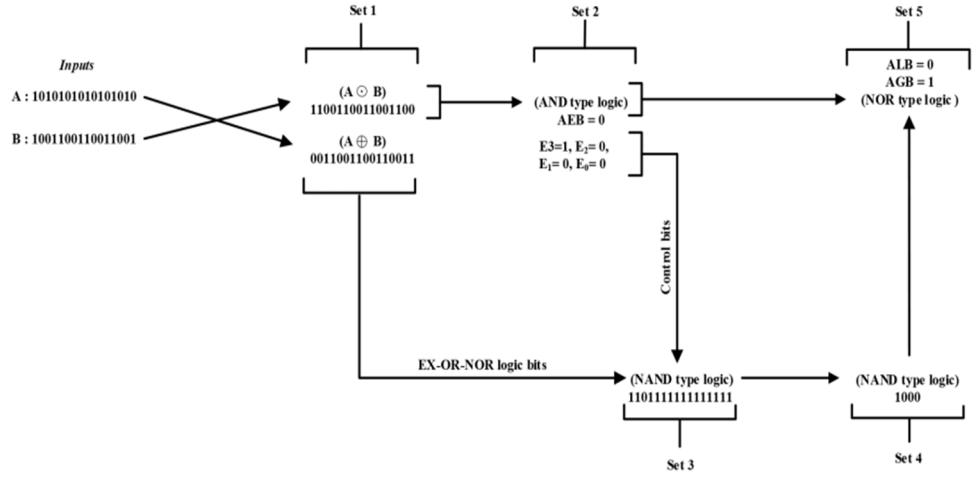


Fig 3.5 : 16 bit comparison using the proposed N-bit digital comparator

The methodology involves 16-bit comparison of two input operands, A=101010101010101010 and B=1001100110011001, using 5T XOR gate. The process is divided into five sets, with set 1 examining equal and unequal bit pairs using bitwise comparison. The outputs are '1100110011001100' and '0011001100110011', indicating equal bit pairs and unequal most significant bit pairs. Set 2 examines equal bit pairs but producesE3 = '1', E2 = '0', E1 = '0', E0 = '0', and AEB = '0' due to unequal most significant bit pairs. Set 4 combines four nibbles from set 3 into 4-bit data as '1000'. The process is illustrated in Figure.Set 5 uses the 4 bit input pattern from set 4 and output bit 'AEB' from set 2 to make the final decision, with outputs AGB='1', ALB='0', and AEB='0', as A is greater than B.

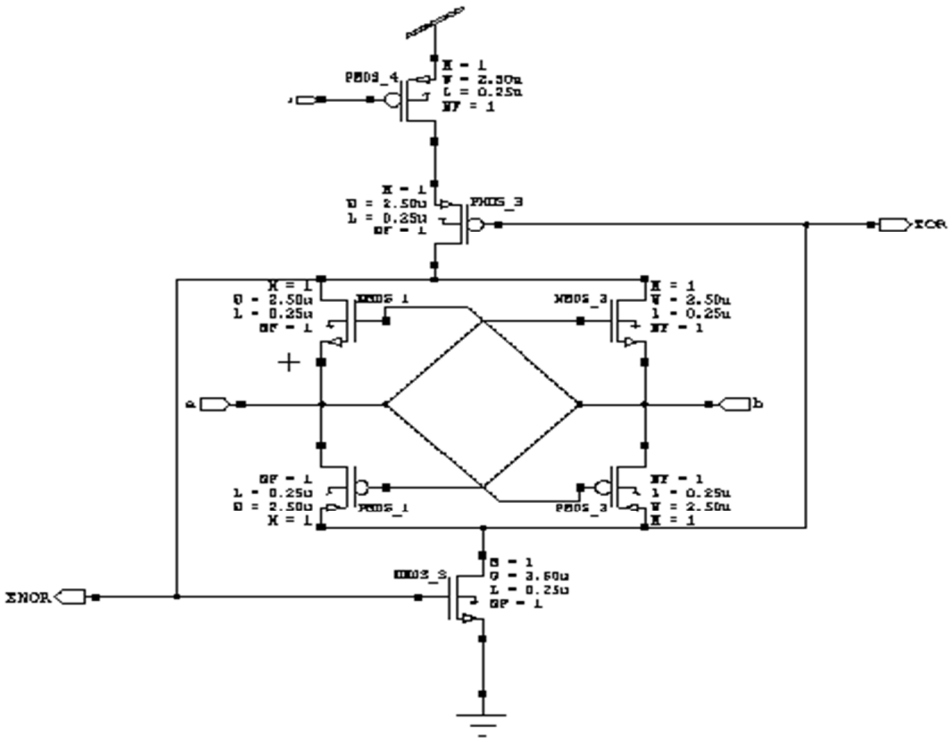


Fig 3.5 : Circuit diagram of 5T XOR gate

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This paper presents a low power hardware efficient comparator using 5T XNOR, an essential module in combinational circuits and comparators. It also uses XNOR and XOR circuits in encryption and arithmetic circuits for low power consumption, making it suitable for VLSI design.The proposed work focuses on setting up a low power area efficient comparator circuit using a 5T XOR gate, consisting of 5 transistors, to achieve maximum output voltage while minimizing parasitic effect. The goal is to maintain a symmetry between power and speed at lower voltage levels and highest output voltage levels.A digital comparator is a hardware that compares two numbers and determines if one number is greater than, less than, or equivalent to the other.

The 5T XOR gate is a simplified version of the traditional XOR gate, featuring five transistors including two NMOS, two PMOS, and an additional NMOS transistor, making it an ideal choice for area-efficient designs.This paper presents a new design for a high-speed, area-efficient N-bit digital comparator. The design is tailored for N-bit digital comparison, achieving speed without compromising area efficiency. The architecture optimizes circuit components and signal propagation, minimizing propagation delays. This design is essential for high-performance digital systems and enables rapid and reliable N-bit comparisons, meeting the growing demand for compact, high-performance comparators.

The proposed XOR gate offers superior power, area, full swing voltage, and excellent driving capability, allowing it to be cascaded to various stages due to its excellent driving capability.

IV. RESULTS

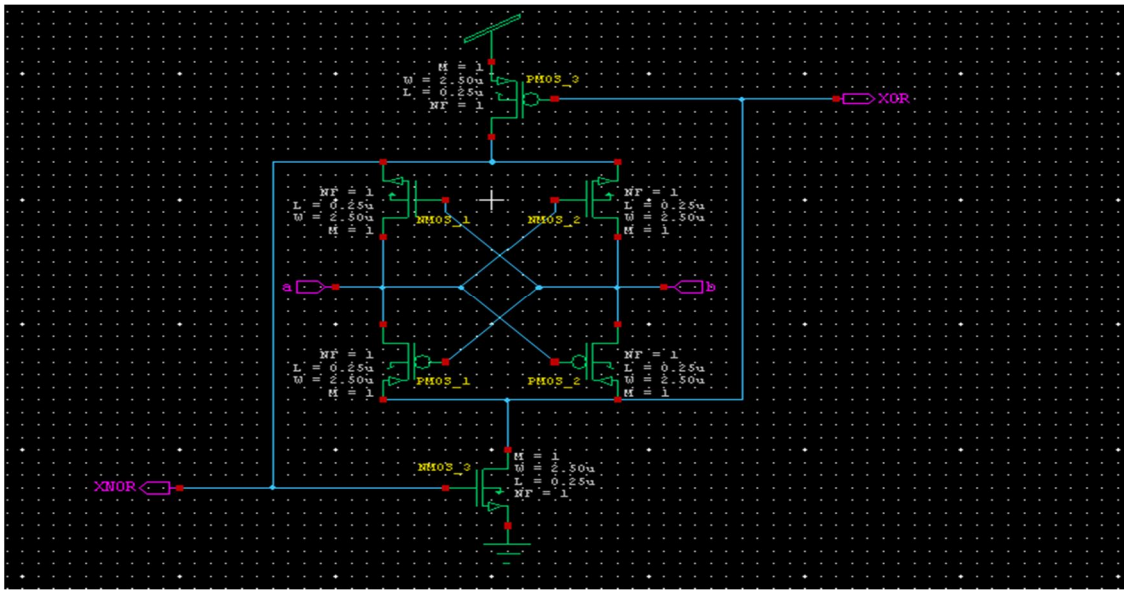


Fig 4.1 : Schematic of 5T XOR Gate

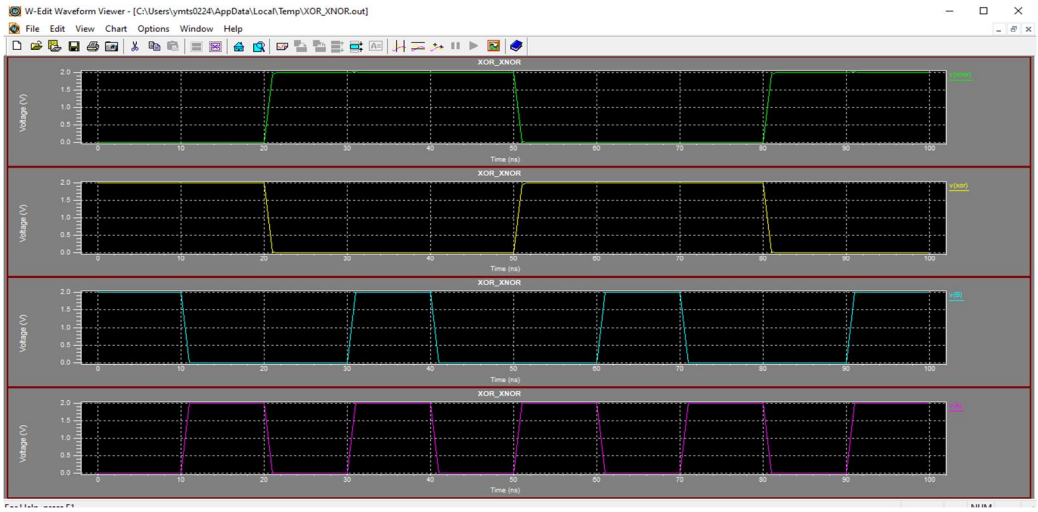


Fig 4.2 : Waveform of Proposed 5T XOR gate

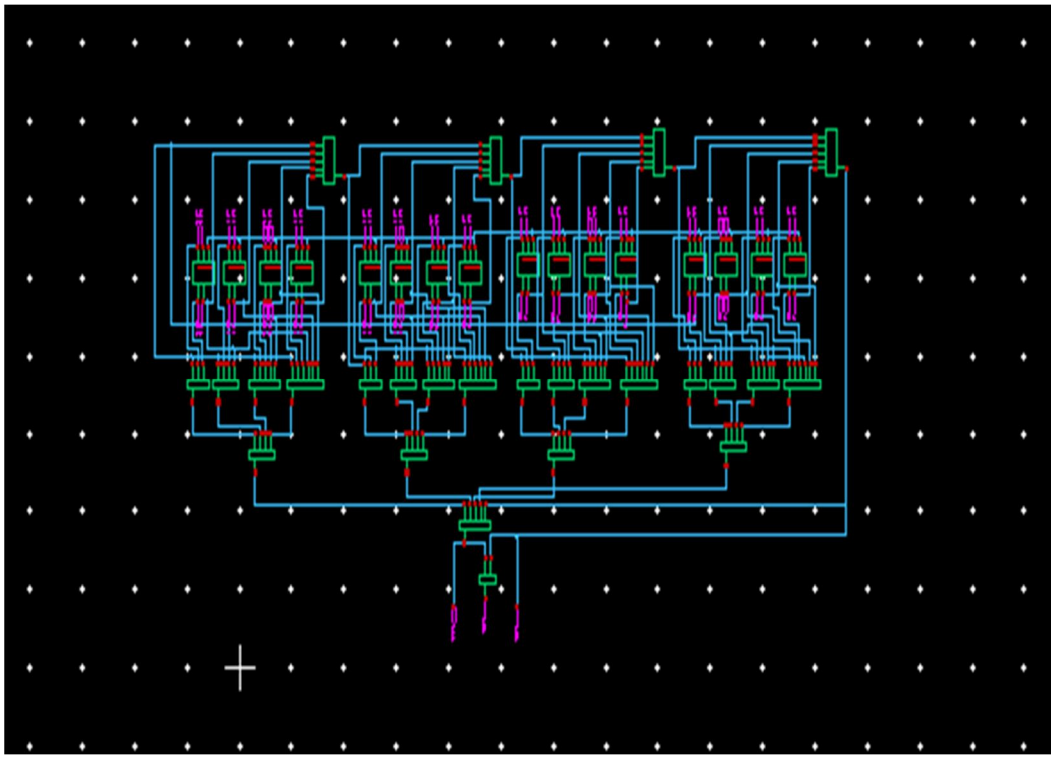


Fig 4.3 : Schematic diagram proposed 16 bit Comparator

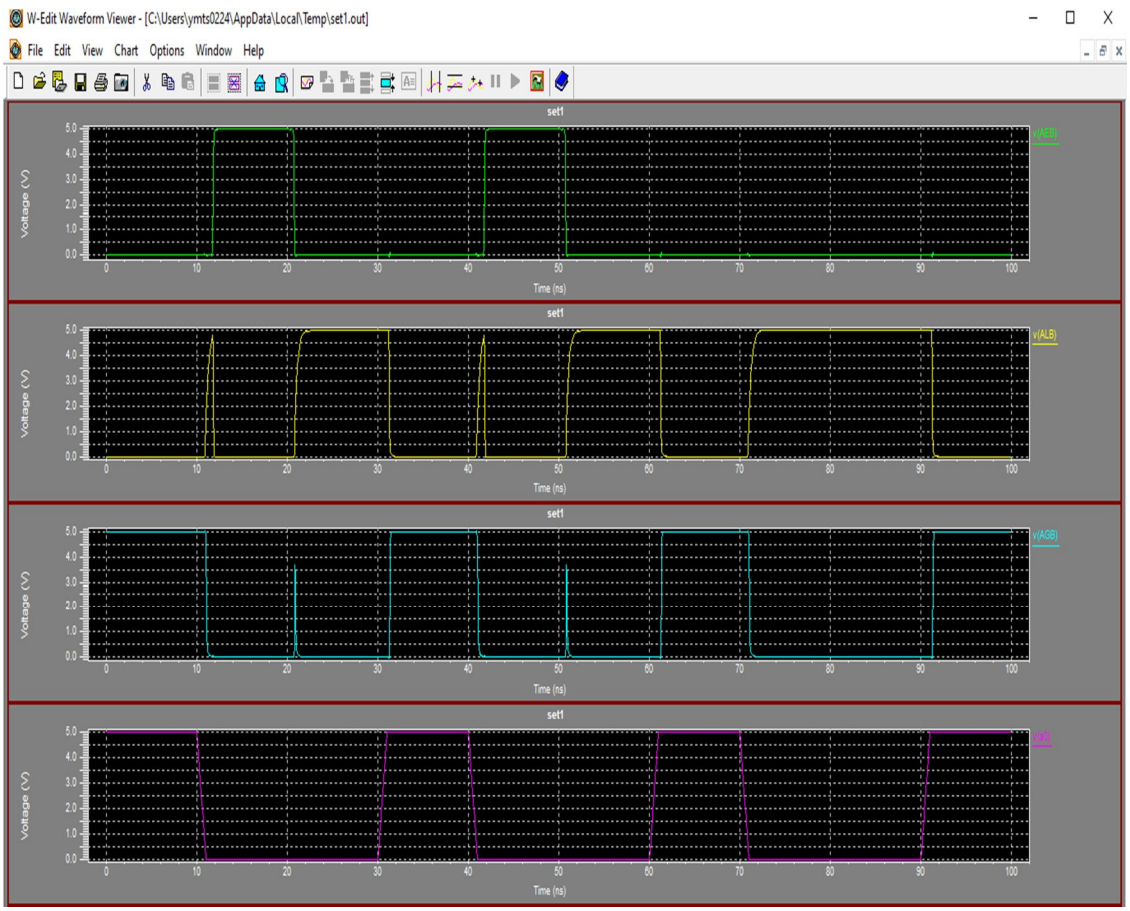


Fig 4.4 : Waveform of Proposed 16bit Comparator

Table 4.1 Power, Delay and Area calculations of the circuits

Name of the circuit	Power(mw)	Delay (ns)	Area (nm)
Proposed 64-bit comparator	4.6	4.2	1318
Existing 64-bit comparator	5.1	4.4	1382
Proposed 24-bit comparator	1.7	1.2	498
Existing 24-bit comparator	1.9	1.3	522
Proposed 16-bit comparator	4.9	0.2	334
Existing 16-bit comparator	6.8	0.3	350

V. CONCLUSION

In conclusion,the proposed scalable comparator uses CEM and FM structures, implementing a parallel prefix tree structure. This structure predicts the comparator's characteristics for arbitrary bit widths. This scalable n-bit digital comparator is a significant advancement in digital circuit design, ensuring adaptability across various applications and seamless integration into complex systems. High efficiency enhances performance and contributes to resource optimization. The comparator is suitable for scientific computations, test circuits, and memory addressing logic.

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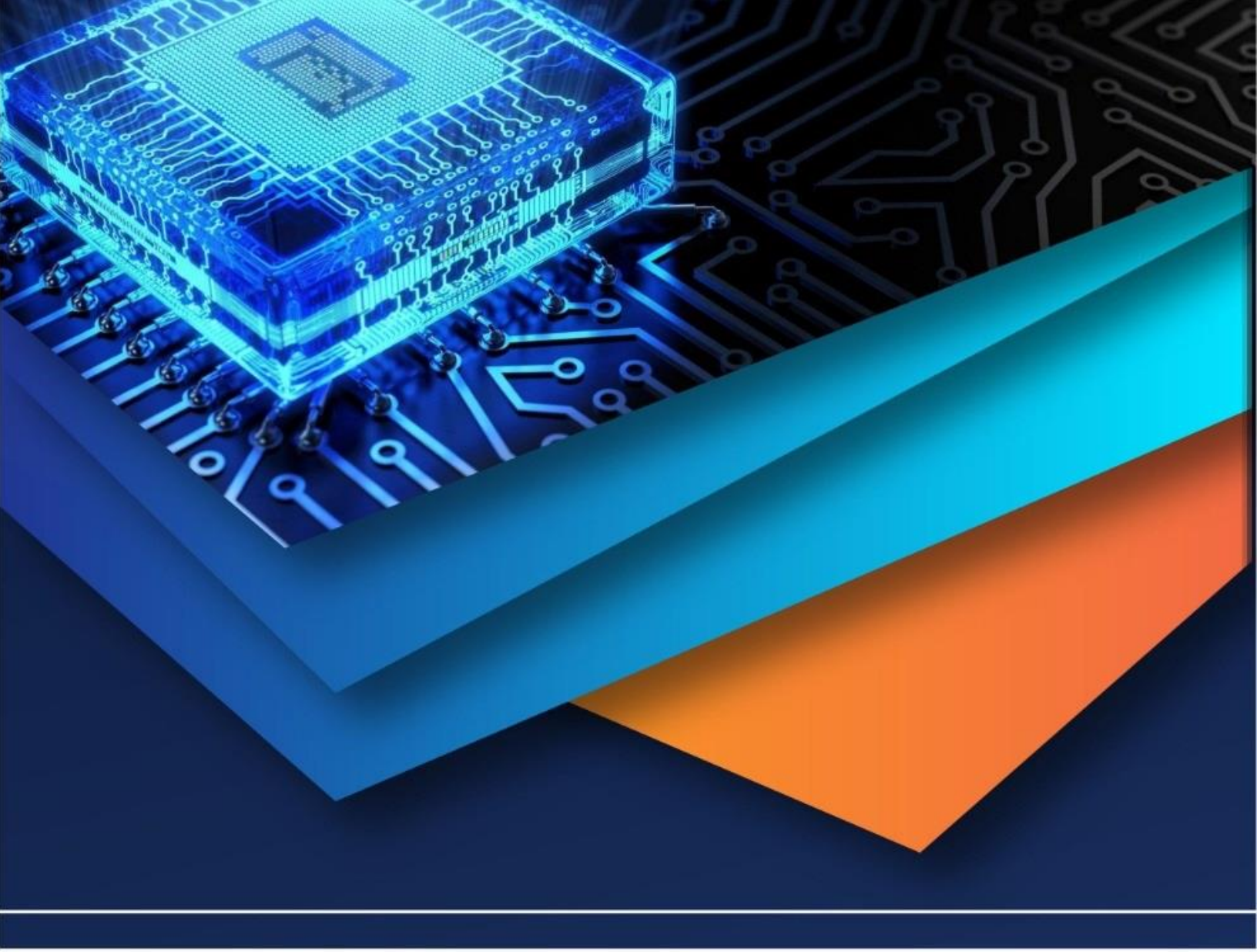
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