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Impact of Miniaturization on the Self-Heating Effect in MOSFET Devices

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Abstract: ***With further scaling of MOSFETs to nanometer sizes, thermal effects have been a major issue affecting device performance and reliability. In this paper, we examine the temperature impacts in scaled MOSFETs, with a focus on self-heating mechanisms, thermal resistance modeling, and their effects on circuit performance. Based on an extensive literature survey and electro-thermal simulations, we examine the interplay among scaling, heat dissipation, and degradation of critical electrical parameters. We offer mathematical models for predicting thermal behavior in nanometer-scale devices and propose possible design considerations for avoiding self-heating.***
Index Terms: MOSFET, Miniaturization, Self-Heating Effect, Thermal Modeling, VLSI, TCAD Simulation, Nanotechnology.

I. INTRODUCTION

The relentless pursuit of greater computational power, energy efficiency, and miniaturization has brought about aggressive scaling of MOSFETs that are the pillar of today's electronic technologies like smartphones, autonomous systems, and edge-AI platforms. With devices trending toward sub-10 nm technology nodes, new issues emerge—most notably thermal management—due to higher power densities and lower physical volumes available for heat dissipation.

At such nanoscale sizes, the classical assumption of good heat spreading no longer holds. Contemporary MOSFET devices contain materials such as high-κ dielectrics and low-k insulators, which have low thermal conductivity, further complicating the dissipation of internally produced heat. Such heat buildup during operation, also known as the self-heating effect (SHE), causes a localized increase in temperature in the device's active region.The effects of SHE are considerable. High junction temperatures have an adverse impact on important electrical characteristics, such as carrier mobility, threshold voltage, and subthreshold swing. With time, thermal stress hastens degradation processes like hot-carrier injection (HCI) and bias temperature instability (BTI), which can shorten the device's operating lifetime. The problem is further exacerbated in sophisticated transistor architectures like FinFETs, Gate-All-Around FETs (GAA-FETs), and Silicon-on-Insulator (SOI) devices in which the heat dissipation routes are drastically restricted due to geometric confinement and insulating layers.It is under such conditions that a through grasp of self-heating and its effect on scaled MOSFETs becomes absolutely crucial. The mechanisms underlying SHE are investigated in this work through a combination of analytical modeling, TCAD-based simulations, and inference from recent literature. Our aim is to bring out how device scaling has a profound impact on the thermal landscape and suggest strategies—spanning material choices to structural optimization—that can overcome thermal constraints in near-nanoscale MOSFETs.

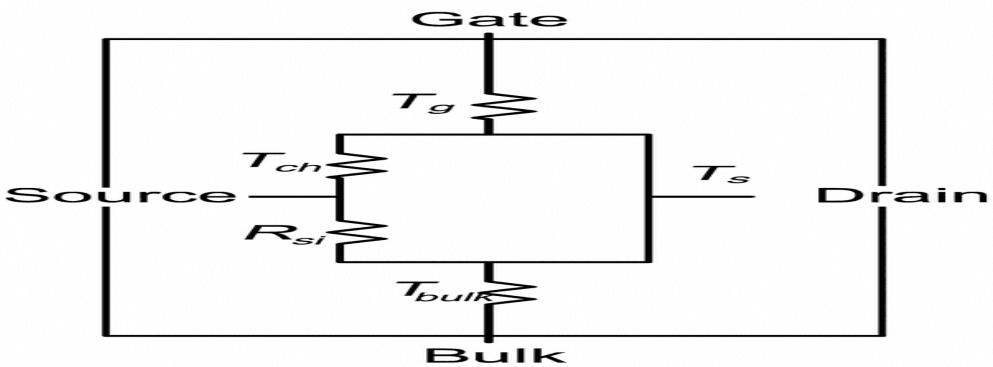

Fig. 1. Equivalent thermal network in GAA SNWT

II. PROBLEM STATEMENT

The ongoing downscaling of MOSFET sizes to sub-10 nm technology nodes, although providing greater integration density and faster switching rates, presents substantial thermal management issues. Among these, a serious issue is the heat concentration within the active channel of the transistor, resulting in the self-heating effect (SHE). With physical sizes decreasing, heat dissipation area reduces, and thermal resistance grows due to smaller heat flow paths. This leads to significant temperature increase even at moderate power levels.

Traditional circuit models typically adopt the assumption of uniform temperature distribution over the device, which becomes more and more inaccurate at the nanoscale. With emerging structures like FinFETs, GAA-FETs, and SOI-based MOSFETs, material-induced thermal isolation due to structures such as buried oxide (BOX) adds to the problem of local heating.

Temperature increase in the channel impacts major electrical characteristics, such as mobility, threshold voltage, leakage current, and subthreshold swing—directly impacting device performance and reliability. Therefore, it becomes crucial to comprehend the evolution of SHE with scaling and also how it may be modeled correctly and controlled practically.

This study is aimed at characterizing the role of miniaturization in SHE for future MOSFET architectures and toward developing models and techniques to mitigate next-generation transistor thermal challenges.

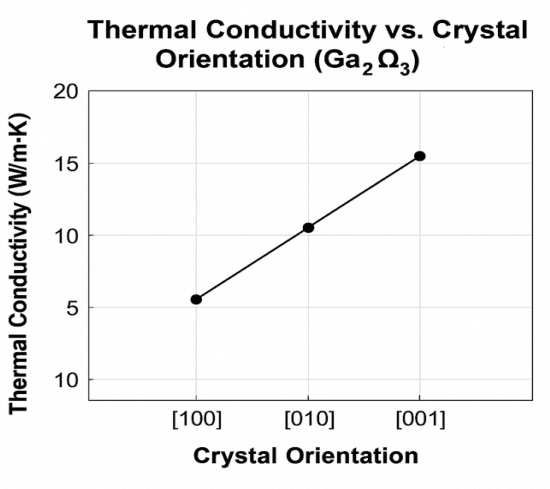

Fig 2: Impact of self-heating on device performance, showing thermal-induced degradation under varying bias conditions

III. OBJECTIVES

The overall objective of this research is to explore the influence of device miniaturization on the self-heating of MOSFETs. This encompasses a detailed examination of the physical phenomena, analytical modeling, and real-world implications of SHE in current and future nanoscale devices. For this, this research is guided by the following specific objectives:

1) To introduce the physics of self-heating in MOSFETs.
2) To theoretically determine the thermal resistance and power dissipation parameters.
3) To model temperature-dependent degradation of significant electrical parameters.
4) For comparison of analytical models with experimental results and TCAD simulations.
5) To recommend mitigation strategies at material, device, and circuit levels.

Through these objectives, the research intends to provide an integrated framework for mitigating the thermal problem generated by miniaturized MOSFETs to provide enhanced performance, reliability, and energy efficiency in future electronics.

IV. METHODOLOGY

In order to study in depth the SHE in miniaturized MOSFETs, this work adopts a multi-aspect combined methodology that combines analytical modeling, literature survey, and numerical simulations. It attempts to capture device-level implications and physical mechanisms of localized heating with additional reduction in transistor geometries.

The strategy begins with an overview that embraces academic journals, conference papers, and preprints on thermal response in nanoscale MOSFET devices. The overview helps to point to emerging trends, deficits in the existing models, and open areas of study—particularly in high-substrate or non-conventional-geometry devices.

To quantify the thermal dynamics within MOSFET structures, several analytical models rooted in thermodynamics and solid-state physics are employed. Key equations include:

- Fourier's Law for one-dimensional heat conduction:

$$\Delta T = P \times R_{th}$$

where ΔT is the temperature rise, P is power dissipation, and R_{th} is thermal resistance.

- Thermal Resistance:

$$R_{th} = \frac{L}{k \cdot A}$$

where L is the heat flow path length, k is thermal conductivity, and A is the cross-sectional area.

- Mobility Degradation due to elevated temperature:

$$\mu(T) = \mu_0 \left(\frac{T_0}{T}\right)^m$$

where μ_0 is the mobility at reference temperature T_0, and m is an empirical constant (typically ≈ 1.5 for silicon).

- Saturation Velocity Model and the Dual-Phase-Lag Heat Equation are also incorporated to model transient and nonlinear effects.

These models collectively facilitate the evaluation of power dissipation, temperature rise, and the temperature-dependent variation of key electrical parameters.

For the purpose of ensuring the outcome achieved by analysis, TCAD simulations are done on software-based computers such as Silvaco Atlas and Synopsys Sentaurus. Various device structures such as bulk, SOI, FinFET, and GAA MOSFETs are simulated by modifying parameters such as gate length, oxide thickness, and doping profiles in a sequential manner.

Thermal boundary conditions and heat source models are also included to provide the self-heating effect during realistic operating conditions. Material parameters are made temperature-dependent, and thermal feedback models are enabled to track lattice temperature oscillations. Devices are operated under various conditions to monitor alterations in threshold voltage, carrier conduction, and drain current features as functions of increasing temperature.

Simulation results are subsequently compared to available experimental data from the literature to ensure consistency and validate model accuracy. The comparative methodology allows for the determination of device architectures most vulnerable to SHE and assessment of design-level mitigation measures, including the utilization of thermally conductive substrates or altered geometries.

V. RESULTS AND ANALYSIS

The results of analytical modeling and TCAD simulations indicate a drastic increase in the SHE with aggressive device scaling. Temperature profiles obtained from simulations indicate that as gate lengths decrease below 20 nm, local temperature rise in the channel becomes increasingly important, especially in SOI and GAA-based devices.

A. Simulation Findings

In simulations of SOI and FinFET structures with gate lengths around 10 nm, the peak lattice temperature was observed to increase by 10–50 K under moderate biasing conditions. This increase correlates strongly with both the power density and the thermal resistance of the device. Structures with thin buried oxides (BOX) showed even higher thermal confinement, suggesting that oxide engineering plays a key role in thermal performance.

B. Analytical Correlation

From the thermal resistance model $R_{th} - \frac{L}{kA}$ it was confirmed that narrower and longer channels exhibit higher resistance to heat flow. Consequently, even small increases in power dissipation led to elevated operating temperatures. The mobility degradation model further revealed that for every 10 K rise, the carrier mobility decreases by approximately 4–10%, depending on doping levels and substrate material.

C. Literature Comparison

The results are in agreement with recent literature. For example:

1) Zhang et al. reported a 30 K temperature rise in 40 nm SOI MOSFETs using on-chip thermometry.

2) Ghibaudo et al. demonstrated that temperature increase in FDSOI devices exhibits non-linear behaviour with increasing power dissipation.
3) 't Hart et al. demonstrated that SHE becomes increasingly important under cryogenic conditions, where silicon's thermal conductivity decreases considerably.

D. Architecture-Specific Trends

1) Bulk CMOS has improved thermal dissipation through direct substrate contact, leading to reduced junction temperatures.
2) SOI devices are subjected to thermal isolation due to the BOX layer, resulting in increased peak temperatures.
3) FinFETs and GAA-FETs exhibit steep thermal gradients as a result of dense geometry and constrained heat spreading channels, which render them susceptible to thermal degradation.

SOME GRAPHICAL RESULTS

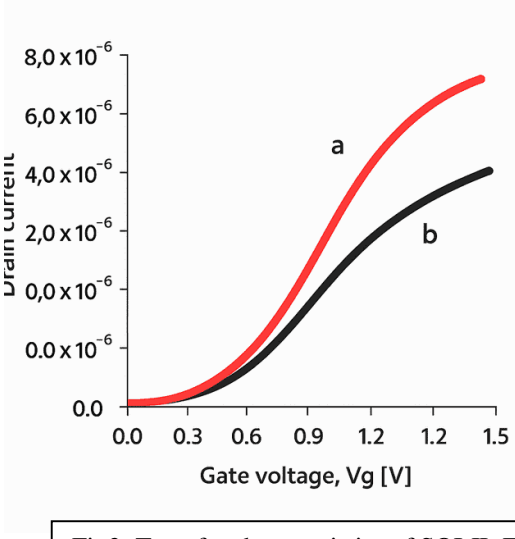

Fig3: Transfer characteristics of SOI JL FinFET (rectangular cross-section) showing comparison without (a) and with (b) self-heating effect.

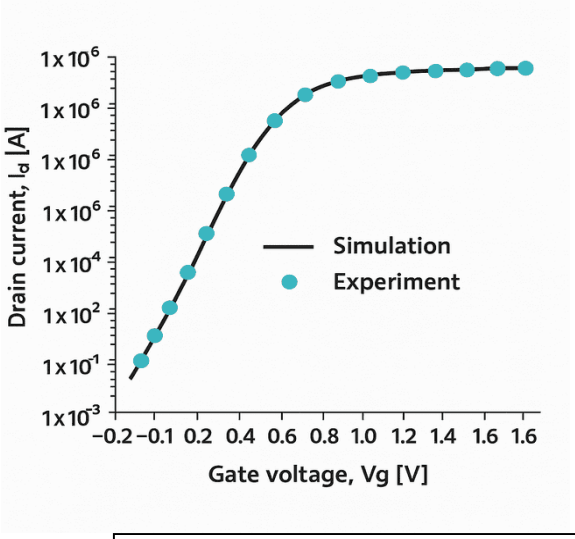

Fig4: Comparison of Id–Vg characteristics between simulated and experimental MOSFET devices.

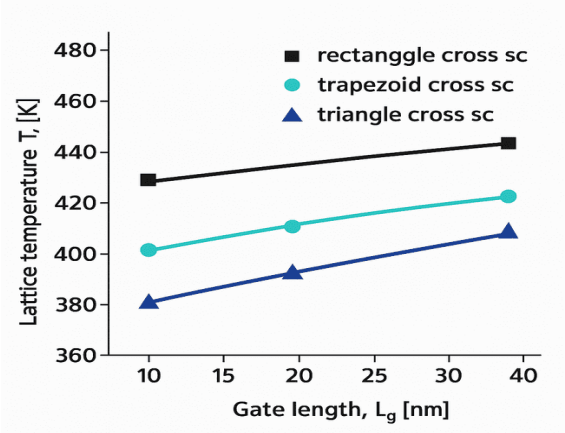

Fig 5: Variation of lattice temperature with gate length for transistors having different cross-sectional geometries (TBOX = 146 nm)

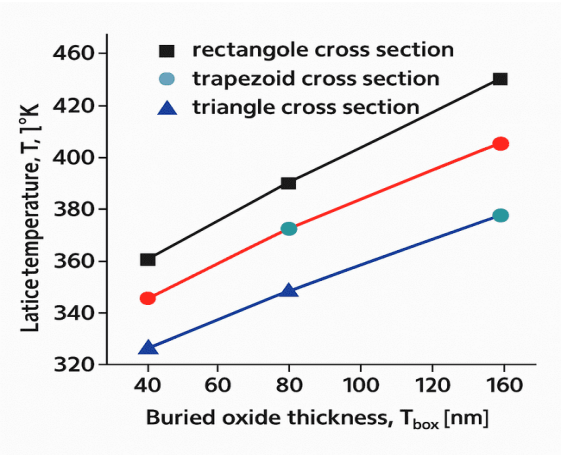

Fig 6: Lattice temperature variation with buried oxide thickness for a transistor with gate length Lg = 11 nm.

VI. DISCUSSION

The results from simulations and analytical models both highlight the key role played by self-heating in nanometer-scale MOSFETs. As further scaling of devices occurs, it is clear that thermal characteristics must be incorporated into design and simulation procedures—not as an addendum, but as a fundamental design parameter.

A. Geometry and Material Impact

The degree of self-heating relies significantly on device geometry and material. Devices with shorter gate lengths and cross-sectional areas have greater thermal resistance, which inhibits efficient heat dissipation. Moreover, materials such as high-κ gate dielectric and BOX layer in SOI technology, although very appropriate for electrostatic control, are thermal barriers that inhibit vertical heat conduction.

To offset this, incorporating materials with increased intrinsic thermal conductivity, like silicon carbide (SiC) or diamond-based substrates, would greatly enhance thermal dissipation. Altering the gate stack and spacer materials in FinFETs and GAA-FETs may also provide thermal relief without any sacrifice to performance.

B. Architectural Considerations

Our findings indicate that even though bulk MOSFETs are still better regarding thermal conduction, electrostatic control is difficult for them in advanced nodes. Meanwhile, SOI, FinFET, and GAA-FET architectures, while great at avoiding short-channel effects, are hindered by localized heating and heat-spreading paths with limited space.

Design optimizations such as:

- Higher fin pitch in FinFETs,
- Thermal vias in GAA-FETs, or
- Slimmer BOX layers in SOI devices can be implemented as effective mitigation measures. These have to be optimized to maintain electrical performance with enhanced thermal dissipation.

C. System-Level and Circuit-Level Implications

Apart from device-level changes, circuit designers must incorporate thermal-aware design techniques. Techniques such as: Dynamic voltage and frequency scaling (DVFS),Thermal-aware placement and routing, and On-chip thermal sensing

are available to manage heat in real time. Software-based techniques such as load balancing, thermal throttling, and activity migration can be implemented at the SoC level and incorporated into control systems for predictive thermal management. Moreover, the increasing trend of 3D IC stacking brings additional thermal challenges. Lacking adequate heat evacuation mechanisms, vertical stacking causes thermal hotspots. Breakthrough solutions such as microfluidic cooling, embedded heat sinks, or thermoelectric coolers (TECs) could be used to preserve temperature uniformity in such structures.

D. Modeling Challenges and Future Directions

Existing compact models tend to assume isothermal conditions, which are no longer valid for sub-10 nm devices. There is an increasing demand for the inclusion of temperature-dependent parameters in SPICE models and Verilog-A device definitions to properly represent SHE effects.

Going forward, the blending of machine learning algorithms with outputs from TCAD might be able to predict the thermal behavior dynamically. Hybrid platforms such as these would allow for designers to optimize and simulate not just electrical but also thermal resistance of devices, which is an absolute requirement in next-generation electronics.

VII. CONCLUSION

This study provides a comprehensive analysis of the self-heating effect (SHE) in miniaturized MOSFET devices, highlighting how device scaling and advanced architectures have amplified thermal challenges. Through analytical modeling and TCAD simulations, we have demonstrated that localized heating significantly impacts key device metrics—such as carrier mobility, threshold voltage, and subthreshold swing—thereby affecting both performance and long-term reliability.

Our findings reveal that as gate lengths shrink and integration densities rise, the thermal resistance of transistors increases, especially in architectures like SOI, FinFETs, and GAA-FETs. These structures, while beneficial for electrostatic control, suffer from limited heat dissipation pathways.

The results emphasize that material selection, structural design, and architectural choices must collectively address thermal constraints to ensure stable device operation.

To mitigate the adverse effects of self-heating, we have discussed strategies at multiple levels:

1) Material level: Introducing substrates with superior thermal conductivity.

2) Device level: Optimizing fin geometry, oxide thickness, and incorporating thermal vias.

3) Circuit and system level: Employing dynamic thermal management, layout optimization, and real-time temperature monitoring.

Furthermore, the study recommends the evolution of compact models to include temperature-dependent parameters, ensuring accurate prediction of device behaviour under realistic operating conditions. Future research may also explore the integration of machine learning with electrothermal simulations for predictive thermal modeling and smarter thermal-aware design tools.

As technology nodes continue to shrink and performance demands grow, addressing self-heating will be crucial to sustaining reliability, efficiency, and scalability in the next generation of semiconductor devices.

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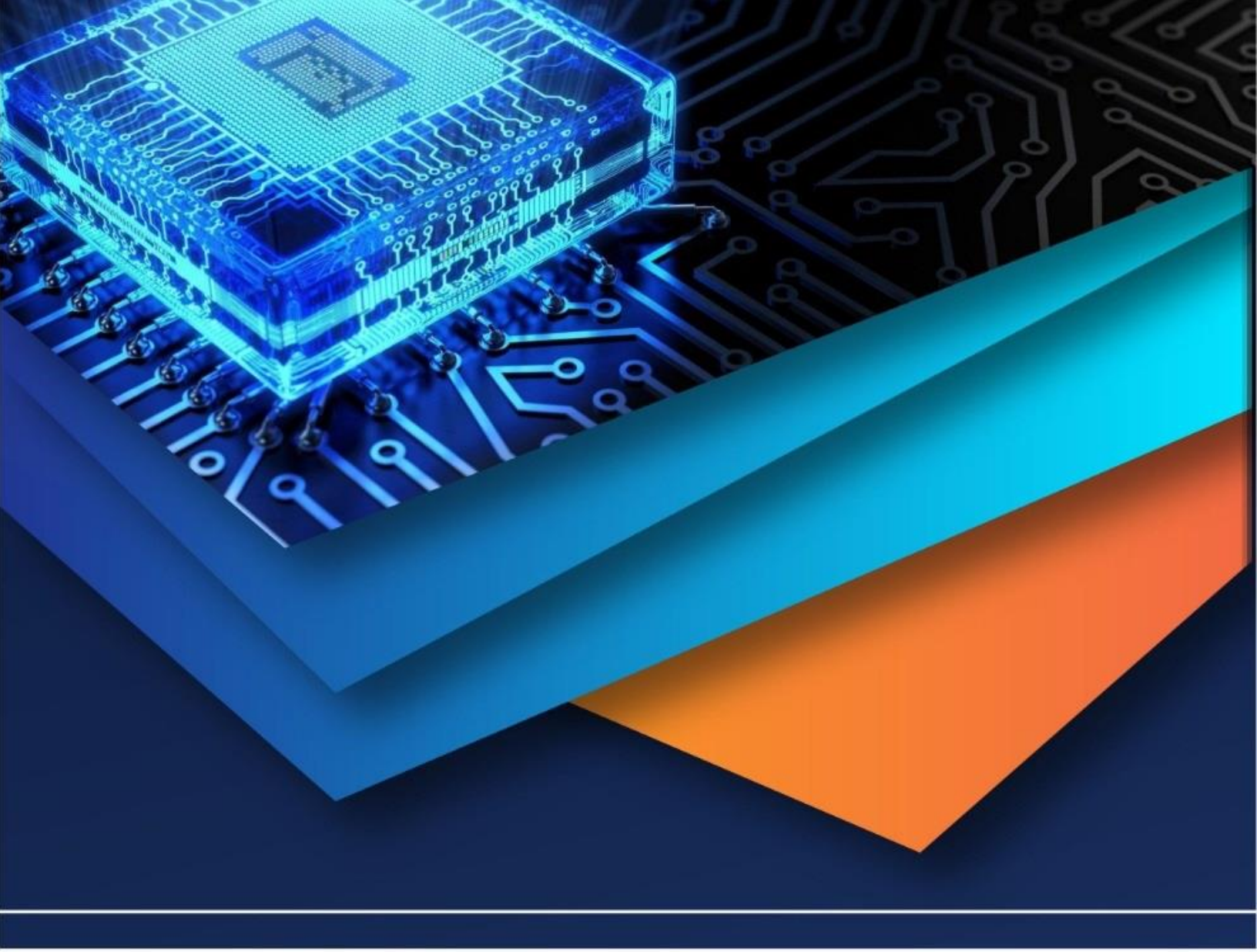

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