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Implementation of 1-bit Full Adder Circuit Using Pass Transistor Logic

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Abstract: ***In this work, we have implemented 1-bit Full Adder Circuit using Pass Transistor Logic. Pass Transistor Logic is used for high-speed technology and is easy to build the basic gate structures. The developed circuit is an extension of pass transistor logic Ex-or gate. The 1-bit Full Adder Circuit has been performed and obtained I-V characteristics and power for sum and carry were calculated. The effect of scaling on the overall performance is also analysed through the performance evaluation of 1-bit full adder circuit. Simulation results have been performed on LT Spice tool simulator at 1.8v single ended supply voltage and simulations are carried out to indicate the functionality of the proposed full adder circuit compared with conventional design to verify the effectiveness and it shows the circuit has low power dissipation at high speeds.***
Keywords: Full Adder Circuit, Pass Transistor Logic, Ex-or gate, and LT Spice

I. INTRODUCTION

A Full Adder is a digital circuit that performs addition. Full adders are implemented with logic gates in hardware. A full adder adds three one-bit binary numbers, two operands and a carry bit. The adder outputs two numbers, a sum and a carry bit. The term is contrasted with a half adder, which adds two binary digits. A full adder takes two binary numbers plus a carry or overflow bit. The output is a sum and another carry bit. Full adders are made from XOR, AND and OR gates in hardware. Full adders are commonly connected to each other to add bits to an arbitrary length of bits, such as 32 or 64 bits. A full adder is effectively two half adders, an XOR and an AND gate, connected by an OR gate.

Full Adder is the adder that adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. Full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another. We use a full adder because when a carry-in bit is available, another 1-bit adder must be used since a 1-bit half-adder does not take a carry-in bit. A 1-bit full adder adds three operands and generates 2-bit results. Fig. 1 shows the block diagram of Full Adder Circuit.

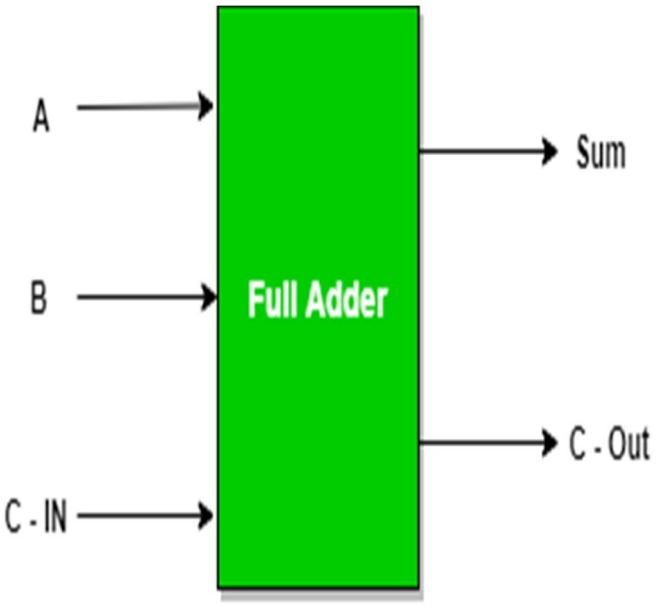

Fig. 1 Block diagram of Full Adder Circuit

A. Full Adder Truth Table

TABLE 1

Inputs			Outputs	
A	B	C-IN	SUM	C-OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1 represents the truth table of the full adder circuit to verify the simulation results functionally.

1) Logical Expression for SUM:

$= \overline{A}\,\overline{B}\,C\_IN + \overline{A}\,B\,\overline{C\_IN} + A\overline{B}\,\overline{C\_IN} + ABC\_IN$

$= C\_IN\,(\overline{A}\,\overline{B} + A\,B) + \overline{C\_IN}\,(\overline{A}\,B + A\,\overline{B})$

$= C\_IN\,\overline{(A \oplus B)} + \overline{C\_IN}\,(A \oplus B)$

$= A \oplus B \oplus C\_IN$

$= (1,2,4,7)$

2) Logical Expression for C-OUT:

$= \overline{A}BC\_IN + A\overline{B}\,C\_IN + AB\overline{C\_IN} + ABC\_IN$

$= AB + BC\_IN + AC\_IN$

$= (3,5,6,7)$

3) *Another form in which C-OUT can be implemented:*

$= AB + BC\_IN(A + \overline{A}) + AC\_IN$

$= AB\,C\_IN + AB + AC\_IN + \overline{A}BC\_IN$

$= AB\,(1 + C\_IN) + AC\_IN + \overline{A}BC\_IN$

$= AB + AC\_IN + \overline{A}BC\_IN$

$= AB + AC\_IN(B + \overline{B}) + \overline{A}BC\_IN$

$= AB + ABC\_IN + \overline{A}BC\_IN + A\overline{B}\,C\_IN$

$= AB\,(1 + C\_IN) + \overline{A}BC\_IN + A\overline{B}\,C\_IN$

$= AB + \overline{A}BC\_IN + A\overline{B}\,C\_IN$

$= AB + C\_IN(\overline{A}B + A\overline{B})$

Therefore $COUT = AB + C\_IN(A \oplus B)$

B. Advantages of Adders

The advantages include:

1) Half Adder's design is very simple. It is the basic building block for single bit addition.
2) Just with an inverter gate, Half-Adders can be converted to Half Subtractors.
3) Full swing output can be obtained with Full-Adders.
4) Power consumption is low.
5) Speed is high.
6) Robustness to supply voltage scaling.

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C. Disadvantages of Adders

The disadvantages are:

1) It does not incorporate (or take care of) previous carry for addition.
2) Hence it is not suitable for cascading for Multi-bit addition.
3) To get rid of this problem, Full Adders are required which add three 1 bit.
4) When Full Adders are used in a chain structure such as a Ripple Adder, the output drive capability is reduced.

D. Applications of Adder

The applications of Adders are:

1) A Full Adder's circuit can be used as a part of many other larger circuits like Ripple Carry Adder, which adds n-bits simultaneously.
2) The dedicated multiplication circuit uses Full Adder's circuit to perform Carryout Multiplication.
3) Full Adders are used in ALU- Arithmetic Logic Unit.
4) In order to generate memory addresses inside a computer and to make the Program Counter point to next instruction, the ALU makes use of Full Adders.
5) Full-Adders are a part of Graphics Processing Unit for graphics related applications.

II. LITERATURE SURVEY

In paper, A 4-bit CMOS Full Adder of 1-bit Hybrid 13T Adder with A New SUM Circuit in [1], designed by tanner EDA tools on 250nm and calculated power consumption. However there is a need to decrease both the technology node and power reduction. In another work, A Novel Approach to Design Low Power and High-Speed Self-Repairing Full Adder Circuit in [2], as the number of transistors have increased, there is a need to decrease the area.

A Novel Design and Implementation of Multi-Valued Logic Arithmetic Full Adder circuit using CNTFET in [3] observed disturbances in output and the output uses 3 levels other than logic 0 level and logic 1 level. Area-Efficient High-Speed Hybrid 1-bit Full Adder Circuit Using Modified XNOR Gate in [4], there is a need for a reduction in power.

In another work, Comparative Study of Full Adder Circuit with 32nm MOSFET, DG-FinFET, and CNTFET in [5] observed some glitches in the output. Compressor Using Full Swing XOR Logic Gate in [6], we have observed some glitches in the output.

In Delay Analysis of Half Subtractor using CMOS and Pass Transistor Logic in [7], as the number of transistors increase, there is a need to decrease the area. In the Design of high-speed and low-power hybrid full adder circuit in [8] observed some glitches in the output.

In Design of 16T Full Adder Circuit Using 6T XNOR Gates in [9], observed some glitches in the output. In Full Adder Circuit Design Using Lateral Gate-All-Around (LGAA) FETs Based on BSIM-CMG Model in [10], there is a need to decrease both the technology node and power reduction.

Implementation of a Full Adder Circuit with New Full Swing Ex-OR/Ex-NOR Gate in [11], number of transistors have increased and there is a need to decrease the area. Low Power and Temperature compatible FinFET-based Full Adder circuit with optimized Area in [12], observed some glitches in the output. Low Power High-Speed 1-bit Full Adder Circuit Design in DSM Technology in [13], as the number of transistors increases, there is a need to decrease the area. However, there is a need to decrease both the technology node and power reduction.

Low-Leakage Full Adder Circuit Using Current Comparison Based Domino Logic in [14], observed disturbances in output and the output uses 3 levels other than logic 0 level and logic 1 level. 6 Transistor Full Adder Circuit Using Pass Transistor Logic in [15], the number of transistors were increased for carry and there is a need to decrease the area. However, there is a need to decrease both the technology node and power reduction

Performance Enhancement of a Hybrid 1-bit Full Adder Circuit in [16], the number of transistors have increased and there is a need to decrease the area. However, there is a need to decrease both the technology node and power reduction. In Strong Indication Full-Adder Circuit for NULL Convention Logic Automation Flows in [17], the number of transistors has increased and there is a need to decrease the area. However, there is a need to decrease both the technology node and power reduction.

Hence there is a need to design and implement a Full Adder Circuit for a smaller number of transistors, voltages, currents, and power.

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III. IMPLEMENTATION

A. Pass Transistor Logic

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits.
It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit instead of switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails (resembling an open collector scheme), so logic voltage levels in a sequential chain do not decrease. Simulation of circuits may be required to ensure adequate performance.

B. Applications

Pass transistor logic often uses fewer transistors, runs faster, and requires less power than the same function implemented with the same transistors in fully complementary CMOS logic. XOR has the worst-case Karnaugh map if implemented from simple gates; it requires more transistors than any other function. The designers of the Z80 and many other chips saved a few transistors by implementing the XOR using pass-transistor logic rather than simple gates.

C. Basic Principles Of Pass Transistor Circuits

The pass transistor is driven by a periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance C_x, depending on the input signal V_{in}. Thus there is two possible operations, when the clock signal is active (CK = 1) are the logic "1" transfer (charging up the capacitance C_x to a logic-high level) and the logic "0" transfer (charging down the capacitance C_x to a logic-low level). In either case, the output of the depletion load nMOS inverter obviously assumes a logic-low or a logic-high level, depending upon the voltage V_x.

D. Complementary Pass Transistor Logic

Some authors use the term "complementary pass transistor logic" to indicate a style of implementing logic gates that uses transmission gates composed of both nMOS and pMOS pass transistors.
Other authors use the term "complementary pass transistor logic" (CPL) to indicate a style of implementing logic gates where each gate consists of a nMOS-only pass transistor network, followed by a CMOS output inverter.
Other authors use the term "complementary pass transistor logic" (CPL) to indicate a style of implementing logic gates using dual-rail encoding. Every CPL gate has two output wires, both the positive signal and the complementary signal, eliminating the need for inverters.
Complementary pass transistor logic or "Differential pass transistor logic" refers to a logic family which is designed for certain advantage. It is common to use this logic family for multiplexers and latches. CPL uses series transistors to select between possible inverted output values of the logic, the output of which drives an inverter. The CMOS transmission gates consist of nMOS and pMOS transistor connected in parallel.

Other forms

Static and dynamic types of pass transistor logic exist, with differing properties with respect to speed, power and low-voltage operation.
As the integrated circuit supply voltages decrease, the disadvantages of pass transistor logic become more significant; the threshold voltage of transistors becomes large compared to the supply voltage, severely limiting the number of sequential stages. Because complementary inputs are often required to control pass transistors, additional logic stages are required.

IV. RESULTS

The circuit is implemented using pass transistor logic and with the help of the logic first constructed the Ex-or gate circuit. And observed the output without any glitches. Tested by applying 1.8v and 2v voltages and obtained simulations are verified through truth table.

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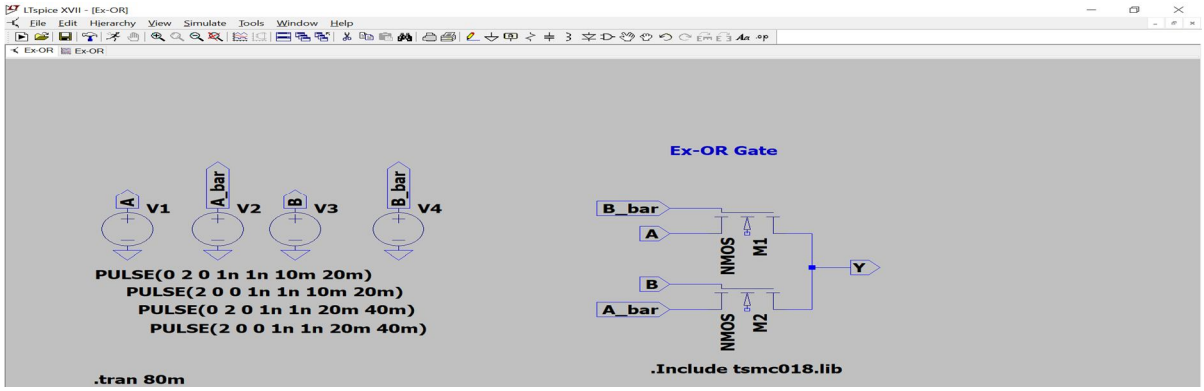

Fig. 2 Ex-or gate circuit diagram using Pass Transistor Logic

Fig.2 represents the circuit diagram of the Ex-or gate with pass transistor logic with all the inputs and outputs applied in LT Spice tools.

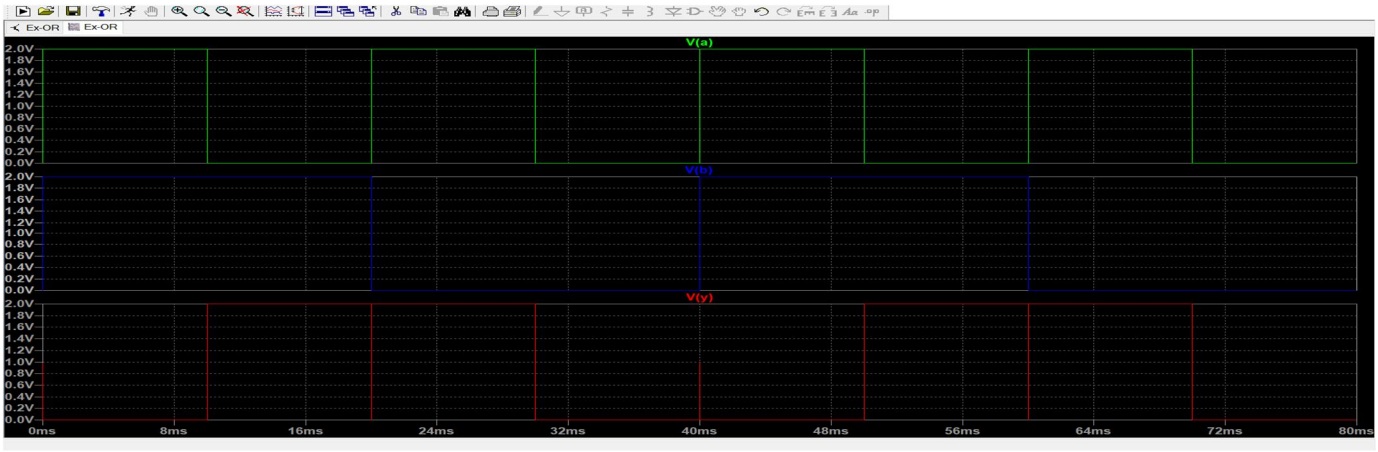

Fig. 3 Ex-or gate output

The Results obtained from the Ex-or gate using Pass Transistor Logic and is observed and verified with the truth table and is shown in Fig. 3.

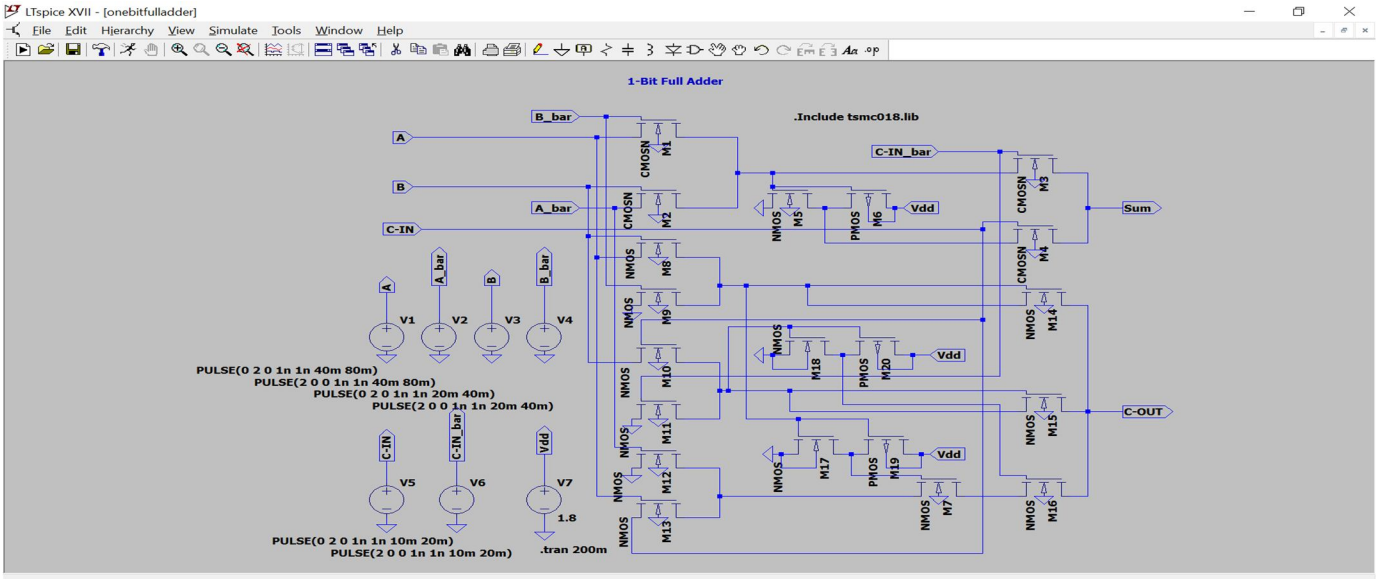

Fig. 4 Proposed One-bit Full Adder Circuit

Fig. 4 represents the proposed circuit diagram of Implemented one bit Full Adder Circuit with Pass Transistor Logic with all the inputs and outputs applied in LT Spice tools.

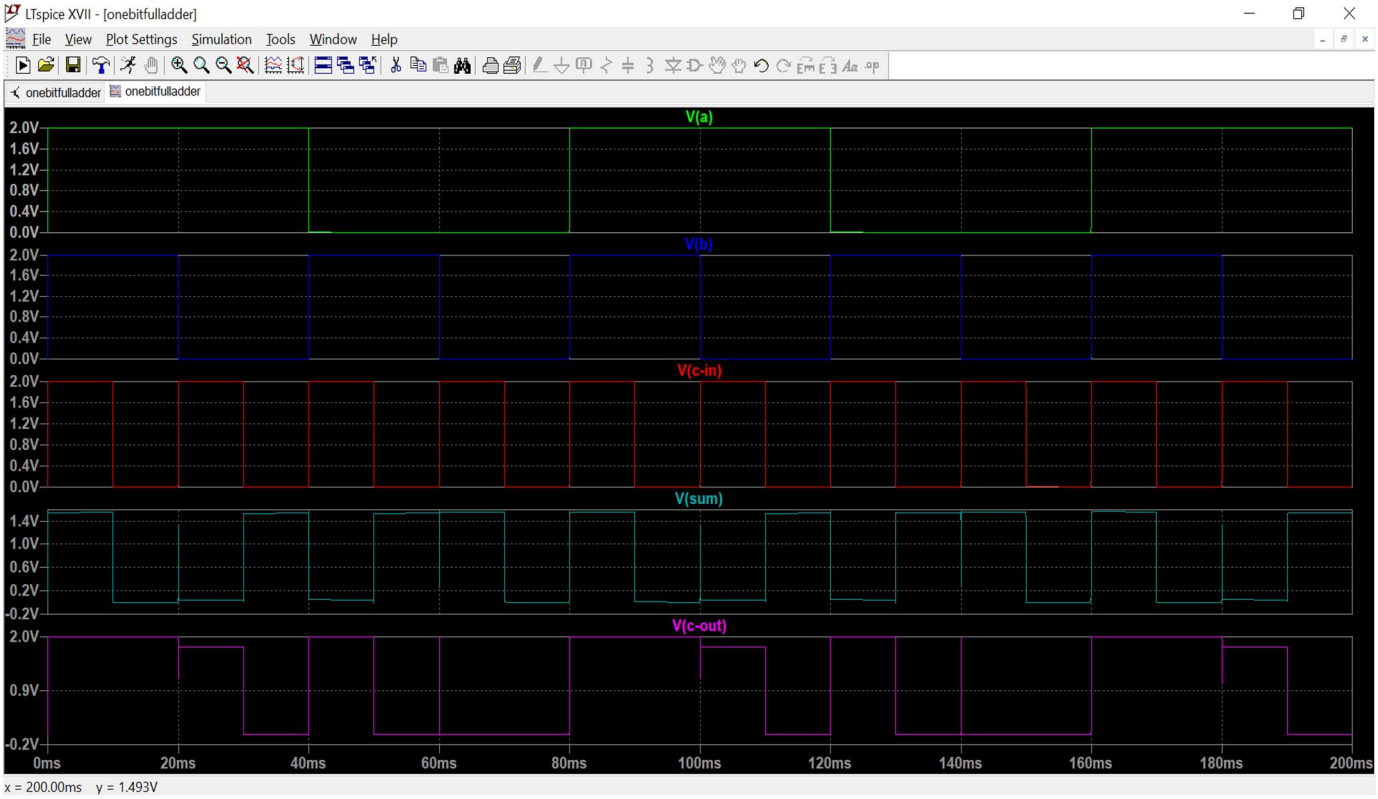

Fig. 5 One-bit Full Adder Outputs

Fig. 5 shows the obtained results from the Full Adder circuit using pass transistor logic is observed and verified with the truth table.

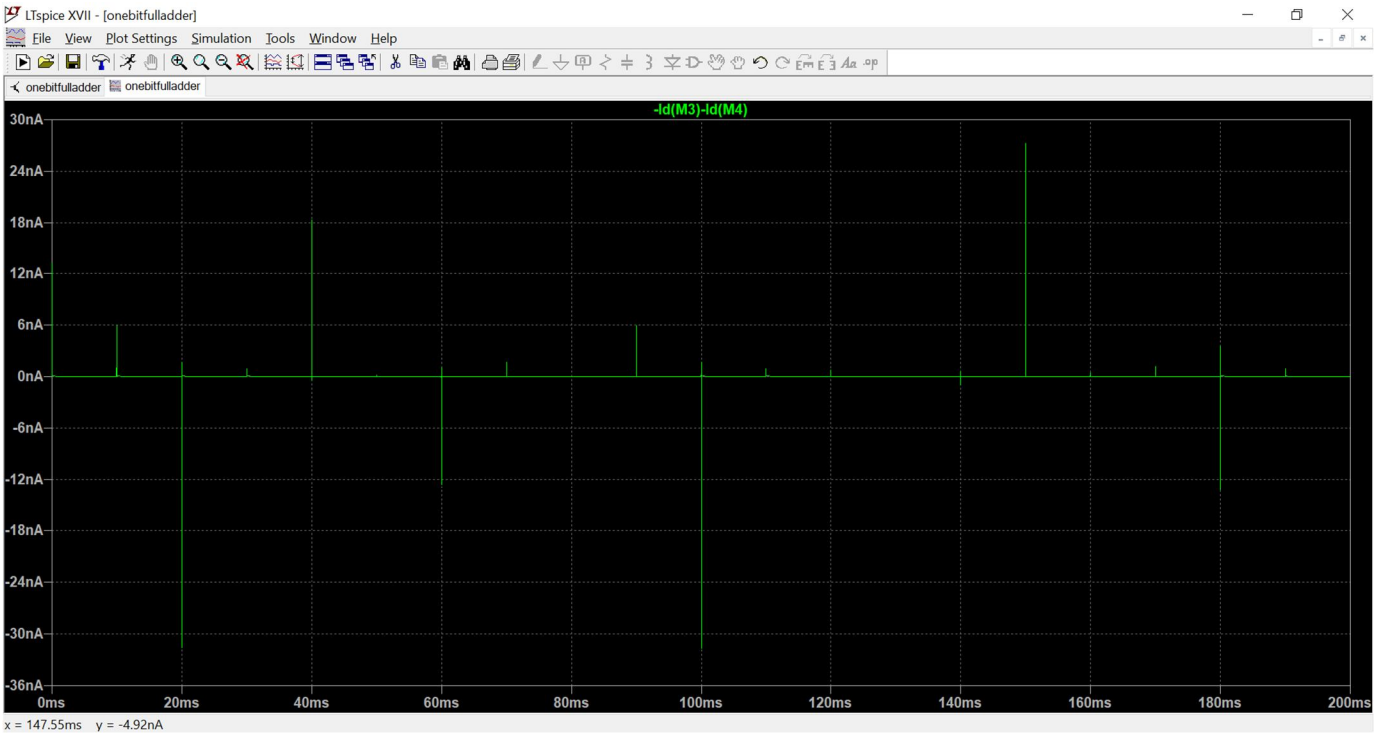

Fig. 6 Sum output current

The Fig. 6 represents the currents obtained at one of the output sum and is observed as 27+32= 59 nA.

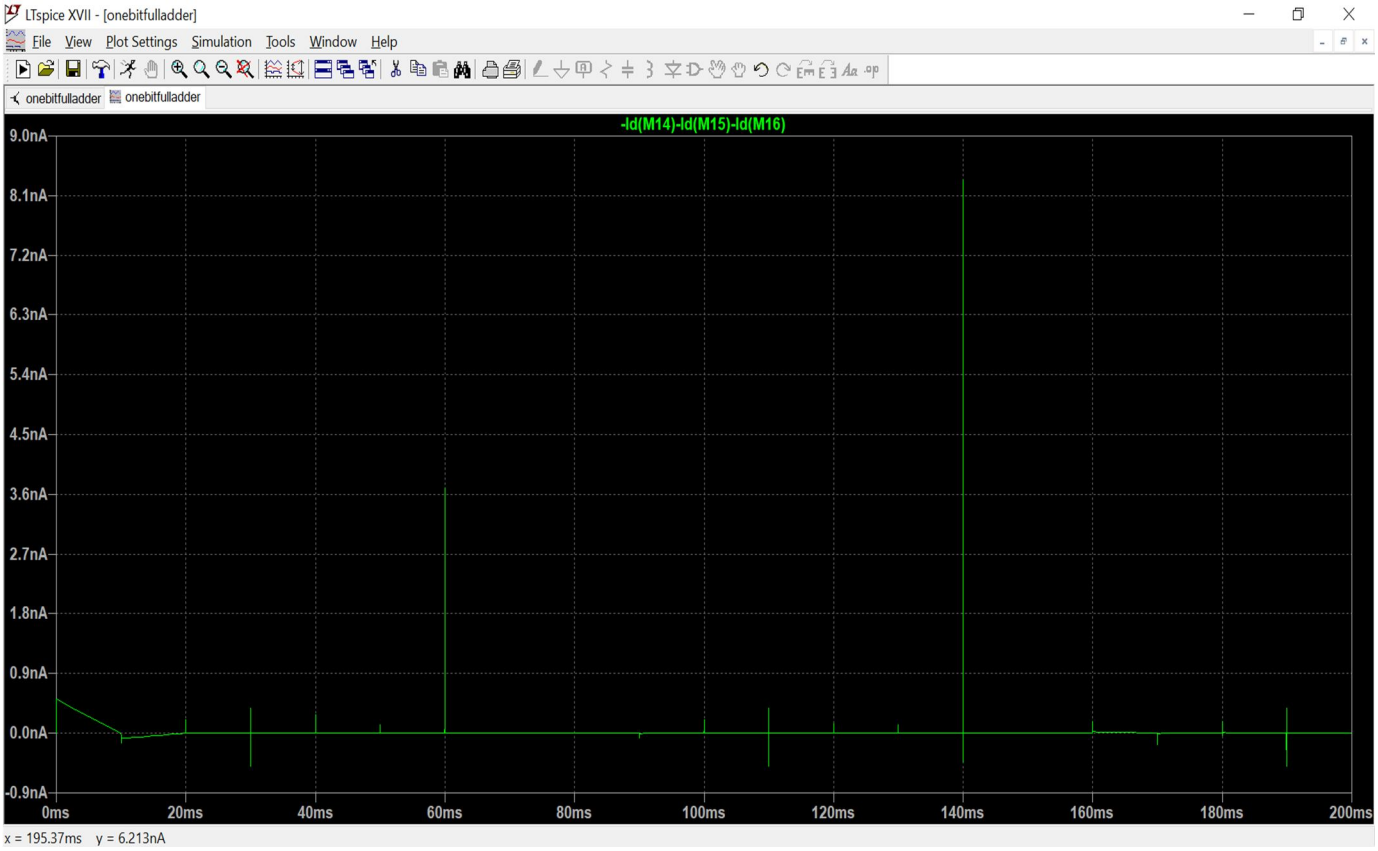

Fig. 7 Carry output current

Fig. 7 represents the currents obtained at carry output of total 8.5 nA.

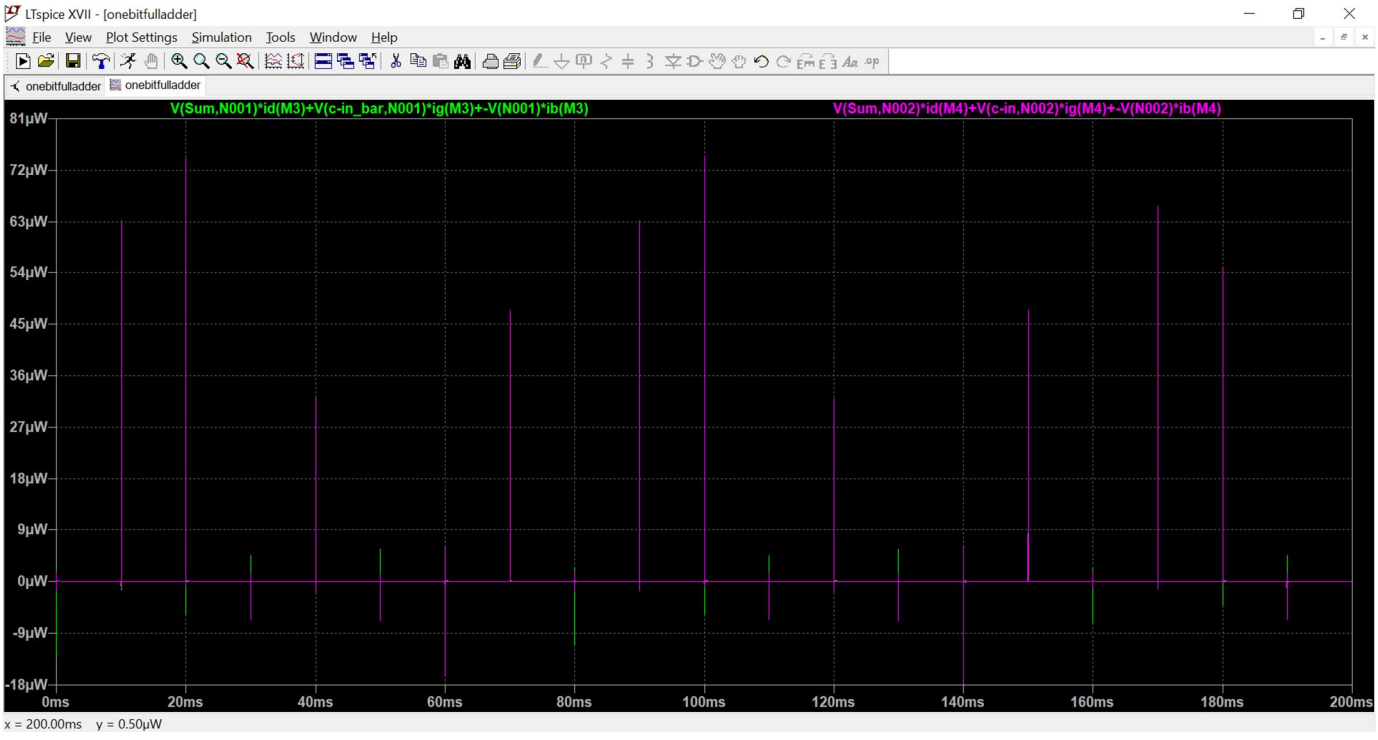

Fig. 8 Combined Power dissipation at output SUM

The Fig. 8 shows the output power dissipation of sum and is observed as 74+16= 90 µWatts is taken low power dissipation.

Fig. 9 Combined Power dissipation at carry

The Fig. 9 shows the output power dissipation of carry and is observed as 7.8 µWatts is taken less power dissipation. Finally the outputs Sum and Carry currents and power dissipation is observed and verified with the LT Spice tools and used on 180nm technology node.

V. CONCLUSION

This work has given a brief explanation about the design of 1-bit Full Adder Circuit using Pass Transistor Logic and the simulation results have shown its correct functionality. The output voltage values of C-OUT can be reduced to logic values of other signals by optimizing the values of drain and source voltages. The implemented Sum and C-OUT circuits have simpler design are expected to have better performances and less power consumption compared to the existing full adder circuit models. Our proposed design has shown a remarkable improvement in area, voltages, current and power, further enhancements can be made to reduce these also. Very less distortion has been observed than the existing adders. The Implemented design is used for future analysis and also designing of 16-bit and 32-bit adder, however, the goal of this implementation is used to design the sub-blocks in ALU.

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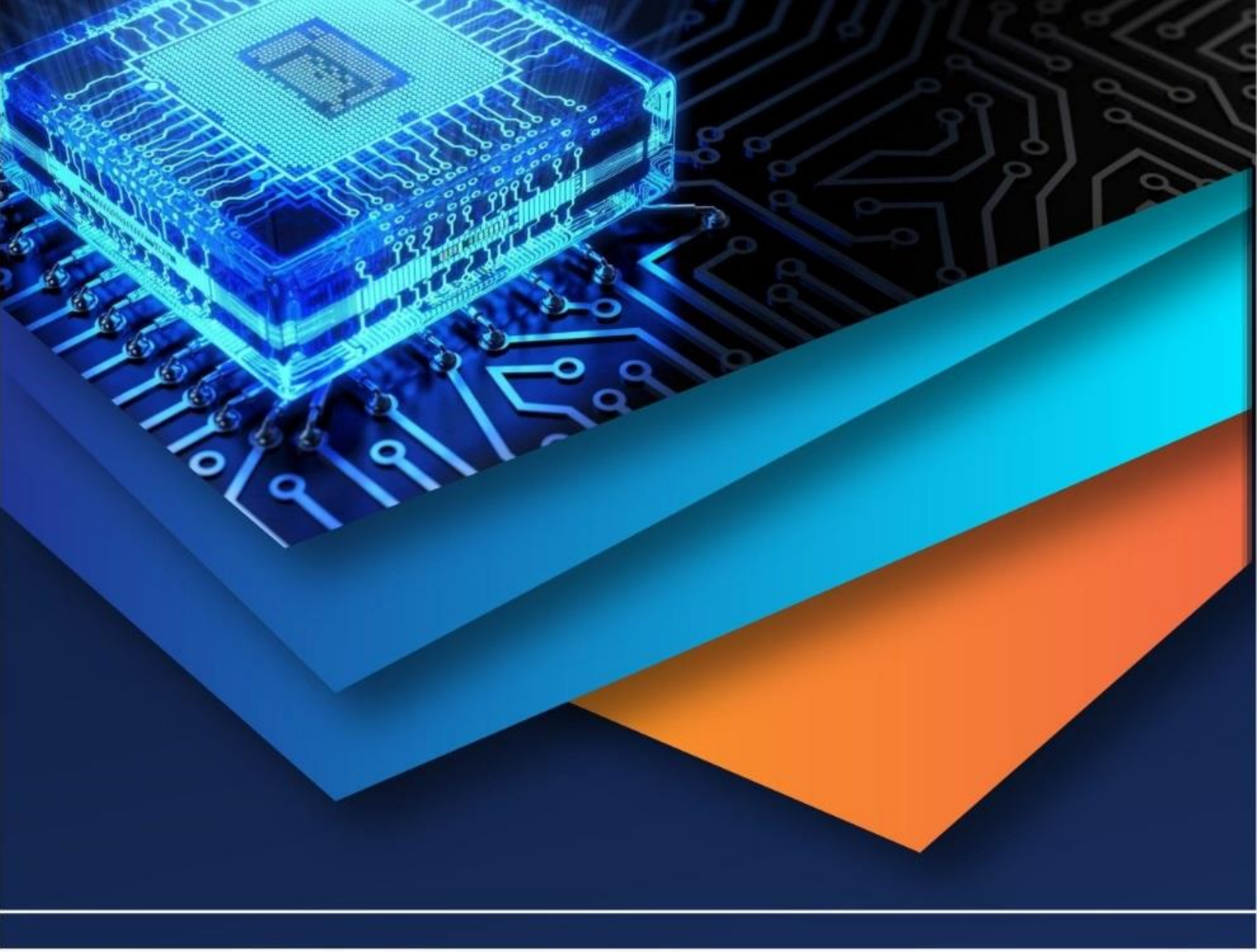

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