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Implementation of Full Adder Circuit using Pass Transistor Logic

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Abstract: ***Advances in Complementary Metal Oxide Semiconductor scaling techniques have led to the proliferate usage of multimedia devices such as laptops, mobiles, graphic cards, personal digital assistants etc. In all these applications, the low power, low die size and high-speed fundamental adder architectures are essential. Various algorithms such as fast-fourier, discrete cosine transforms and inverse discrete cosine transform are used. To implement these algorithms, adders with enhanced performance features such as low area and high-speed computation are vital and necessary. Several adder architectures are available for different applications. In this paper, a ten-transistor using CMOS Exclusive OR and Exclusive NOR gates in combination is proposed. The full adder logic circuit is designed and simulated in cadence virtuoso too environment and operated a dc voltage of 1.5V in 180nm process technology. The proposed full adder logic circuit on an average operates at less power when compared to the conventional CMOS logic full adder circuit. The propagation delay performance was also slightly better when compared to previous circuit. Both the full adder logic simulations have been carried for multiple dc voltages and performance analysis has been carried out at the end of the paper.***

Index Terms: ***NMOS Pass Transistors, CMOS Inverter, PMOS Latches, Input/Output signals.***

I. INTRODUCTION

The continuous scaling of Complementary Metal Oxide Semiconductor (CMOS) technology has played a significant role in enabling compact, high-performance, and power-efficient integrated circuits. With the advancement of semiconductor fabrication techniques, modern electronic systems are now capable of integrating millions of transistors on a single chip. This rapid evolution has led to the widespread adoption of multimedia and portable devices such as laptops, mobile phones, graphics cards, and personal digital assistants. In such applications, power consumption, silicon area, and operating speed have emerged as critical design constraints that directly impact battery life, system reliability, and overall performance.

Arithmetic circuits play a crucial role in the overallperformance of digital signal processing (DSP) and multimedia systems.Am-ong these circuits, the full adder is a fundamental building block extensively used in arithmetic logic units (ALUs) ,multipliers, filters, and signal processing architectures. The efficiency of a full adder directly affects the powerconsumption, speed, and area of complex systems. Therefore, designing a full adder with optimized power dissipation, reduced propagation delay, and smaller die size is essential for achieving high-performance VLSI implementations.

Many signal processing algorithms such as Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT), and Inverse Discrete Cosine Transform (IDCT) rely heavily on repetitive addition operations. These algorithms are widely used in image processing, video compression, and multimedia communication systems. The efficiency of such algorithms depends on the speed and power characteristics of the arithmetic units used for their implementation. Therefore, designing high-speed and low-area full adder circuits is essential to achieve improved system-level performance in modern digital applications.

Several full adder architectures have been proposed in the literature to meet different design objectives. Conventional CMOS full adders provide full voltage swing and good noise margins but require a large number of transistors, leading to increased power consumption and silicon area. To overcome these limitations, alternative logic styles such as transmission gate logic, complementary pass transistor logic, and hybrid logic approaches have been explored. Each of these techniques offers trade-offs between power, delay, robustness, and design complexity.

Pass transistor based and reduced-transistor-count full adders have gained significant attention due to their ability to minimize power consumption and area.In PTL, transistors are used as switches to pass logic levels between nodes. By reducing the number of transistors used to implement logic functions, switching activity and capacitive loading can be effectively lowered. However, careful design is required to address issues such as threshold voltage drop and degraded output voltage levels.

Combining Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates has proven to be an effective approach for implementing compact and efficient full adder circuits.

In this work, a full adder circuit based on a reduced transistor count usingCMOS XORand XNORgate combinations is proposed. The designed full adder requires minimum number of transistors configuration to achieve low power operation. The circuit is designed and simulated using the Cadence Virtuoso tool in a 180 nm CMOS process technology. The proposed design operates at a supply voltage of 1.5 V and is evaluated for power consumption and propagation delay.

Simulation results demonstrate that the proposed full adder achieves an average power reduction of approximately 14 percent compared to the conventional CMOS full adder circuit, while also exhibiting slightly improved propagation delay characteristics. Performance analysis is carried out for multiple supply voltages to validate the robustness of the design. The results indicate that the proposed full adder is well suited for low-power and high-speed arithmetic applications in modern VLSI systems.

II. RELATED WORK

B. Khan, *IEEE TCAS-I,*2025 in this paper introduces a full-swing restored six-transistorCMOS full adder using complementary pass transistor logic. The design aims to achieve minimum transistor count while maintaining full output swing. A novel restoration technique is applied to eliminate degraded voltage levels. The proposed adder uses only six transistors, making it extremely compact. Detailed transistor-level design methodology is presented. Simulations are performed to verify correct operation for all input cases. Performance metrics such as power,delay, and PDP are evaluated.

G. Mahendran and S. Sundar,IEEE 2024,in this paper the authors uses swing restore pass transistor logic(PTL).It concentrates on that it consumes low power.In Pass transistor logic it suffers from degradation of the signals.The swing restoration technique helps to overcome with this issues.It consumes less power compared to all exixting full adders.The drawbacks of this technique are it requires more area for placing additional restoration transistors.Even the power is low,the delay is more due to extra capacitance and with low voltage the restoration becomes weak.The noise margins are also low.

A. K. Verma and R. Singh, IEEE Access2024,in this paper the authors compared the CMOS full adders and pass transistor logic which gives the low power and delay compared to CMOS adder.CMOS full adders are strong output drive and full voltage swing for better signal integrity.The drawbacks are the pass transistors suffers from threshold voltage drop which causes low noise margin.PTL circuits are sensitive to load capacitance ehich causes degradation in speed and power.This paper was evaluated only for one bit adders not for multiple adders like ripple carry adder.

N. Yin, W. Pan, Y. Yu, C. Tang, and Z. Yu,IEEE 2023,this paper introduces 1-bit full adder circuit using pass transistor logic with 8-bit multiplier.This paper focuses on to reduce transistor count and to reduce the power and delay.Firstly,the adder is designed using PTL and evaluates the power and then they added multiplier and again evaluates the power.When both results are compared the ptl using multiplier consumes less amount of power.

The drawbacks are the pass transistor logic suffers from threshold voltage drop and the multiplier suffers from cascading issues.

M. Hasan, M. J. Hossein, M. Hossain, H. U. Zaman & S. Islam,IEEE2020,this paper introduces a full adder circuit using different logic styles it uses pass transistor logic,Transmission gates andConventional Complementary Metal-Oxide-Semiconductor (CCMOS) logicto achieve an energy-efficient full adder with good overall performance in terms of power consumption, propagation delay, and power-delay product (PDP). It is a low power and fast operation.The proposed adder is compared with many existing adders which improves power and speed.The drawbacks are it suffers from signal degradation,driving capability and the complexity of the design increases.

Paramita Chowdhury,Arnesh Halder, Ankit Mahata, SunipaRoy,this paper introduces full adder using pass transistor logic and it mainly focuses on low power consumption and getting better delay compared to CMOS adder.The drawbacks are that it suffers from low threshold and weak noise margins.It has weak driving strengths to drive capacitive loads which degrades the speed of the operation.The complexity of the design increases and limited real time verification. Often evaluated only via simulation without post-layout parasitic extraction or silicon measurement, so real benefits might be overstated.

Despite the numerous PTL and hybrid full adder designs proposed in literature, achieving an optimal trade-off between power consumption, delay, and voltage scalability remains a challenge. Many existing designs focus on either power reduction or speed improvement without comprehensive evaluation across multiple supply voltages. This motivates the present work, which proposes a compact full adder design using pass transistor logic and evaluates its performance under different operating voltages using 180 nm technology.

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III. PASS TRANSISTOR LOGIC (PTL) OVERVIEW

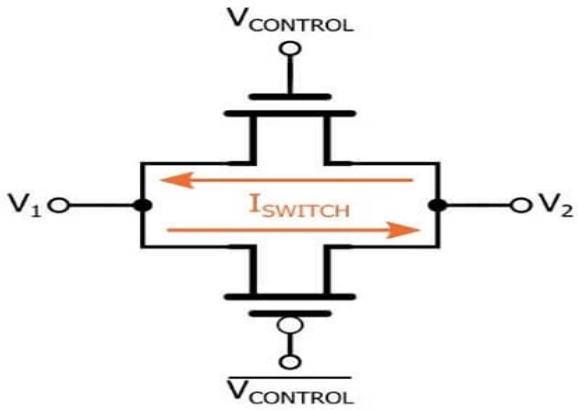

Fig.1. Basic Concept of Pass Transistor Logic Using NMOS Switch

Pass Transistor Logic (PTL) is a logic design technique in which transistors are used as controlled switches to pass logic signals between circuit nodes. Unlike conventional CMOS logic, where pull-up and pull-down networks are employed to generate logic levels, PTL implements logic functions by allowing input signals to directly propagate through transistors. This approach significantly reduces the number of transistors required to implement a given logic function, making PTL an attractive option for low-power and area-efficient VLSI designs.

In conventional static CMOS logic, logic gates are constructed using complementary pull-up networks of PMOS transistors and pull-down networks of NMOS transistors. This structure ensures full voltage swing and high noise margins but results in increased transistor count and higher power consumption. In contrast, PTL eliminates redundant transistors by using NMOS or PMOS devices to selectively pass logic levels, thereby reducing circuit complexity. As a result, PTL circuits typically occupy less silicon area compared to CMOS logic implementations.

One of the primary advantages of PTL is the reduced transistor count. Since logic functions are realized using fewer devices, the overall parasitic capacitance is reduced. This leads to lower switching activity and decreased dynamic power consumption. Reduced transistor count also contributes to smaller layout area, making PTL suitable for high-density integrated circuits and low-power applications such as portable and multimedia devices.

Another significant advantage of PTL is lower power dissipation. By minimizing the number of transistors involved in signal transitions, PTL circuits reduce capacitive charging and discharging losses. This characteristic makes PTL especially effective in arithmetic circuits, such as full adders, where multiple logic operations are performed repeatedly. Consequently, PTL-based designs often exhibit improved power efficiency compared to conventional CMOS implementations.

Despite its advantages, PTL suffers from certain limitations that must be carefully addressed during design. One major drawback is the threshold voltage drop associated with pass transistors.

When an NMOS transistor passes a logic high or a PMOS transistor passes a logic low, the output voltage is degraded by the threshold voltage of the device. This results in reduced output voltage levels, which can affect reliable logic operation, particularly at low supply voltages.

Additionally, PTL circuits may experience voltage swing degradation due to the absence of complementary pull-up or pull-down networks. Reduced voltage swing can lead to increased delay and degraded noise margins. To overcome these issues, PTL circuits are often combined with CMOS inverters or level-restoring stages. Such hybrid approaches improve signal integrity while preserving the benefits of reduced transistor count and low power consumption.

Another important characteristic of PTL is its reduced switching activity. In CMOS circuits, every logic transition involves charging and discharging of large capacitive nodes connected to the power supply rails.

IV. PROPOSED FULL ADDER DESIGN USING PASS TRANSISTORLOGIC

The full adder is a fundamental arithmetic circuit that performs the addition of three single-bit inputs, namely A, B, and carry-in (C_{in}), and produces two outputs: Sum (S) and Carry-out (C_{out}).

The functionality of a full adder can be mathematically expressed using Boolean logic equations. These equations form the basis for designing an efficient transistor-level implementation using Pass Transistor Logic (PTL).
The Boolean expressions for the full adder outputs are given as:

$$S = A \oplus B \oplus C_{in}$$
$$C_{out} = AB + BC_{in} + AC_{in}$$

The SUM output is generated using the XOR operation among the three inputs, while the CARRY output is obtained when any two or more inputs are at logic high. These expressions are well suited for PTL implementation, as XOR and multiplexing operations can be efficiently realized using pass transistors.
In the proposed design, PTL is employed to reduce the overall transistor count and power consumption compared to conventional CMOS implementations. Instead of using separate pull-up and pull-down networks, the proposed circuit utilizes NMOS and PMOS pass transistors to transfer logic levels directly between nodes. This approach minimizes switching capacitance and reduces dynamic power dissipation, making the design suitable for low-power applications.

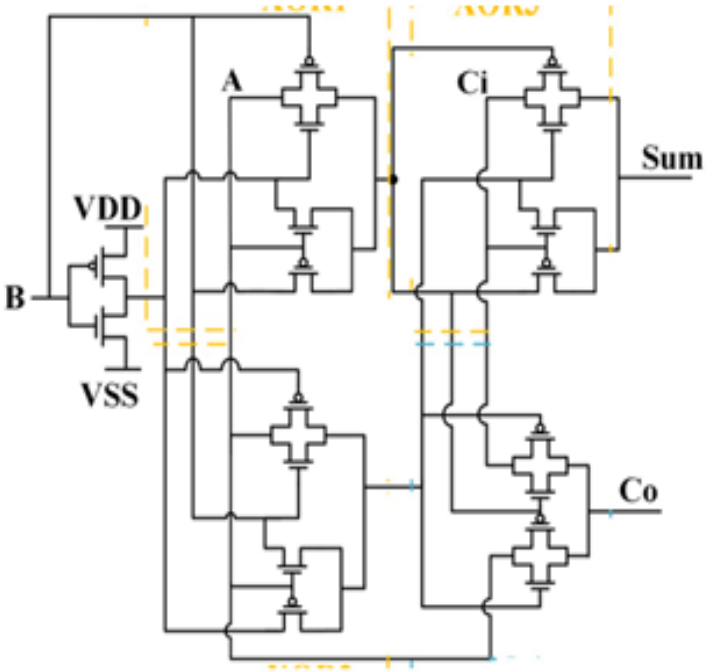

Fig. 2. Full Adder circuit Using Pass Transistor Logic

The SUM generation circuit is implemented using a combination of XOR and XNOR gates realized through pass transistor structures. Initially, the XOR of inputs A and B is generated, which is then combined with the carry-in input to produce the final SUM output.
The CARRY generation circuit is designed using a PTL-based multiplexing approach. The carry-out output is selected based on the intermediate XOR result of inputs A and B.
When $A \oplus B = 0$, the carry-out is determined by the input A, and when $A \oplus B = 1$, the carry-out is determined by the carry-in input. This conditional selection mechanism allows the carry logic to be implemented efficiently with a reduced number of transistors.
To address the voltage degradation inherent in PTL circuits, CMOS inverters are employed at critical output nodes. These inverters restore full voltage swing and improve signal integrity without significantly increasing power consumption. As a result, the proposed full adder achieves a favourable trade-off between reduced power dissipation, acceptable propagation delay, and reliable operation.

The complete transistor-level schematic of the proposed PTL full adder is shown in Fig. 3. The circuit is designed and simulated using Cadence Virtuoso in a 180 nm CMOS process technology. Simulation results validate the correct operation of the SUM and CARRY outputs and demonstrate improved power efficiency compared to conventional CMOS full adder designs.

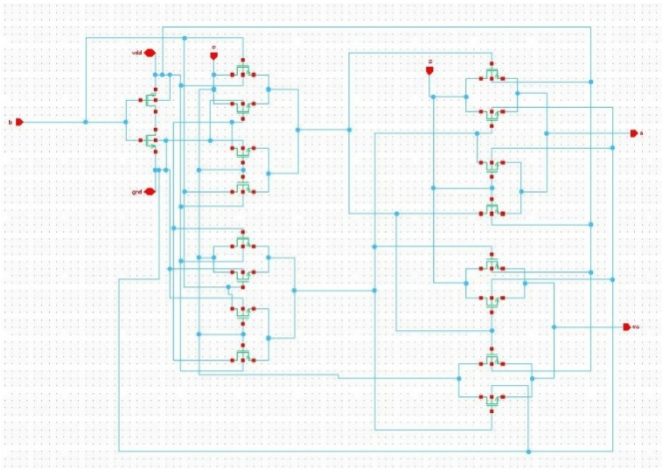

Fig 3 : Schematic Design of Proposed PTL adder in Cadence using 180nm technology

V. SIMULATION SETUP AND METHODOLOGY

The proposed PTL-based full adder circuit was designed and simulated using Cadence Virtuoso Spectre simulation environment. Simulations were carried out using standard CMOS process technology, with emphasis on the 180 nm technology node. To study voltage scalability, simulations were also performed at different supply voltages where required. The selected technology node provides a good trade-off between performance and reliability and is commonly used for academic and low-power VLSI research.

The supply voltage (V_{DD}) for the proposed design was set to 1.5 V for the primary analysis, and additional simulations were conducted at higher voltages such as 2.5 V to evaluate the effect of voltage scaling on power and delay performance. All simulations were performed at room temperature conditions. The circuits were verified for correct logical functionality under all possible input combinations.

To validate the full adder operation, input test vectors covering all eight possible combinations of inputs A, B, and C_{in}were applied using pulse voltage sources. These test vectors ensure complete functional verification of both SUM and CARRY outputs. A suitable load capacitance was connected at the output nodes to model realistic operating conditions and interconnect effects.

In order to ensure accurate and repeatable simulation results, all circuits were designed using standard design rules provided by the selected CMOS process. Transistor dimensions were carefully chosen to balance drive strength and power consumption. Default minimum channel lengths were used, while channel widths were optimized to achieve acceptable rise and fall times at the output nodes.

Transient analysis was performed to evaluate the dynamic behaviour of the proposed full adder under realistic operating conditions. The simulation time was selected such that all possible input transitions were observed multiple times, ensuring stable average power measurements. The input signals were generated using pulse voltage sources with appropriate rise and fall times to avoid unrealistic sharp transitions.

Performance evaluation was carried out by measuring key parameters such as average power consumption, propagation delay, and power-delay product (PDP). The average power was calculated by measuring the supply current over the simulation time interval. The propagation delay was measured as the time difference between the 50% transition points of the input and corresponding output signals. The PDP was computed as the product of average power consumption and propagation delay, providing a comprehensive metric for energy efficiency.

VI. RESULTS AND DISCUSSION

The simulated output waveforms of the proposed PTL full adder are shown in Fig. 4, which confirm correct logical operation for all input combinations. The SUM and CARRY outputs accurately follow the expected truth table of a full adder, demonstrating the functional correctness of the proposed design.

The waveforms also indicate stable transitions and acceptable signal integrity under the applied load conditions.

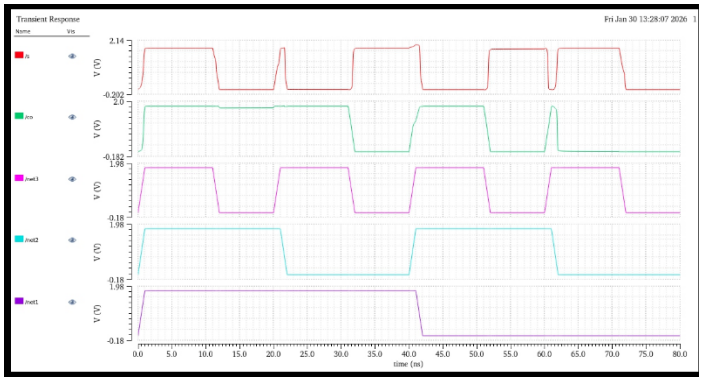

Fig 4. Waveforms of PTL Adder

The simulated waveforms indicate clean transitions and correct logical behavior across all input combinations. No functional mismatches were observed during the simulation, confirming the correctness of the proposed PTL-based full adder design. The output waveforms exhibit stable voltage levels, demonstrating the effectiveness of the voltage restoration stages used in the circuit.

Propagation delay was evaluated by measuring the worst-case delay among 1.5v input transition. The proposed PTL full adder exhibited reduced delay compared to the conventional CMOS full adder due to lower parasitic capacitance and reduced transistor count. The delay performance remained consistent across different supply voltages, indicating reliable operation.

The average power consumption of the proposed design was significantly lower than that of the conventional CMOS full adder. This reduction in power consumption is mainly attributed to fewer switching devices and lower capacitive loading in the PTL implementation. The measured power values validate the effectiveness of PTL in low-power arithmetic circuit design.

The power-delay product (PDP) was calculated to assess the overall energy efficiency of the proposed design. The PTL full adder demonstrated a lower PDP compared to both CMOS and transmission gate based full adders, indicating improved performance in terms of energy consumption per operation.

Fig 5 : Total power delay for vdd 1.5

Table 1: Calculation of parameters of PTL Adder

Parameter	Value
Average Power	1.085uW
Total Delay Power	10.955ns
Power Delay Product	11.89fj

When the supply voltage was increased in Cadence Virtuoso for the 180 nm PTL full adder, the propagation delay decreased due to improved driving strength of the transistors.

The Fig 6 shows the calculations of total power delay for the input transition vdd of voltage 2.5V.

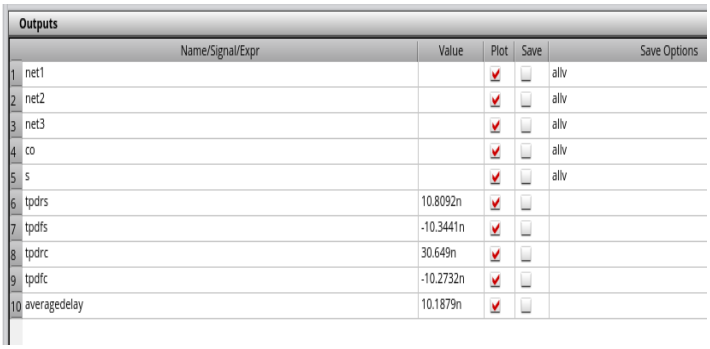

Fig 6: Total Power delay for vdd 2.5

Table 2: Calculation of parameters of PTL Adder

Parameter	Value
Average Power	18.77uW
Total Delay Power	10.18ns
Power Delay Product	191.1fj

It was observed that power consumption increases with higher supply voltage due to increased switching energy, while propagation delay decreases as the drive strength of transistors improves. This trade-off between power and speed is consistent with theoretical expectations. The proposed PTL full adder shows improved energy efficiency, particularly at lower supply voltages.

The reduction in power-delay product highlights the suitability of the proposed design for low-energy arithmetic applications. Compared to conventional CMOS and transmission gate designs, the PTL full adder demonstrates better overall performance, especially in power-sensitive operating conditions.

VII. COMPARATIVE ANALYSIS

A comparative analysis was performed between the proposed PTL full adder and existing CMOS and transmission gate based designs. The results indicate that the proposed design achieves a noticeable reduction in average power consumption while maintaining comparable or improved propagation delay. Compared to conventional CMOS full adders, the proposed design shows a significant percentage reduction in power dissipation due to reduced transistor count.

Although transmission gate based adders provide good signal integrity, they require more transistors, resulting in increased power consumption and area. The proposed PTL full adder offers a better trade-off between power and delay, making it suitable for low-power applications. However, PTL designs may require voltage restoration stages to address threshold voltage degradation, which introduces a minor increase in circuit complexity.

Table 3: Comparision of CMOS Adder and PTL Adder

Parameter	CMOS Adder	PTL Adder
Average Power	699.9mW	1.085uW
Average Delay	12.83ns	10.955ns
Power Delay Product	8.98nj	11.89fj

When compared with transmission gate based full adders, the proposed design offers reduced power dissipation at the cost of slightly increased sensitivity to voltage degradation. However, this limitation is effectively mitigated through the use of output inverters, ensuring reliable operation.

The comparison with previously reported designs in literature further validates the effectiveness of PTL in low-power arithmetic circuits. The observed improvements in power consumption and power-delay product demonstrate the potential of the proposed architecture for energy-efficient VLSI systems.

Advantages of PTL Adder

1) PTL adders use fewer transistors than conventional CMOS adders, resulting in compact circuit design.

2) Fewer switching nodes and smaller capacitances lead to reduced dynamic power dissipation.

3) Due to low power consumption, PTL adders generally achieve better energy efficiency.
4) Reduced transistor count directly translates to lower silicon area, which is beneficial for dense VLSI designs.
5) With fewer series transistors, PTL can provide faster signal propagation under proper voltage conditions.
6) PTL adders are well suited for battery-powered and portable devices.

VIII. CONCLUSION

In this paper, a low-power full adder circuit based on Pass Transistor Logic has been presented. The proposed design utilizes efficient PTL-based XOR/XNOR structures to reduce transistor count, power consumption, and propagation delay. The circuit was implemented and simulated using Cadence Virtuoso in 180 nm CMOS technology at a supply voltage of 1.5 V.

Simulation results demonstrate that the proposed PTL full adder achieves lower average power consumption and improved power-delay product compared to conventional CMOS and transmission gate based full adders. These characteristics make the proposed design well suited for low-power VLSI applications such as portable devices and arithmetic-intensive circuits.

The proposed design successfully balances the trade-off between power efficiency and signal integrity, making it suitable for integration into low-power digital systems. The outcomes of this work highlight the importance of logic style selection in achieving energy-efficient VLSI designs.

IX. FUTURE SCOPE

The proposed PTL-based full adder can be extended to advanced CMOS technology nodes such as 90 nm, 65 nm, and 45 nm to further reduce power consumption and silicon area. Technology scaling combined with voltage scaling can significantly improve energy efficiency, making the design more suitable for modern low-power and portable electronic applications. Performance evaluation across multiple technology nodes would also provide deeper insight into scalability and robustness.

Further improvements can be achieved by incorporating leakage power reduction techniques, such as transistor stacking, power gating, and multi-threshold CMOS approaches. These techniques are particularly important for deep submicron technologies where leakage current becomes a dominant factor. Applying such methods to PTL circuits can enhance their suitability for ultra-low-power VLSI systems.

The proposed full adder can also be integrated into larger arithmetic structures, including ripple carry adders, carry select adders, and multipliers. System-level analysis of these architectures can help evaluate overall performance improvements in terms of power, delay, and area. Such integration would demonstrate the practical applicability of the proposed design in real-world digital signal processing and microprocessor systems.

Additionally, future work may focus on improving signal integrity and noise immunity in PTL circuits by optimizing voltage restoration techniques and exploring hybrid logic styles. The use of adaptive body biasing and error-tolerant design methods can further enhance reliability under process variations and low-voltage operation, making the design more robust for next-generation low-power VLSI applications.

and correct logical behavior across all input combinations. No functional mismatches were observed during the simulation, confirming the correctness of the proposed PTL-based full adder design. The output waveforms exhibit stable voltage levels, demonstrating the effectiveness of the voltage restoration stages used in the circuit.

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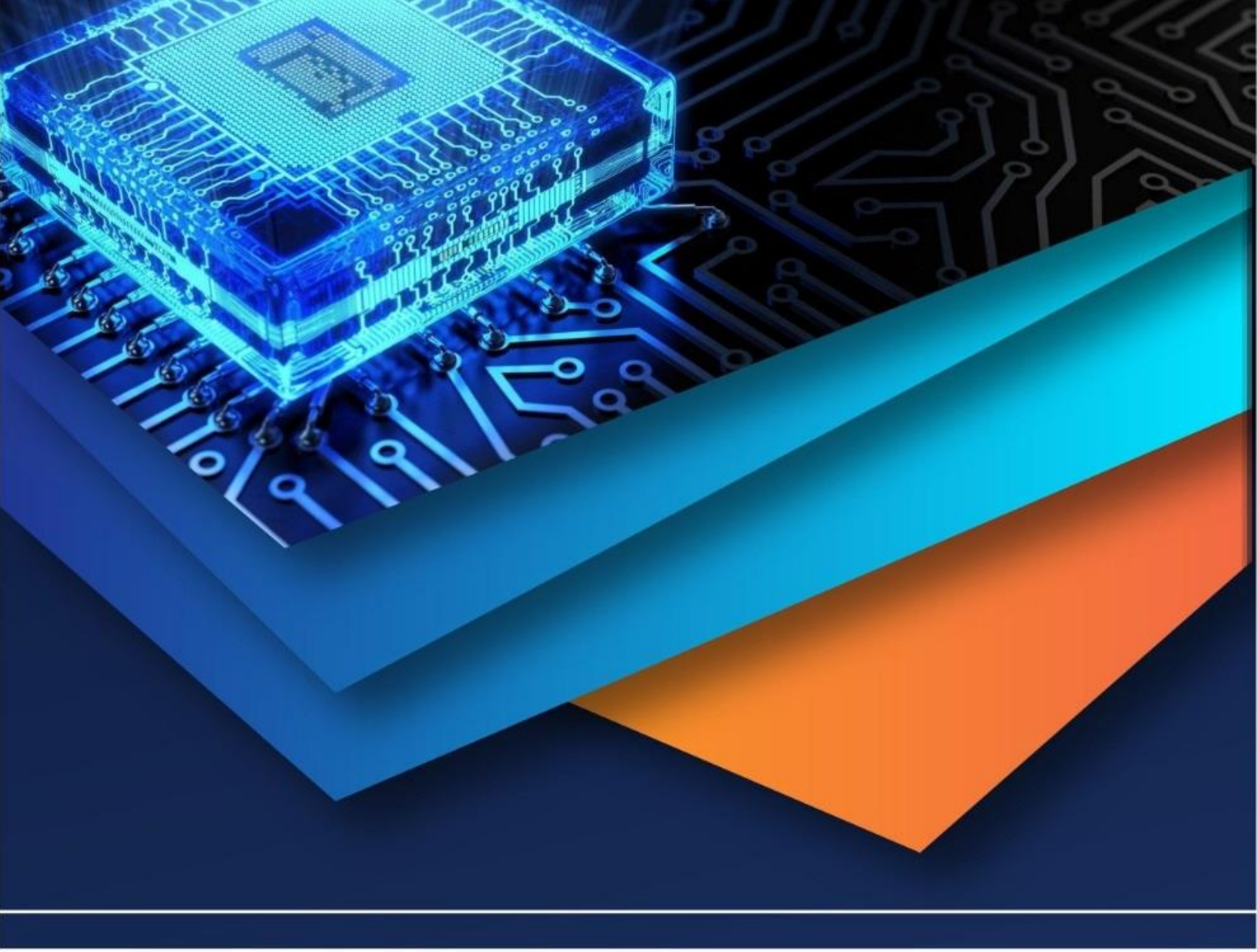

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