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Implementing and Analysing the Performance of Dadda Multiplier on FPGA

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Abstract: ***Multiplication is an arithmetic operation where we will perform some arithmetic operations on the input operands and obtains the final result. Natural multiplication involves partial products generation and adding the obtained partial products to get the final result. But it consumes more power and time if the bit-width increases. Hence, we will use a Dadda Multiplier which results in increasing the execution speed and power efficiency and we will observe the same on FPGA. Hence this arithmetic technique can be used in various error tolerant applications such as image processing, digital processing and FFT.***

I. INTRODUCTION

Even though arithmetic operations are the basic operations it plays a major role in variety of applications. Multiplication is one among those operations. Multiplication is one of the main factors which helps in getting high data rates based on its speed of functionality [1].

Now-a-days the technology has been upgrading rapidly, equally the electronic components should also be upgraded in terms of their power, area, speed etc. Hence in terms of multipliers also there needs to be a better way comparing with the normal multiplication. There are several types of multipliers such as Array Multiplier, Wallace Multiplier, Dadda Multiplier, Vedic Multiplier etc. which are more efficient than normal multiplication.

Basically, the normal multiplication can be performed in two stages which are partial product generation and addition of partial products where as in Dadda Multiplier it is of three stages i) Partial product generation ii) Reducing the height of the tree (partial products) and iii) Adding the obtained partial products. In this paper, we are going to look at how the Dadda Multiplier works and the same can be verified on FPGA.

II. DADDA MULTIPLIER

Dadda Multiplier is a type of binary multiplier which multiplies two binary input operands and gives the result. It is like a tree structure in which we will reduce the height of the tree with the help of Half and Full Adders. The reduction is based on the height of the tree. The minimum height should be 2 and the maximum is based on the bit-width. And each stage should not exceed 1.5 times to its previous stage. For example if it is 8*8 bit multiplication the maximum height that we will consider is 6 and in the next stages the height will be reduced until it reaches to 2.

In this paper we are going to analyse the results for 8*8-bit, 16*16-bit, and 32*32-bit Dadda tree. Let's consider an example for 8*8-bit Dadda Multiplier. Consider the two input operands A and B as $(10101011)_2$ and $(01111001)_2$. Since it is an 8*8 bit the maximum height for the reduction is 6.

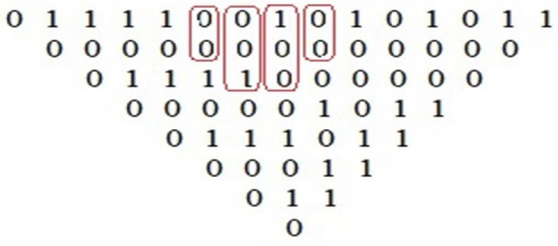
1) Stage-1

```
  1 0 1 0 1 0 1 1
    X 0 1 1 1 1 0 0 1
-----------------------
          1 0 1 0 1 0 1 1
          0 0 0 0 0 0 0 0
        0 0 0 0 0 0 0 0
        1 0 1 0 1 0 1 1
      1 0 1 0 1 0 1 1
      1 0 1 0 1 0 1 1
    1 0 1 0 1 0 1 1
  0 0 0 0 0 0 0 0
```

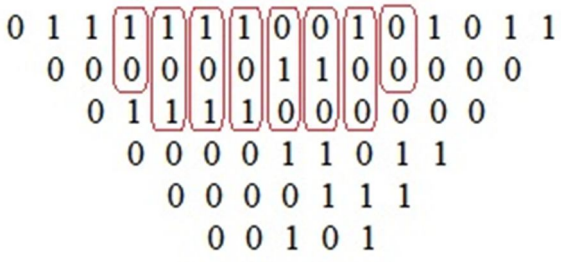
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2) Stage-2

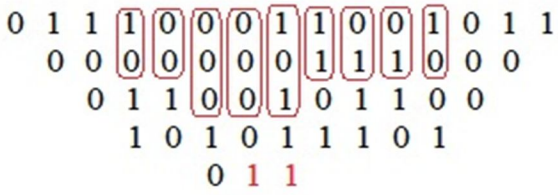
a) Step-1: In this stage the maximum height is 6 and the reduction will only takes place if the column height is more than 6. The result will become as



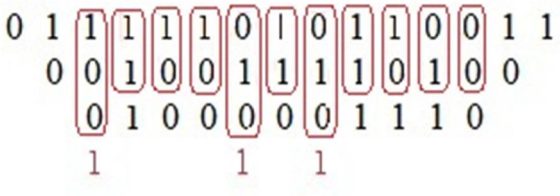
b) Step-2: In this stage the maximum height is 4 and the reduction will only take place if the column height is more than 4. The result will become as



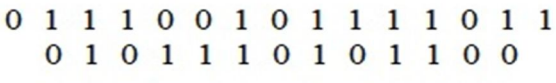
c) Step-3: In this stage the maximum height is 3 and the reduction will only take place if the column height is more than 3. The result will become as



d) Step-4: In this stage the maximum height is 2 and the reduction will only take place if the column height is more than 2. The result will become as



e) Step-5: In this the final partial product will be generated and it is



3) Stage-3

In this stage the addition of the partial products will be performed and the final result is $(0101000011010011)_2$.

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III. RESULTS

In this we have compared Dadda Multiplier with other multipliers and observed its performance in terms of power and area with reference of the other multipliers and observed the same on FPGA. The simulation results for 8*8, 16*16 and 32*32 bits are showed in the following figures:

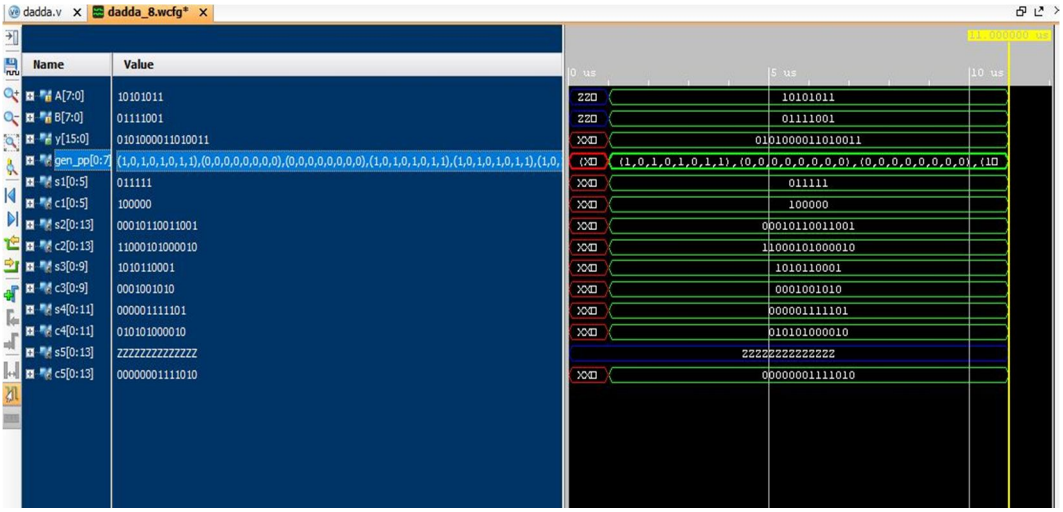


Fig-1: Simulation result for 8*8 Dadda Multiplier

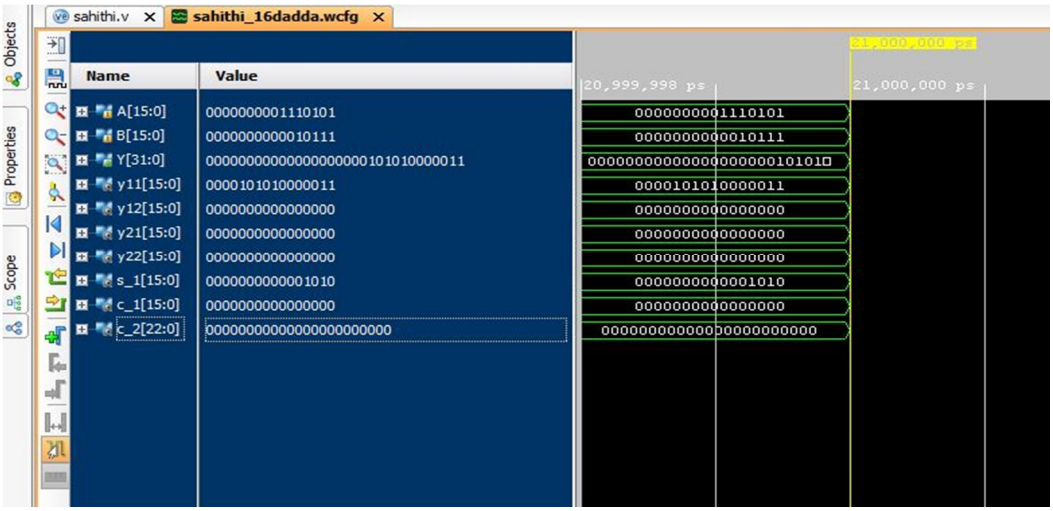


Fig-2: Simulation result for 16*16 Dadda Multiplier

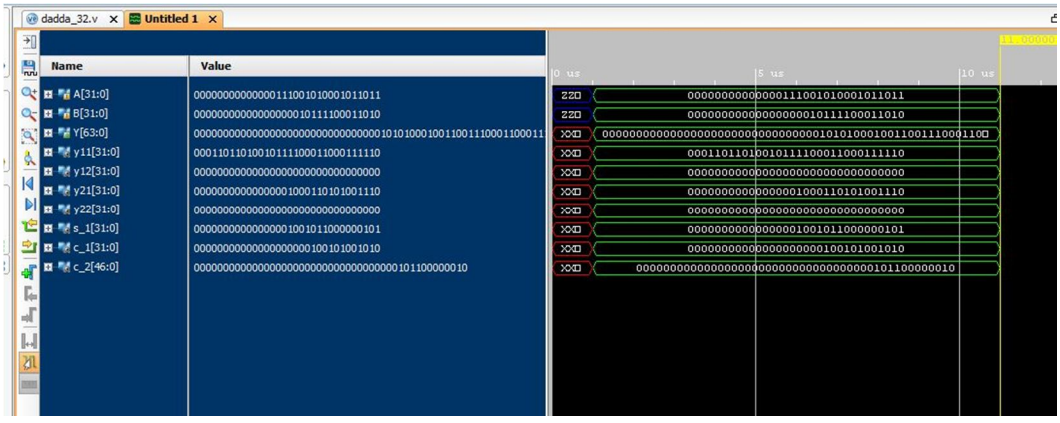


Fig-1: Simulation result for 32*32 Dadda Multiplier

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The RTL design for 8*8 Dadda Multiplier is shown below:

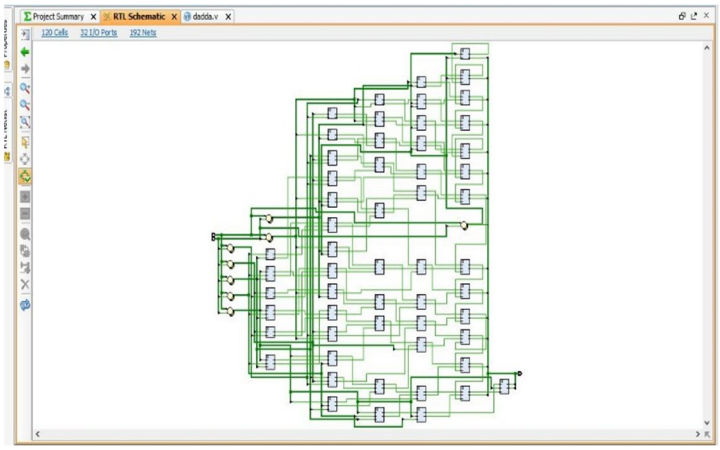


Fig-4: RTL design for 8*8 Dadda Multiplier

The following table indicates the performance of Dadda multiplier for different bits:

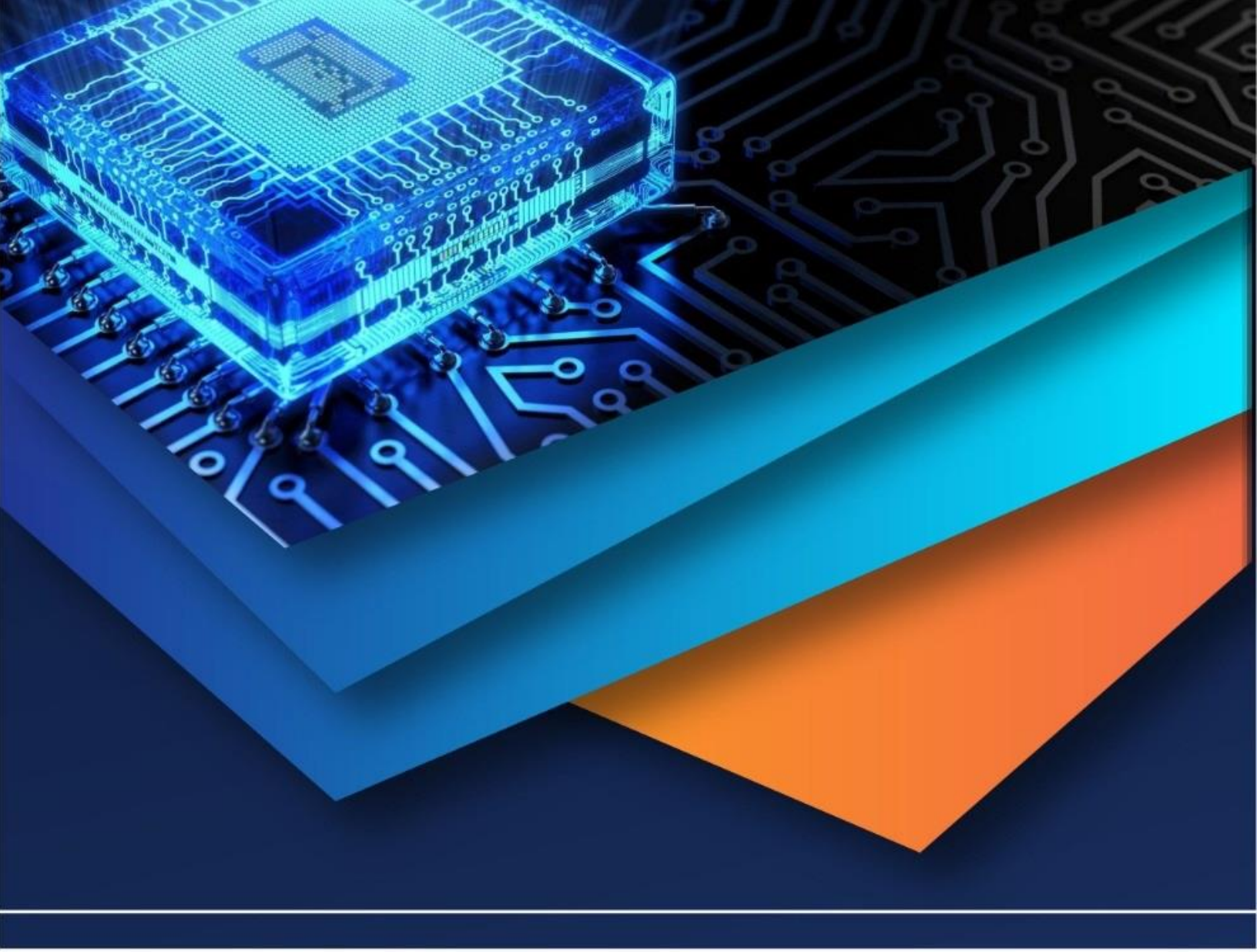
Parameters	8*8 bit	16*16 bit	32*32 bit
Number of LUT's used	675	865	942
Number of occupied slices	1034	1124	1236
Power Consumption	0.24 w	1.23w	1.867w
Delay	5.4 ns	6.96 ns	7.87 ns

IV. CONCLUSION

This paper presents the performance analysis of Dadda Multiplier for different bits. We have compared the results with Array Multiplier [3] and some other multipliers and observed that Dadda Multiplier is more efficient than other multipliers. Hence, dadda multiplier can be used in several applications such as image processing, digital processing etc.

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