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Introduction to Reversible Logic Gates and its Operations

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Abstract: ***Reversible logic is one of the most important issues at the moment and has a wide range of applications, such as low power CMOS, quantum computing, nanotechnol- ogy, cryptography, optical computing, DNA computing, and -digital signal processing (DSP), quantum Dot automata for mobile, communication, computer graphics. It is not possible to detect quantum computing without the implementation of a postponed brain operation. The main objectives of design are logical thinking to reduce quantum costs, circuit depths and the amount of waste disposal. This paper provides basic logical retrospective gates, which in the construction of a highly sophisticated system with retractable circuits as part of the old and unable to perform the most complex operations using quantum computers. Reversible circuits form the basic building block of quantum computers as all quantum functions are reversed. This paper presents data related to older retractable gates found in books and assists research in the design of complex computer circuits using retractable gates.***

Keywords: Defendable Logic, Portable Gate, Dismissal, Trash, Quantum Cost, Quantum-dot Cellular Automata, Reversible Computing, Reversible ALU, Flip Flop using Reversible Gates, Reversible Adder

I. INTRODUCTION

Reduction of energy dissipation remains one of the principal goals inside the VLSI circuit design for decades. R.Landauer confirmed in early Nineteen Sixties, that irreversible hardware computation results in electricity dissipation due to the statistics loss, irrespective of its aware- ness method . it is proved that the loss of each one little bit of records dissipates at the least KTln2 joules of strength (heat), where okay is the Boltzmann's steady and T is absolutely the temperature at which operation is carried out . Reversible good judgment circuits have theoretically zero internal energy dissipation when you consider that they do now not lose statistics. Bennett confirmed that that allows you to avoid KTln2 joules of power dissipation in a circuit, it need to be constructed the usage of reversible common sense gates . The records loss was the supply of power loss that is because of the correspondence to the range of bits decline during the working of the virtual system. the full entropy of the virtual device reduces after the operation due to the low density of output traces in comparison to the input traces of the gate(statistics loss = power loss).

Fundamental DEFINITIONS touching on REVERSIBLE good judgment:

1) *Reversible Feature:* The more than one output Boolean characteristic F(x1, x2,..., xn) of n Boolean variable is known as reversible if: 1. The quantity of outputs is equal to the quantity of inputs. 2. Any output pattern has a completely unique pre-photo. In different words, the reversible features are those that carry out variations of the set of input vectors.
2) *Reversible Common Sense:* Gate A reversible gate is a logical cell that has the N number of inputs and N number of outputs with a one-to-one mapping among the input and output vector. For the logical cell to be reversible the following two situations are not authorised. 1. Direct fan-outs from the reversible gates. 2. remarks from a gate output at once to its input.
3) *The wide Variety of Reversible gates (N):* This refers back to the quantity of reversible gates used in circuit.
4) *The Variety of Steady Inputs (CI):* This refers to the quantity of inputs that are to be maintained regular at both zero or 1 so that it will synthesize the given logical function.
5) *The Wide Variety of Garbage Outputs (Move):* This refers to the number of unused outputs present in a reversible circuit. One cannot keep away from the garbage outputs as these are very important to reap reversibility.
6) *Quantum Cost (Quality Control):* This refers to the price of the circuit in phrases of the cost of a primitive gate. it's miles calculated by way of understanding the variety of primitive reversible good judgment gates (1 1 or 2 2) required to recognize the circuit.
7) *Flexibility:* This refers to the universality of a reversible logic gate in knowing greater features.
8) Design constraints for Reversible logic circuits within the layout of any reversible logic circuits the following factors should be considered to acquire an optimized circuit. i. Fan-out is not approved. ii. minimal quantum price. iii. garbage outputs need to be minimum. iv. consistent inputs need to be minimum. v. minimum variety of good judgment intensity or gate degrees. vi. minimal delay.

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A. *The Concept*

Reversibility in computing means that information about computational states can never be lost, so we can restore any previous steps by counting them back or un-computing the results. This is called logical reversibility. Logical reversibility has advantages. Physical reversibility can only be achieved after use. Physical reversibility is the process of converting heat into energy. Perfect physical reversibility is practically impossible. The computing system heats up when the voltage level changes from positive to negative: bits from zero to one. Most of the energy needed to make that change goes hot. Instead of converting the voltage to new levels, the reversible circuit elements slowly transfer the charge from one node to another. In this way, only one minute of energy is lost during each transition. Reversible computing strongly influences digital logic designs. Reversible logic elements are required to recover the input status from the output. It also affects instruction sets and high-level programming languages. Finally, these must also be reversible to provide optimal efficiency**.**

II. MOTIVATION BEHIND REVERSIBLE LOGIC

High-performance chips emit large amounts of heat, placing a practical limit on how far we can improve system performance. Reversible circuits that store information will soon provide the only physically possible way to improve performance, by uncomputing rather than disposing of bits. Reversible computing also improves power efficiency. Energy efficiency primarily affects the speed of circuits such as nanocircuits and therefore affects the speed of most computing applications. Reversible computing is needed to re-improve the portability of devices. This allows the size of the circuit element to be reduced to the limit of molecular size and thus the devices become more portable. Despite the fact that hardware design costs will be higher in the near future, the need for reversible computing cannot be ignored in this age of computing, although power costs and performance are more effective than logic hardware costs.

A. *Reversible Logic Gates*

Reversible Logic Gate is an n-input n-output logic device with one-to-one mapping. It helps to identify the output from the input and can specifically recover any input from the output. Also direct fan-out is not allowed in the synthesis of reversible circuits because one to many concept is not reversible. Fan-out, however, is achieved by the use of additional gates in reversible circuits. The reversible circuit must be designed using a minimum number of reversible logic gates. From a reversible circuit design perspective, there are several parameters that determine the complexity and performance of a circuit.

Number of reversible gates (N): Number of reversible gates used in the circuit.

Fixed number of inputs (CI): Specifies the number of inputs that must be kept constant at 0 or 1 to synthesize a given logical function.

Worst Output Number (GO): Indicates the number of unused output in reversible logic cir- cuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility

Quantum Price (QC): This refers to the circuit price In terms of primitive door price. It is calculated To find the number of primitive reversible logic gates(1 1 or 2 2) is required to comprehend the circuit

* *

III. BASIC REVERSIBLE LOGIC GATES

A. *Feynman Gate*

Feynman gate is a 2 2 one through reversible gate as shown in figure 1. The input vector is I(A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q≝A [U+F0C5] B. Quantum cost of a Feynman gate is 1. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

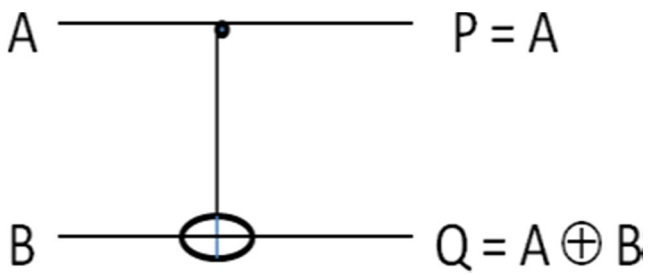

Figure 1

1) Figure 1: Feynman Gate Truth table of Feynman gates

Double Feynman Gate (F2G)

Fig.2 shows a 3 3 Double Feynman gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A [U+F0C5] B, R=A [U+F0C5]C. Quantum cost of double Feynman gate is 2.

Truth table of double Feynman gates

a) Toffoli Gate

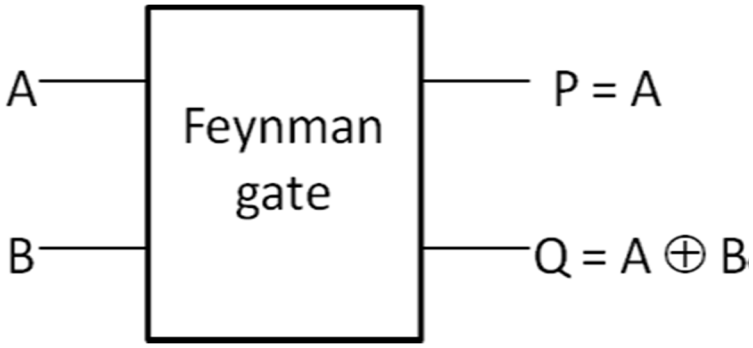

Figure 2

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Figure 3

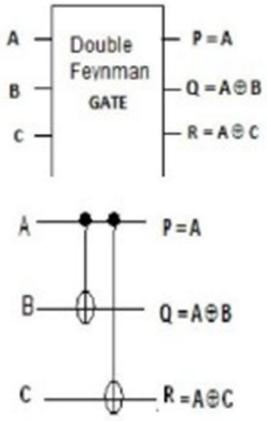

Fig 2: Double Feynman gate

Figure 4

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Figure 5

Fig 3 shows a 3 3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB [U+F0C5]C. Quantum cost of a Toffoli gate is 5.

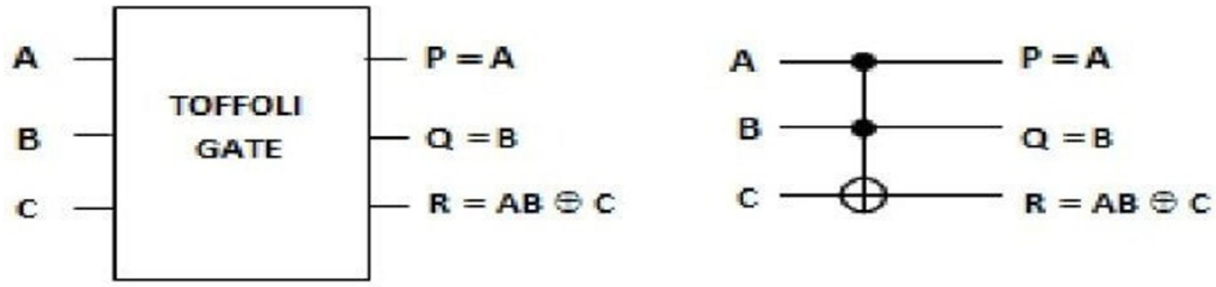

Figure 6

2) Fig 3: Toffoli gate Truth table of Toffoli gate

Fredkin Gate

Fig 4 shows a 3 3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A'B [U+F0C5] AC and R=A'C [U+F0C5]AB. Quantum cost of a Fredkin gate is 5.

3) Fig 4: Fredkin gate Truth table of fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Figure 7

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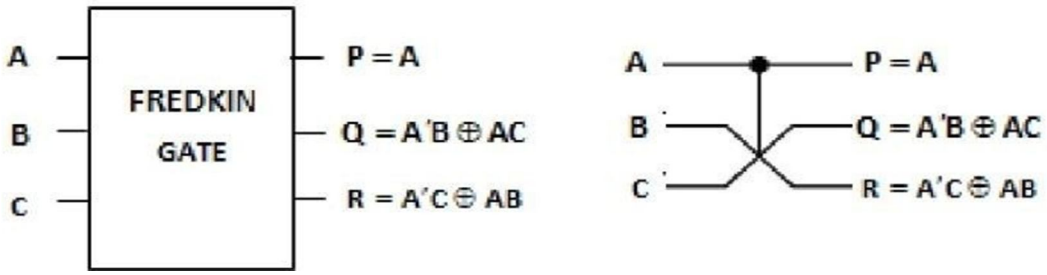

Figure 8

a) Peres Gate

Fig 5 shows a 3 3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A [U+F0C5] B and R=AB [U+F0C5] C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

A full- adder using two Peres gates is as shown in fig 6. The quantum realization of this shows that its quantum cost is 8 two Peres gates are used

TSG gate: Fig 7 shows a 4 4 TSG gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). The output is defined by P = A, Q = A'C" ⊕B', R = (A'C' ⊕B')[U+F0C5]

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Figure 9

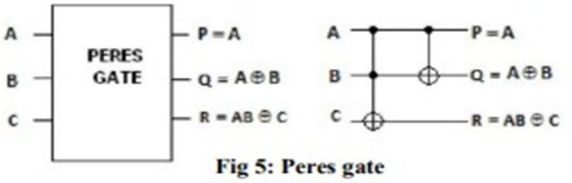

Fig 5: Peres gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table 5: Truth table of peres gate

Figure 10

D and S = (A'C' ⊕ B').D ⊕ (AB ⊕ C) Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost. It can be verified that the input pattern corresponding to a particular output pattern can be uniquely determined. The proposed TSG gate is capable of implementing all Boolean functions and can also work singly as a reversible Full adder

b) Sayem Gate

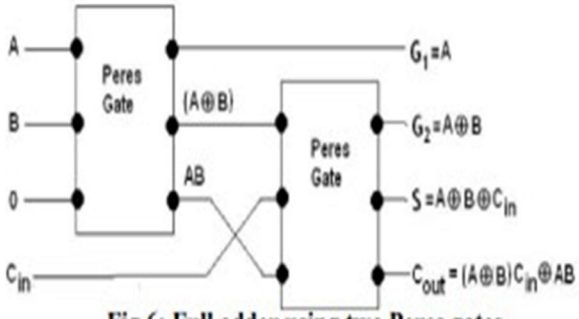

Fig 6: Full adder using two Peres gates

A single 4*4 reversible gate called PFAG gate with quantum cost of 8 is used to realize the multiplier

Figure 11

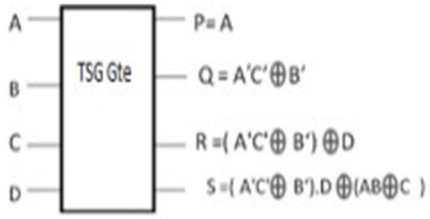

Fig 7: TSG gate

Fig 8: TSG Gate Working As Reversible Full Adder

Figure 12

SG is a 1 trough 4x4 reversible gate. The input and output vector of this gate are, Iv = (A, B, C, D) and Ov = (A, A'B [U+F0C5]AC, A'B [U+F0C5]AC[U+F0C5]D, AB [U+F0C5]A'C
[U+F0C5] D). The block diagram of this gate is shown in Fig 9

D-latch: The characteristic equation of D-Latch is Q+ =DE+E'Q. It can be realized with one SG. It can be mapped with SG by giving E, Q, D and 0 respectively in 1st, 2nd, 3rd and 4th input of SG. Fig 10(a) shows the design of D-Latch with only Q output and Fig 10(b) shows the design of reversible D-Latch with both the output Q and Q+ .One FG is needed to copy and produce the complement of Q from SG for the design of Fig 10(b)

4) Fig 10(a): Proposed design of D-Latch with only output Q

Reversible Positive Edge Triggered T-Flip Flop: This section includes the construction of Master-Slave T FlipFlop using reversible gates. The truth table is shown in the Table 6. The design is shown in the

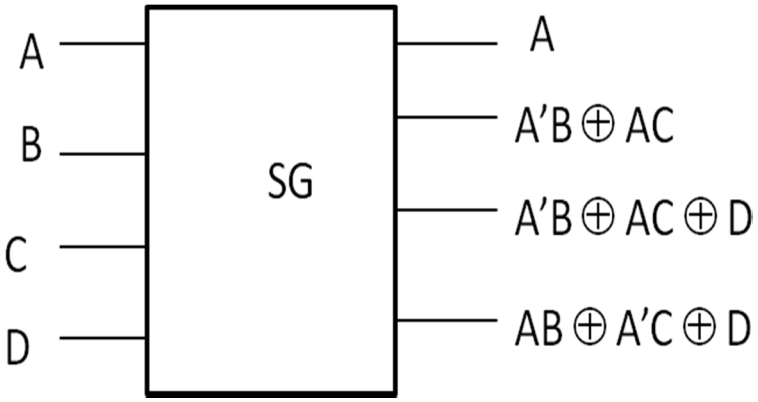

Figure 13

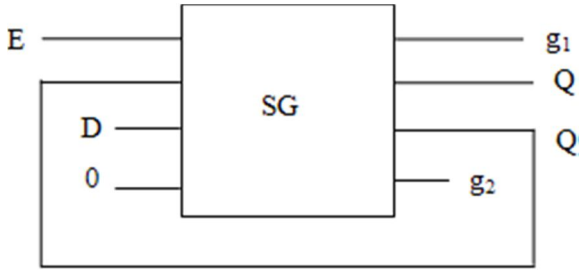

Figure 14

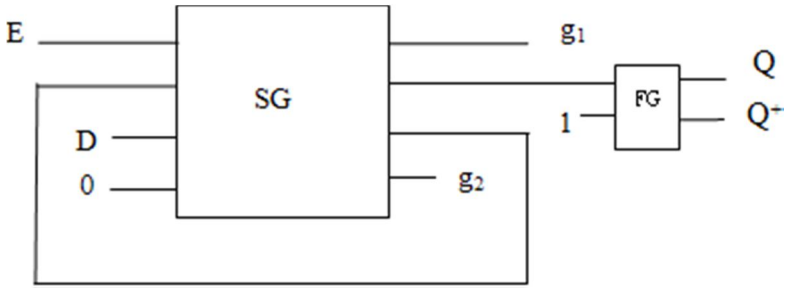

FIGURE 15

a) Proposed design of D-Latch with output Q and Q+

Figure 11 (10). The added Feynman gate as shown in figure to get the desired functionality of Q-1.positive edge triggered T flip-flop This construction is done can be done by replacing fredkin and Feynman gate by single sayem gate The reversible realization of T Flip-flop has two SG gates and one Feynman Gate is shown in fig 12 (7).

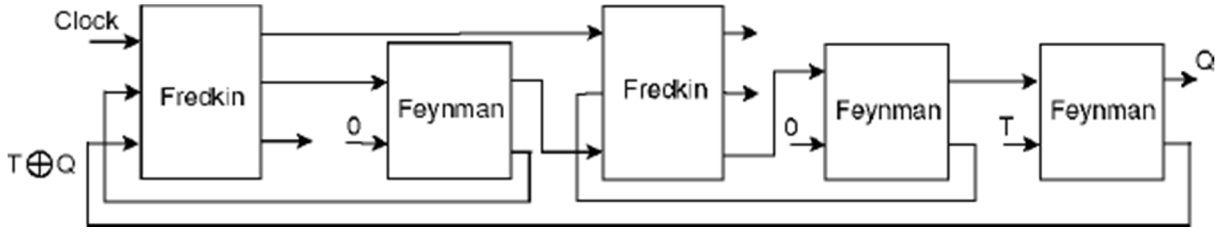

Figure 16

CLK	T	Q_{t-1}	Q
0	O	0	0
1	O	0	0
0	O	1	1
1	O	1	1
0	1	0	0
1	1	0	1
0	1	1	1
1	1	1	0

Figure 17

Reversible positive edge triggered T flip-flop reversible T flip flop

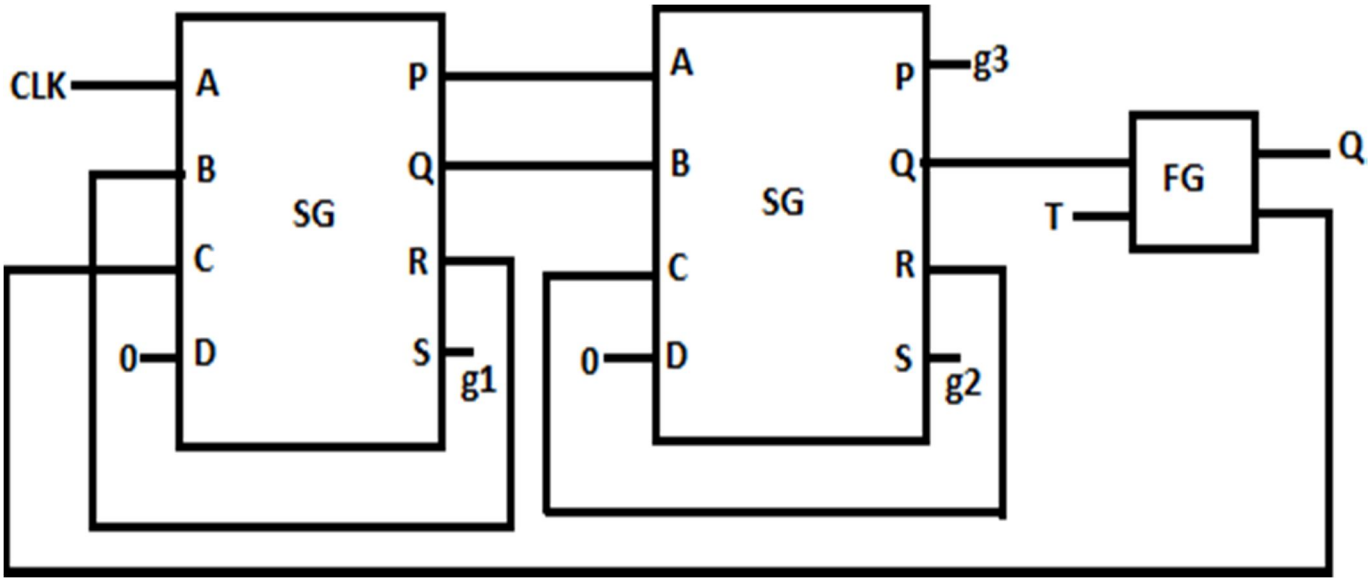

Figure 18

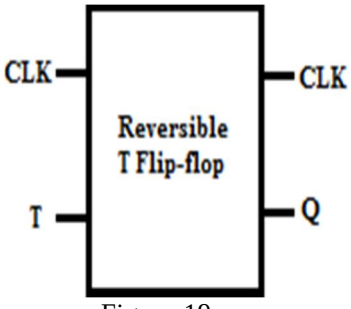

Figure 19

b) Proposed 4-BIT Asynchronous UP/DOWN Counter

The reversible design of the asynchronous Up/Down Counter is shown in Fig. 14. The Up/Down operation of this reversible design is controlled by the control input UP/DOWN. When this control input is 1 the reversible design operates as an Up counter. When this control input is 0 the reversible design operates as a Down Counter

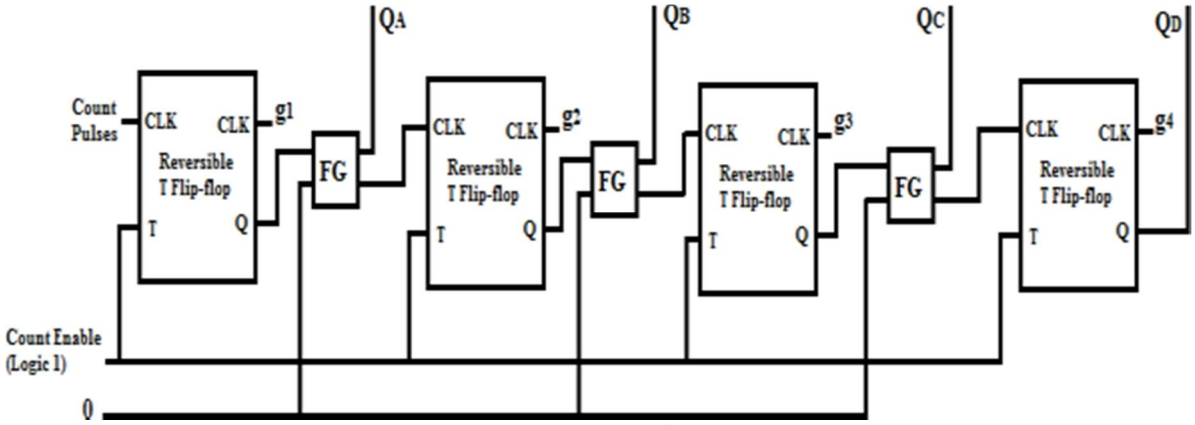

Figure 20

5) Fig 14: Proposed 4-bit Reversible Asynchronous down Counter

APPLICATIONS Reversible computing may have applications in computer security and transaction processing, but the major long-term benefits are felt in areas where high power efficiency, speed and performance are required. Areas such as:

a) Low power CMOS
b) Quantum computer
c) Nano Optical computing
d) Low power arithmetic and design of data paths for digital signal processing (DSP
e) Field programmable gate arrays (FPGAs) in CMOS technology for extremely low power, high test capability and self-repair

IV. CONCLUSION

We have provided a mechanism to comprehend Multipurpose binary reversible gates. Such gates can be used Absorption of Boolean functions in simple circuits. Just like that Possible way to build multi-valued reversible gates Have similar properties. The proposed asynchronous design There are applications in digital circuits such as timers / counters, This is the work of making reversible ALU, reversible processor etc. An important step in building a large and complex Reversible Sequential Circuit.

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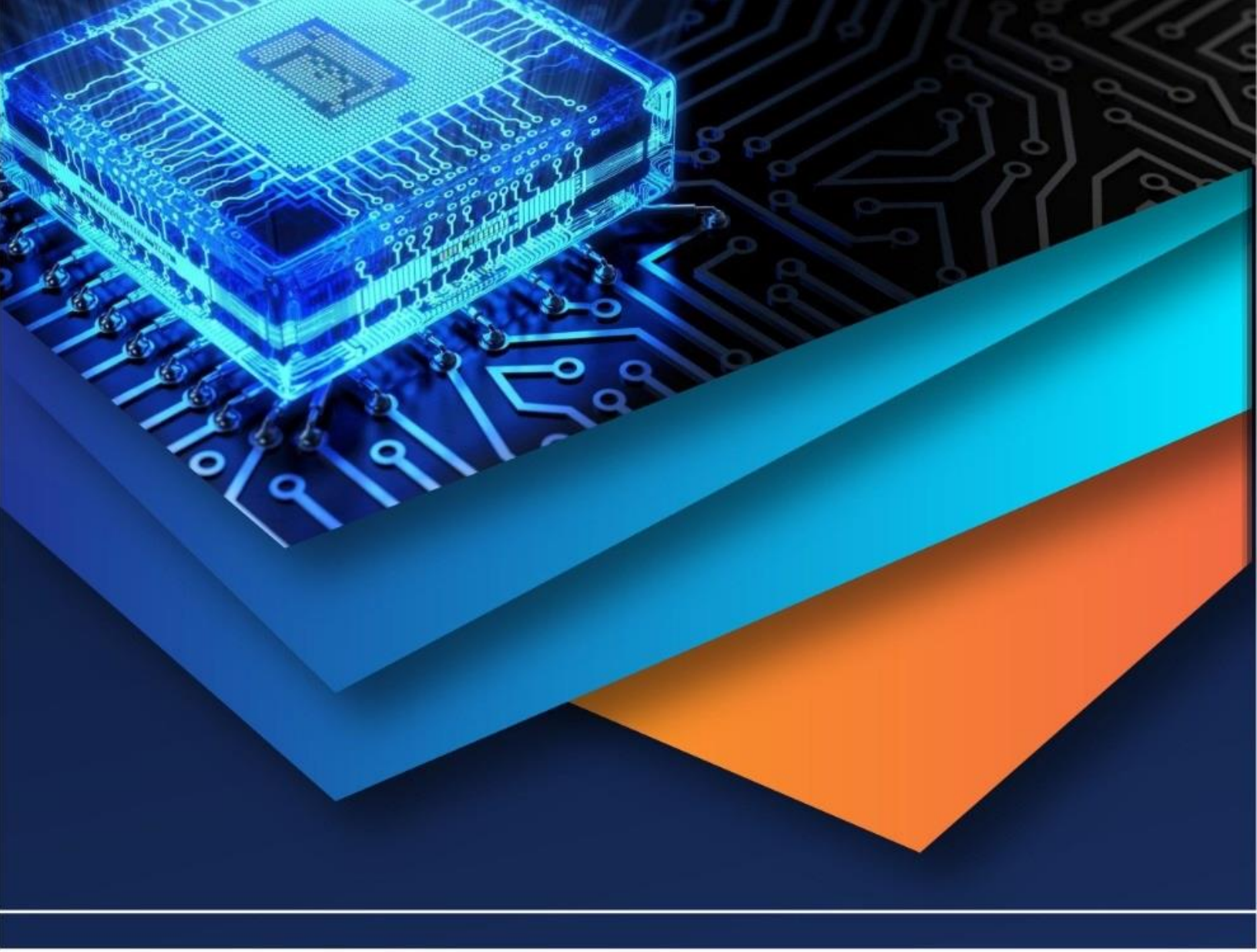

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