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Layout Design of Row Decoder using Cadence

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Abstract: Logic circuits, data transport circuits, and analogue to digital conversions all frequently employ decoders. For the line decoders, a mixed logic design approach incorporating transmission gate logic, pass transistor logic, and complementary metal-oxide semiconductor (CMOS) technology is employed to achieve the desired performance and operation.
A unique topology is proposed for the 2 to 4 decoders, which calls for a topology with fourteen transistors to reduce operating power and transistor count and a topology with fifteen transistors to achieve high power and low delay performance. For a total of four new designs, standard and inverting decoders are created for each situation. All of the suggested decoders have a low transistor count in comparison to their traditional CMOS architectures.
Last but not least, a number of suggested solutions demonstrate a notable improvement in operating power and propagation latency, exceeding CMOS in virtually all instances.
Keywords: Decoders, Mixed Logic design, Logic gates, Power and Delay Optimization.

I. INTRODUCTION

More room is required in internal circuits for general decoders. Using two inverters and four AND gates, a general-purpose traditional 2-4 decoder with a total of 28 transistors can be created. Similar to this, a 4-16 conventional decoder that uses 104 transistors overall and 4 inverters, 16 AND gates, and 16 AND gates can be created. By combining transmission gate logic and pass transistor logic, new mixed logic can lower these sizes. Speed and power are also increased via pass transistor logic. The CMOS circuits have greater propagation delays, power dissipation, and die area requirements. All of these characteristics will be as minimally reduced as possible by the suggested method. The design of integrated circuits frequently makes use of CMOS technology, which ranges from simple digital logic gates to System on Chips (SoCs) [2].
Both n-channel enhancement mode and p-channel enhancement mode metal oxide semiconductor field effect transistors (MOSFET) are employed in complementary metal oxide semiconductor (CMOS) technology. To obtain superior fan-in and fan-out capabilities, MOSFET additionally uses NMOS transistors as pull-down networks and PMOS transistors as pull-up networks. Because CMOS logic circuits can endure various voltage scaling and enable transistor channel sizing to be as small as possible, this technology can operate at high speeds while using little power.
The pass transistor logic (PTL) was first introduced in the early 1990s, and various design approaches are discussed in [4] to [6] with the aim of generating additional opportunities to achieve high speed and occupy less space on the die by applying the inputs directly to the gates of transistors and drain-source terminals of MOSFETs. The pass transistor designs use individual PMOS and NMOS transistors, in contrast to the transmission gate logic designs, which use parallel pairs of either NMOS or PMOS transistors. All digital circuits, input and output circuits, data transmission modules, memory devices, and all basic digital circuits employ decoders extensively.

II. DESIGN METHDOLOGY

Decoder is a multiple input and multiple output combinational logic circuit that accepts 'n' Coded inputs and generates 2^n output signals or fewer if there are any unused combinations in n- bit coded input data.
The decoder circuits designed and analyzed in this work are n:m line decoders, as they accept n inputs and generate 2^n outputs such that m=2^n.

A. Conventional Design

The decoder, which decodes coded input typically utilised in all forms of memory devices, is the fundamental digital module as shown in Fig.1 and Fig.2 shows the Gate level logic of Decoder. An n input to 2n output binary decoder is the most used type of decoder circuit. The logic of any application is created using CMOS technology in the typical architecture.

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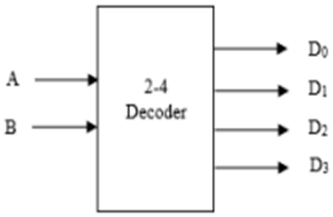


Fig.1. Block diagram of 2-4 Decoder.

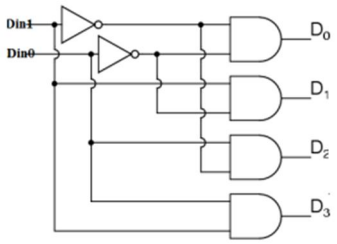


Fig. 2. 2-4 Decoder Gate level diagram.

Logic operation of 2:4 decoder is summarized Table I where A and B are the inputs and D0 to D3 are outputs of the decoder. An inverting 2:4 decoder generates complementary outputs D0 - D3 and each time the selected output will be set to logic 0 and the other three outputs are set to logic 1. The logic operation of an inverting 2:4 decoder is summarized in Table II

Table I : 2:4 Decoder Truth Table

A	B	D0	D1	D2	D3
L	L	H	L	L	L
L	H	L	H	L	L
H	L	L	L	H	L
H	H	L	L	L	H

Table II : 2:4 Inverting Decoder Truth Table

A	B	D0	D1	D2	D3
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

B. Pass Transistor Logic

More NMOS and PMOS transistors are utilised in the pass transistor logic, either in parallel or in series, to create the appropriate logic. Transistors function as switches in this PTL logic to propagate the VDD to the output port and produce the desired logic. This technique lowers the overall number of active transistors, but it has the disadvantage that voltage variations are present at each level's output and spread to the final output stage Therefore, these PTL design methodologies, as opposed to conventional designs, are only for a few specific applications

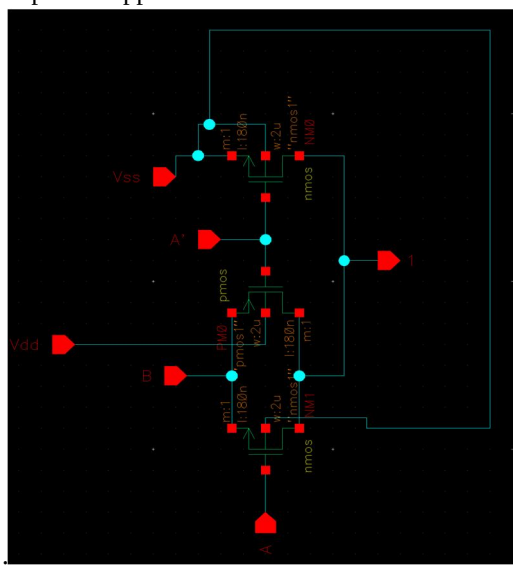


Fig. 3. DVL AND

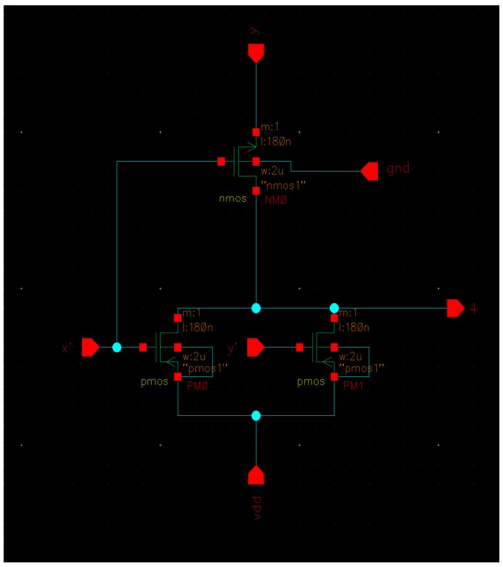


Fig. 4. DVL OR

C. Transmission Gate Logic

Transmission gates are utilised frequently because they have the advantage of keeping a good output voltage value over pass transistor logic. The transmission gate logic is used in the suggested design to implement the low power, high performance, and small chip area decoder designs using 15- transistors high power and high-power inverted decoder and 14 transistor high power and low power inverted decoders, respectively.

A transmission gate logic AND gate is depicted in Fig. 5. This gate only functions when X and Y are both logic high (H,-H), in which case the output is logic high; otherwise, it is logic zero. Similar to this, Fig.6 depicts an OR gate that operates when either X or Y is at logic high; otherwise, the output is logic zero. Only one transmission gate and one NMOS transistor are needed in both cases for the circuits. In contrast to traditional CMOS 6-transistors designs, dual value logics of the AND gate and OR gate are shown in Fig. 3 and Fig.4, which require just 3 transistors.

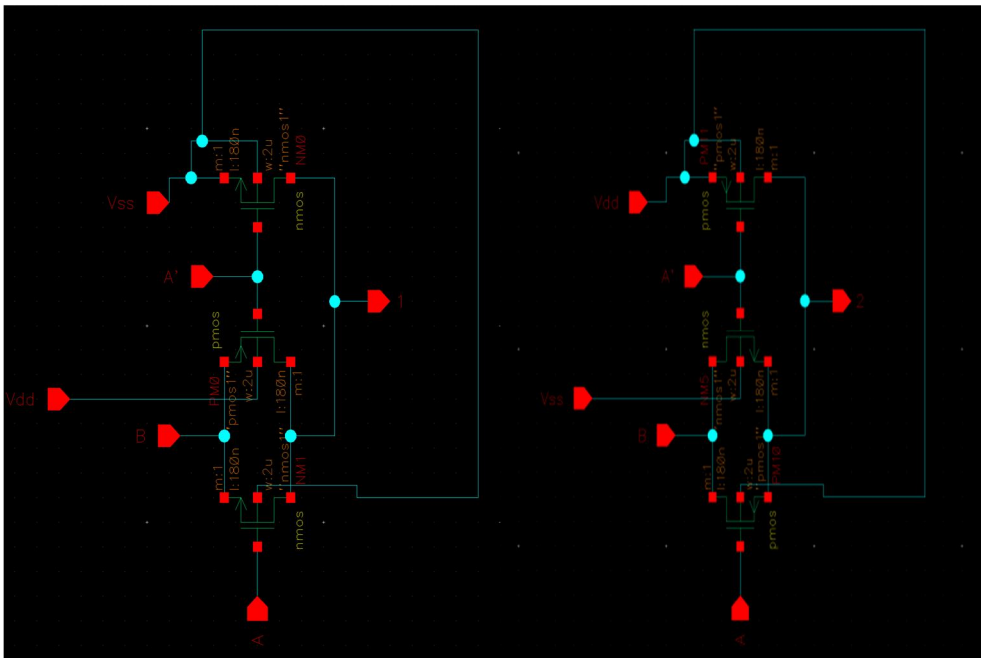


Fig.5. TGL AND Fig.6. TGL OR

D. Mixed Logic Design

In this mixed logic design technique combines the CMOS, PTL, and DVL logics to achieve the low operating power, low power dissipation, minimal die area, and high performance. In the proposed design uses mostly transmission gate logic and CMOS technologies to achieve the fundamental digital logic gates and 14-transistors low power and low power inverted designs,15-transistors high power and high-power inverted designs to get the 2 to 4 decoders.

14-Transistor Low Power Topology For 2-4 Decoder Design of a mixed logic 2-4 decoder would require two inverters and four TGL or DVL AND /OR gates with a total of 16 transistors. However, using both TGL and DVL AND gates in the same design and by select proper control and propagate signals, one of the two inverters can be eliminated resulting in a 14-transistor decoder topology. Consider two inputs of the decoder as A and B which generates 4 minterms D0-D3. With an aim of eliminating inverter B. The first minterm D0(A'B') and third minterm D2(AB') are implemented using DVL AND gates with A and B as the propagate signals respectively. The minterms D1(A'B) and D3(AB) are implemented using TGL AND gate with B as the propagate signal for both minterms. With this selection of gates and inputs it is possible to eliminate B inverter resulting in 14 transistor decoder topologies. Similarly, an inverting 2-4 decoder can be implemented using 14-transistor topology with 4 TGL/DVL OR gates and one inverter. TGL OR gates are used for implementation of minterms I0 and I2 with input B as the propagate signal, and DVL OR gates are used for implementing I1 and I3 with input A as the propagate signal. The two new low power decoder topologies implemented in this section are named as '2-4 LP' and '2-4 LPI', where LP stands for Low Power and I for Inverting. There schematics as shown in Fig. 7(a) and Fig. 7(b) respectively.

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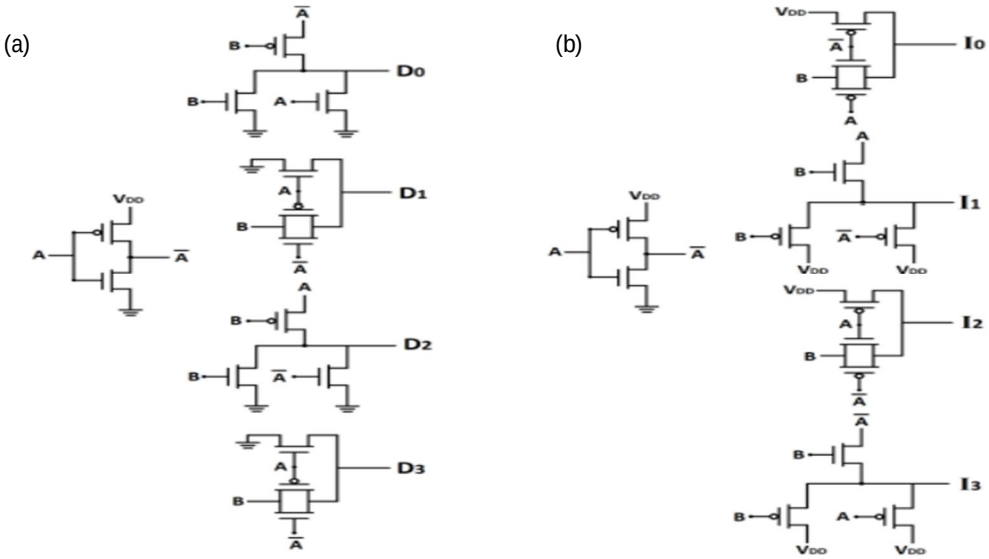


Fig.7: 15-transistor 2-4 line decoders: (a) 2-4LP (b) 2-4LP

15-Transistor High Performance Topology For 2-4 Decoder The drawback of 14 transistor low power decoder topologies presented above is the worst-case delay due to the complementary propagate signal used in minterms D0 and I3. It is possible to overcome this drawback by implementing these minterms using standard CMOS logic gates as they do not need complementary inputs. CMOS NOR gate is used to implement minterm D0 and I3 is implemented using CMOS NAND gate, with addition of one extra transistor in each topology. With this modification, the resulting decoder topology has 3 types of logic (CMOS. TGL, DVL) in the same circuit providing improvement in both power and delay performance, hence it is named as High Performance (HP) topology. The schematics of 2-4 HP and 2-4 HPI decoders are as shown in Fig. 8(a) and Fig. 8(b), respectively.

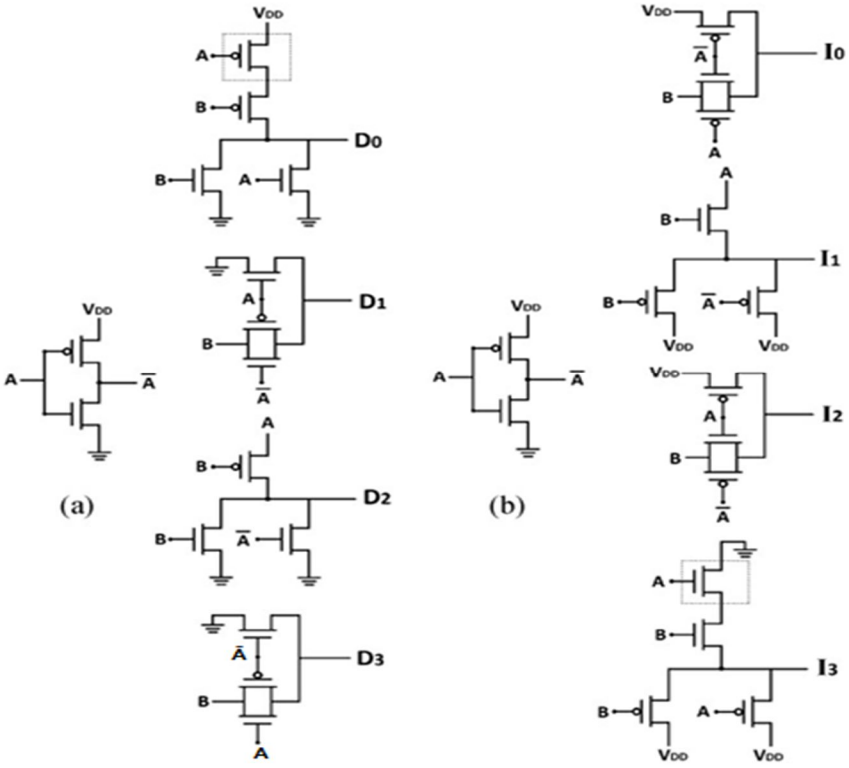


Fig 8: 15-transistor 2-4 decoders: (a) 2-4 HP, (b) 2-4 HPI

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III. DESIGN IMPLEMENTATION

Mixed logic 2-4 line decoders are designed using the Cadence Tools under 90nm technology to draw the Low power, Low power Inverting, High Power and High Power Inverting decoders.

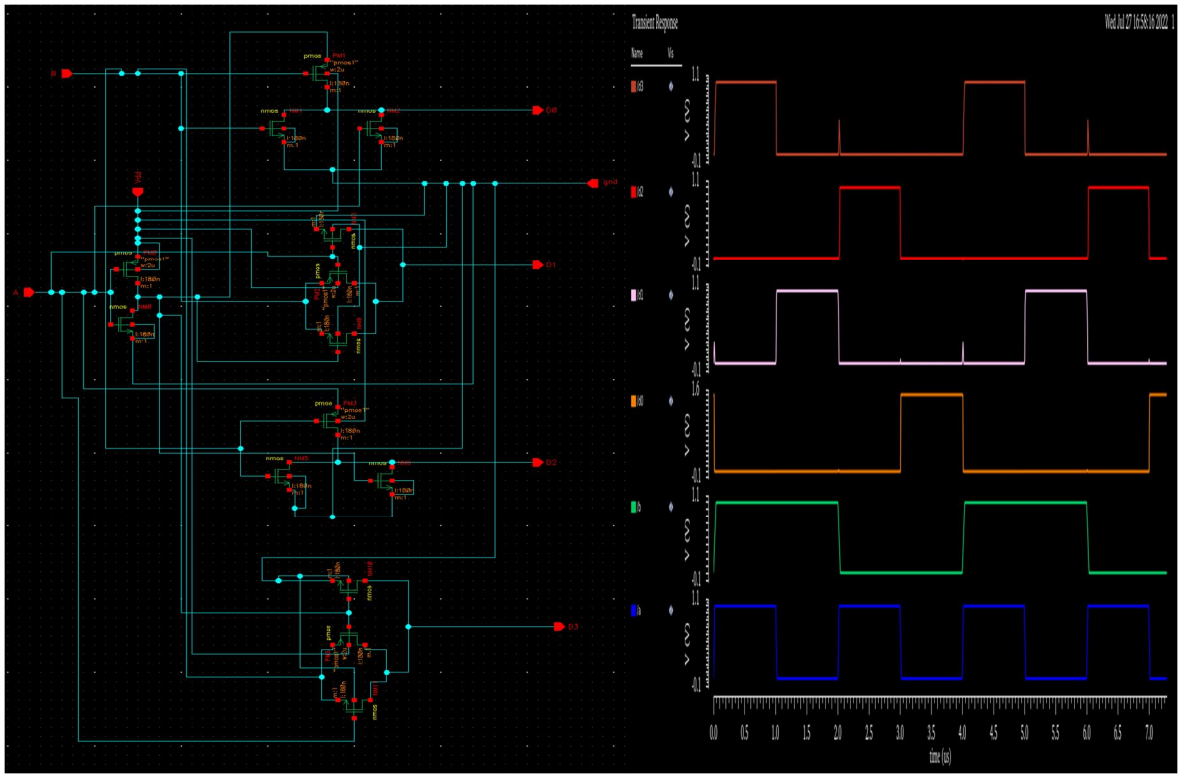


Fig.9: 14-transistor 2-4 LP decoders: (a) Schematic design (b) transient result

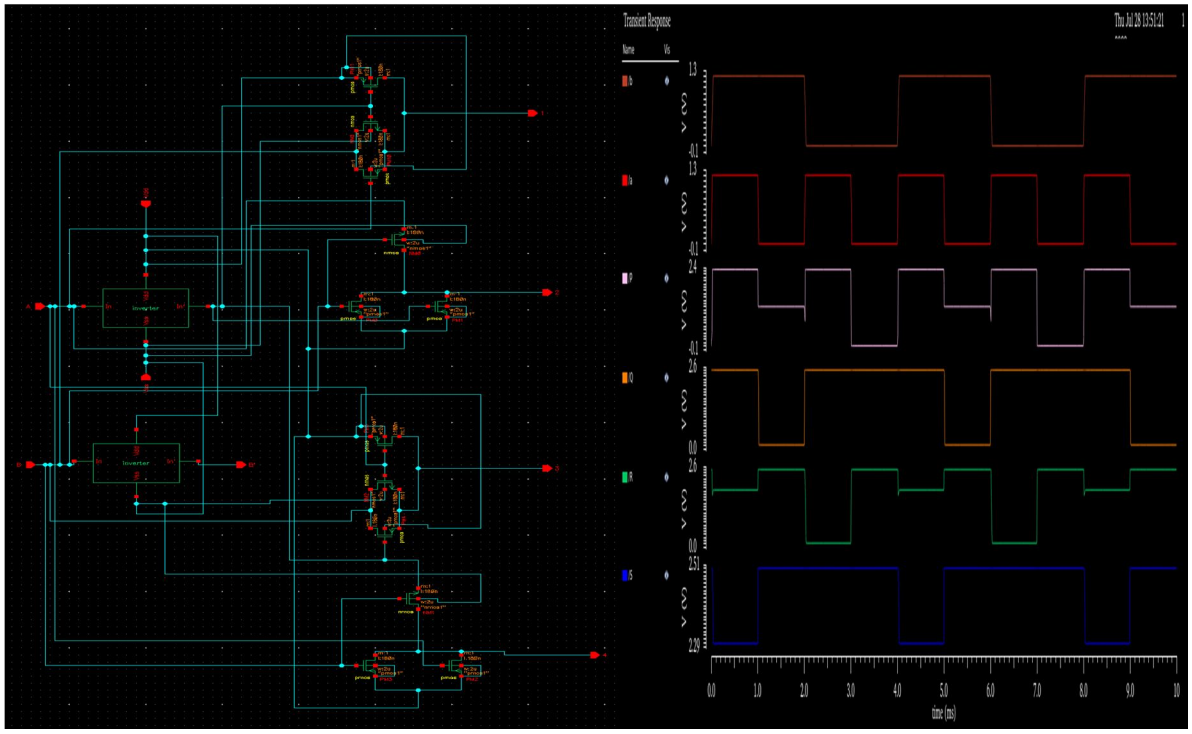


Fig.10: 15-transistor 2-4 LPI decoders: (a) Schematic design (b) transient result

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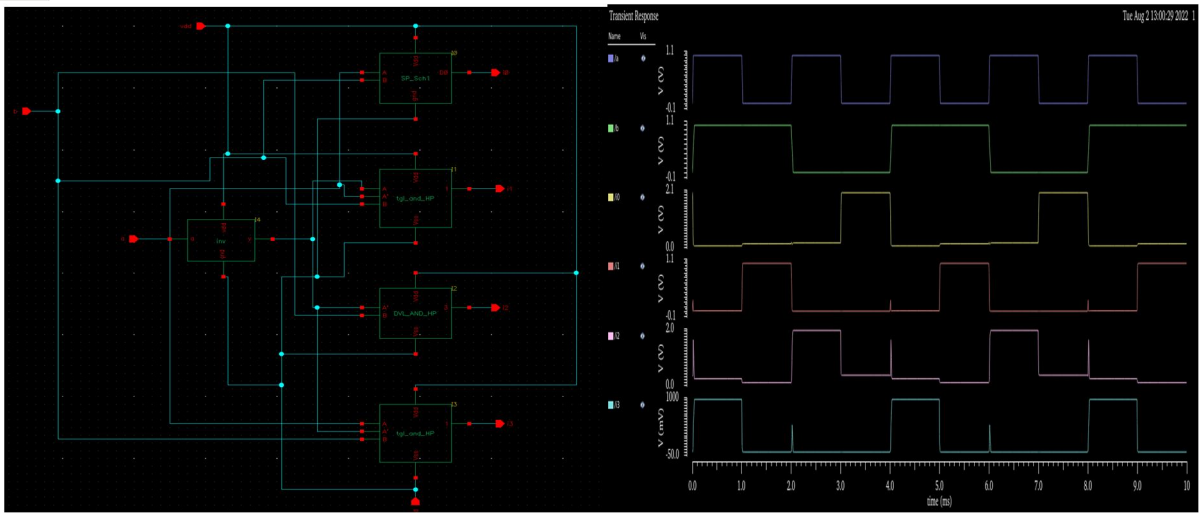


Fig.11: 14-transistor 2-4 HP decoders: (a) Schematic design (b) transient result

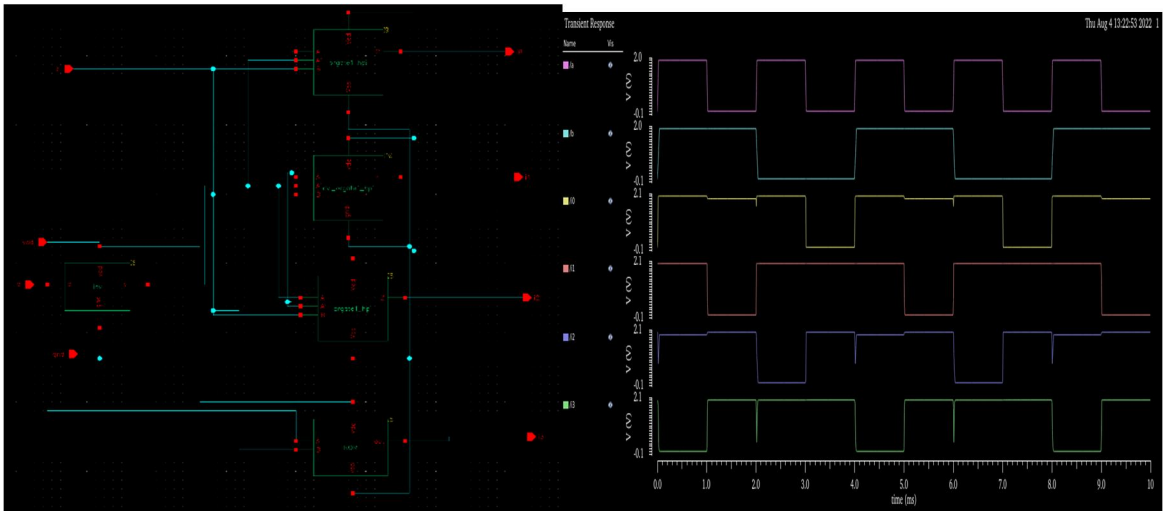


Fig.12: 15-transistor 2-4 HPI decoders: (a) Schematic design (b) transient result

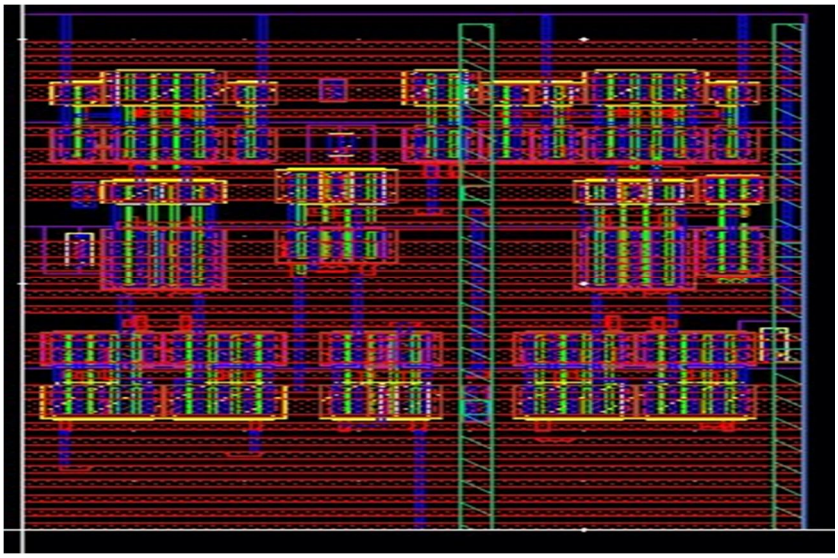


Fig.13: Layout of 2-4 decoders

TABLE III : PARAMETER DETAILS

Designs	Voltages(V)		Pulse width (ms)		Supply voltage (Vdd) in V
	A	B	A	B	
2-4 DECODER CONVENTIONAL CMOS	1.5	1.5	2	4	2.5
2-4 LP DECODER	1	1	2	4	2.5
2-4 HP DECODER	1	1	2	4	2
2-4 HPI CMOS DECODER	1.9	1.9	2	4	2
2-4 LPI DECODER	1.2	1.2	2	4	2.5

TABLE IV : COMPARISON OF PARAMETERS

Designs	Power (uW)	Propagation Delay (ns)
2-4 DECODER CONVENTIONAL CMOS	21.27	79.62
2-4 LP DECODER	12.47	38.1
2-4 HP DECODER	13.5	42.5
2-4 LPI DECODER	24.78	48.37
2-4 HPI DECODER	25.9	50.1

IV. CONCLUSION

By using Mixed Logic Line methodology, we developed four 2–4 line decoder topologies, namely 2–4 LP, 2–4 LPI, 2–4 HP and 2–4 HPI, which offer reduced transistor count and improved power delay performance in relation to conventional CMOS decoders. All the circuits are designed using a DSCH tool and layout using Micro wind Software EDA Tool and simulated using built-in Mix-Signal simulator and analyzed further for DRC in CMOS 180nm Technology.

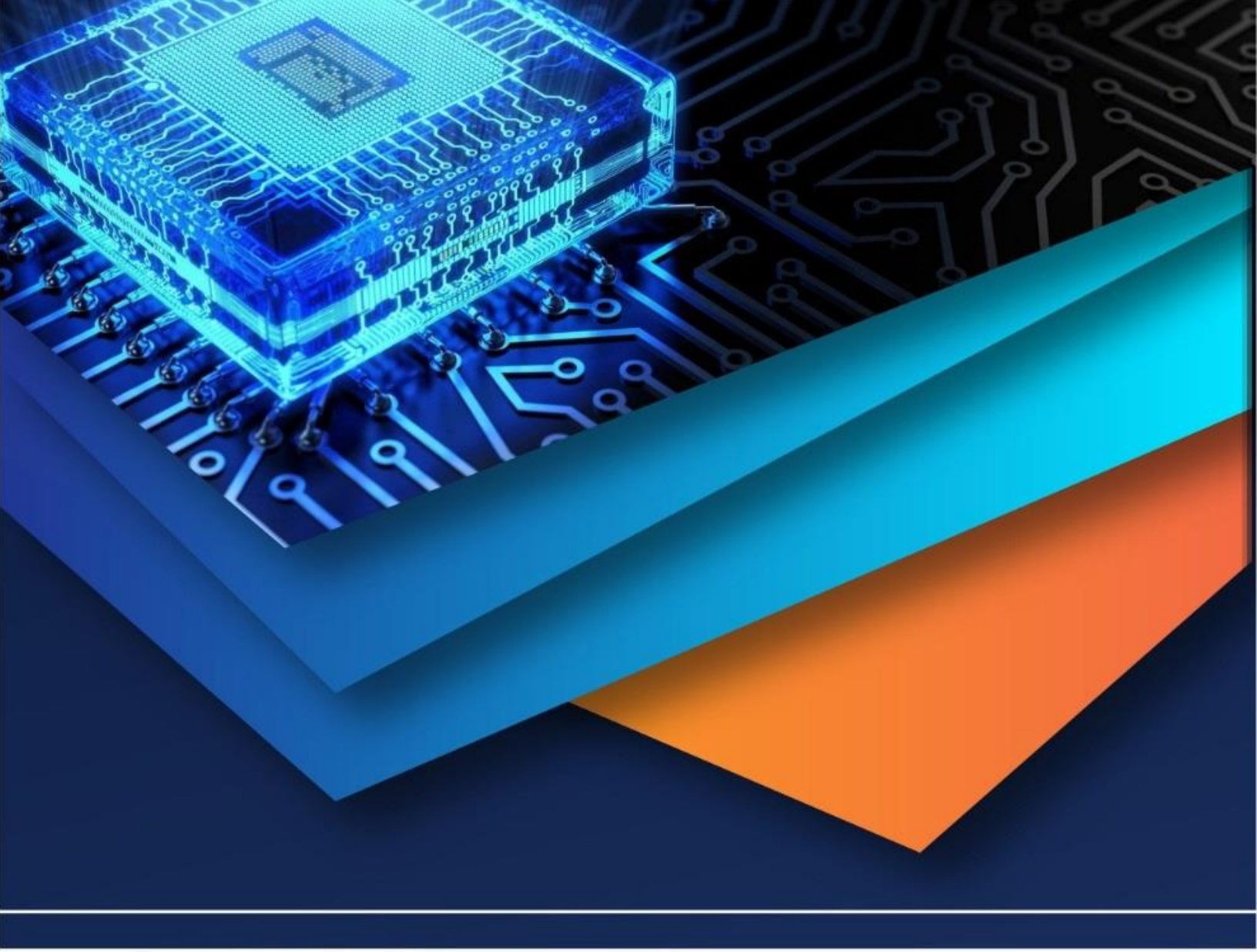
The main feature of this project is to optimize the decoder designs in order to achieve better speed and power performance. This work can be extended by using various mixed design styles like DVL, gating technique etc. in this we can obtain better results than CMOS logic where the power consumption and transistor count can be reduced. By this way can obtain less power consumption and high-performance operation when compared to CMOS logic design technique. The Higher input /output Decoders can be extended to further by drawing Physical Layout and these Decoders can be used in Audio Frequency Applications like used at receiver end to decode the audio signal. We can use these decoders in the applications where low power consumption and decoding is necessary such as Generally, these decoders are frequently used in communication systems like telecommunications, networking and transfer of data from one end to another end.

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