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Low Power Digital Image Compression Using Approximate Adders

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Abstract: ***Low power is one of the arising trend in field of VLSI which can be used in multimedia bias employing colorful signal processing algorithms and armature. In utmost multimedia operation mortal beings can gather useful information from incorrect afFull Adderir. Thus we don't need to produce an exact correct numerical afFull Adderir. So we're using different adders to apply this algorithm in signal processing. We design infrastructures for videotape and image contraction algorithms using the proposed approximate computation units and estimate them to demonstrate the efficiency of our approach. We also decide simple fine models for error and power consumption of these approximate adders. The approximate adders are reduced with complexity which are used in designing this algorithm. The proposed adders can achieve significant through afFull Adderir and total power reduction over conventional adders. Simulation results indicate up to 69% power savings using the proposed approximate adders, when compared to being executions using accurate adders.***
Keywords: Approximate Computing, Adder Design, Low Power, Mirror Adder.

I. INTRODUCTION

The digital signal processing(DSP) blocks is the backbone of multimedia operation which is used in movable bias. Ultimate of the DSP blocks apply the signal in image and videotape processing algorithm where the ultimate afFull Adderir is either as an image or videotape for mortal consumption. mortal beings have limited perceptual capacities when interpreting an image or a videotape. We can use this freedom to come with low power design at different position of design abstraction videlicet sense, armature and algorithm. The paradigm of approximate co putting is a specific to opt a particular attack performance of DSP blocks. It's known that bedded signal instruction reduced to a set of calculating processor which consumes about 70 of energy in supplying data and instruction and 6 of energy while performing computation. The programmable processors are designed for general purpose operation with no operation specific specialization.

thus we consider operation-specific intertwined circuit performance of error-flexible operation like image and videotape contraction former work on sense complexity reduction which have to be concentrated on algorithm, sense and gate position. We propose a sense complexity reduction at transistor position. The simplified computation units which give an spare estate of power savings over conventional low power design ways. This is attributed to the reduced sense complexity of proposed approximate computation units. We propose a measure of quality of DSP blocks that as an approximate adders. We also propose a methodology that can be used to harness the maximum power savings using approximate adders, subdued to a maximum power savings using approximate adder.

The proposed system methodologies of sense complexity reduction at transistors position as an necessary approach to approximate computing for DSP operations. To simplify the complexity the conventional MA cell by reducing the number of transistor and internal knot capacitance to insure the minimum crimes in Full Adders(FULL ADDER) verity table. The simplified interpretation of FULL ADDER cell to propose several squishy or approximate multi- bit adders that can be used as a structure blocks of DSP system. The Vos is a truly popular ways to get advancements in power consumption. still V_{os} will lead to detention Full Adderilure in MSB bits. This might leads to large afFull Adderir quality of operation.

The design for image and videotape contraction algorithm using proposed approximate computation units to estimate the approximate armature in terms of afFull Adderir quality and power dispersion. The fine description of afFull Adderir quality of DSP blocks uses approximate adders to propose a simple fine models for estimating the degree of voltage scaling and power consumption of approximate adders. The optimization methodology with help of Discrete Cosine Transform(DCT) and Finite Impulse Response(FIR) sludge.

II. LITERATURE REVIEW

Padmanabhan Balasubramanian etal.,(2021) has proposed the new approximate adder that's design- optimized and optimized error criteria . Optimization in design which translates into optimization of the design parameters similar as detention, power, and area/ coffers, and optimization of the error criteria points to the utility of the proposed approximate adder for practical operations.

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The proposed approximate adder that's tackle optimized the perpetration of approximate adders is grounded on ASIC and FPGA design. We used a Xilinx Artix- 7 device for a FPGA perpetration. To demonstrate the practical mileage, we consider a digital image processing as a practical operation and trial with numerous images. The quality of the images reconstructed using the approximate adders was anatomized which is grounded on the peak signal- to- noise rate(PSNR), which is used as a qualitative figure- of- merit to assess the images
[1].

Seyed ErFull Addern Full Addertemieh et al.,[2020] has proposed that the full adders are the main block in digital arithmetic as Multipliers, subtractors, and dividers use these blocks as the fundamental part. Approximate computing is a promising method for designing low-power and Full Adderst digital circuits, which are applicable in error resilient applications such as image processing. In this paper, the current mode logic (CML) approximate full adder are proposed. Circuit-level simulation is performed by HSPICE applying 32nm Carbon Nanotube Field Effect Transistor (CNTFET). The analysis shows that the proposed circuit's power consumption and delay are highly acceptable, while its error distance (ED) is minimum. The application-level simulation shows that the full adder's peak signal to noise ratio (PSNR) and structural similarity index (SSIM) are the highest among the previous CML approximate full adders [2].

Krishna Sravani Nandam et al.,[2020] has proposed the CSL (Carry Select) adder which is one the best adders to perform the adequate arithmetic operations for several architectures. The structure of the CSL adder is so significant that tends to decrease the area, delay and power usage. The CSL adder structure is that the area, delay and power consumption will be further minimized and it has the ability to vary between the approximate and exact modes of the operation. In CSL adder the area, delay and power are reduced with quick and successful gate-level adjustments. Multiplier is used as an essential component in digital signal processing to perform the arithmetic operations. The dual mode can provide a multiplier with an efficient utilization, where the accuracy can change significantly during execution. The Dynamic Accuracy Configurable Multiplier is used in contrast approximate multiplier which provides a lower delay and higher power accuracy. The parameter result indicates low power delay, higher power consumption and high speed [3].

Mohammad Saeed Ansari etal.,(2019) has proposed the squaring function which is extensively used in Digital Signal Processing(DSP). There are numerous DSP operations with noisy inputs for simplifying approximations of the squaring function perpetration which have a minor impact on the afFull Adderir quality, while permitting the significant reductions in the tackle. This composition proposes a Low- Error Squaring Function(LESF) and its low- power tackle perpetration. The simulation results show that the 16-bit LESF has23.23 further accurate(in the mean relative error distance) than the birth Mitchell approximate logarithmic squaring function. LESF and other logarithmic squaring functions are estimated for the square- law sensor operation [4].

Raunaq Nayar et al.,(2019) has proposed the tackle optimized approximate adder that has virtually zero average error(i.e.) a Gaussian error distribution. The proposed approximate adder which is expanded as tackle optimized approximate adder with a normal error distribution. We considered the use of digital image processing with the accurate adder and numerous other approximate adders for a practical analysis. The additions are involved in performing Full Adderst Fourier Transform and inverse Full Adderst Fourier Transform which operations to reconstruct the images are enforced using accurate and approximate adders independently. The observation is grounded on physical design perpetration using a 32/ 28nm CMOS standard digital cell library [5].

Chunmei Yang et al.,(2019) has proposed the Approximate computing which are lately surFull Adderced as a promising paradigm to achieve considerable energy savings at the expenditure of demoralized computing delicacy. In this paper, an approximate adder is proposed to reduce the power consumption while furnishing minimum calculation crimes for circle accumulation, which is a pivotal operation in colorful signal processing algorithms. The proposed adder is grounded on smart revision of Karnaugh chart to induce a compensation effect of circle accumulation. In proposed approximate adder, the power consumption is reduced by over to42.8 and24.9 when compared to completely-accurate adder and the preliminarily published approximate adders, independently, in an artificial 65- nm CMOS technology. By using the product of regularized mean error distance(NMED) and power consumption as the Figure- of- Merit(FoM), the proposed approximate adder improves the FoM up to37.7 x when compared to the preliminarily published approximate adders [6].

HonglanJiangetal.,(2018) has proposed the Approximate circuits which has been considered for multitudinous operations that can tolerate some loss of delicacy with bettered performance and energy effectiveness. Multipliers are vital calculation circuits in multitudinous of these operations including digital signal processing (DSP). In This multiplier leverages a lately designed approximate adder that limits its carry propagation to the nearest neighbors for Full Adderst partial product accumulation. Both AM1 and AM2 have a low mean error distance,(i.e.) ultimate of these crimes are not significant in magnitude. When compared to

Wallace multiplier which is optimized for speed, an 8 × 8 AM1 which uses four MSB for error reduction which is of about 60.(when optimized for detention) and a 42 of reduction in power dissipation(when optimized for area) [7].

Masoud PashaeiFull Adderr et.al (2018) has proposed the a frame for analytically estimating the afFull Adderir quality of common digital signal processing(DSP) blocks that use approximate adders. The afFull Adderir rates of DSP blocks, analogous as finite impulse response sludge, separate cosine Transform, and Full Adderst Fourier Transform, which utilizes the approximate adders. The delicacy of the proposed frame is estimated by comparing fine model prognostications to simulation results by using the signal-to- noise rate(SNR) metric. The trip of the SNR is predicted by the frame on average, lower than2.5 dB when compared with attained simulations. therefore, a fine model optimization approach is rested on Lagrange Multipliers for optimizing design parameters. The optimization is realized by choosing a proper configuration of the target block, analogous as determining the data range of inexact computation part for each approximate adder in the design [8].

Nivya Rose Varghese etal.,(2018) has proposed numerous operations similar as image processing and multipliers which are flexible to inexactness or approximations in their underpinning calculations. The performing declination of afFull Adderir quality can be traded off to develop further energy effective and high performance of tackle systems. numerous operations similar as signal processing and image processing requires the use of multipliers in its core operating system. The abecedarian ideal of a multiplier is that it must be effective in power and operate at high speed. A radix 4 approximate cell multiplier operation is proposed in this paper which has significant enhancement in power, speed and delicacy when compared to the earlier approaches in approximate cell multipliers. The comparison is performed with the conventional radix 4 cell multiplier and there's a 72 and 17 reduction in power and detention independently [9].

S.Thava Bala etal.,(2018) has proposed the complexity of VLSI design circuits which has increased dramatically. The common known Full Adderct is that multiplier circuit plays an important part in the digital signal processor design,currently, low power and low area multiplier designs are in high demand when compared to other multipliers, Wallace tree multipliers are considered to be Full Adderst rather than other multipliers. For performing the process of addition, there will be numerous stages in- between and those stages are to be enforced using fresh gate circuits. The operation of fresh circuits will eventually affect in increased area which in turn increases the power consumption also. To overcome these disadvantages, Approximate Wallace Tree Multiplier is enforced using deficient adder cell(ICAC) and Accurate Compressor with Cin and Cout ignored circuits. It's set up out that it reduces the area when compared to normal Wallace Tree Multiplier Design. Then, another system for Approximate Wallace multiplier using 42 compressors is proposed to keep the area over minimum. This system uses four to two compressors for addition and this circuit is used in the Approximate Wallace Tree Multiplier. The below designs are synthesized by Synopsys, the power consumed and area is enthralled by both the styles which is compared. By comparing, this multiplier the compressor minimizes the area by98.39 when compared to Approximate Multiplier which also reduces the power consumption by98.13% [10].

Morteza Rezaalipour et al.,(2017) has proposed the Moore's Law scaling tapers by growing the emphasis on improving the energy-efficiency of nanometer ICs through architectural techniques. Recently, the approximate computing has been introduced to address the energy-efficiency problems of error tolerant applications in all forms of computing from mobile IoT devices to datacenters and servers. This technique has been proved successful in various application domains such as digital signal processing, deep machine learning, and combinational optimization. Approximate computing trades is accuracy for power, delay, and area in computing systems. Adders consume significant amounts of system energy and occupy large portions of the processor area. The need for low power and high-speed circuits as well as the error-resiliency of the digital signal processing systems allow the system designers to innovate the energy-efficient approximate adders. This paper examines, a design remedy for approximation, which provides an automatic method to improve the accuracy of an approximate adders with virtually no impact on their power and area consumption. The proposed method is applied to seven state of approximate adders for evaluation; our simulation results indicate 12-50% accuracy regarding mean error distance metric improvements are attainable for the baseline approximate adders using the proposed design approach [11].

Arghavan Mohammad Hassani etal.,(2017) has proposed the low power consumption, currently, it has surFull Adderced to be an necessary Full Adderctor as there's a growing demand for designing effective calculation- ferocious systems and integrating further transistors on chips. The trade- off between area, detention, power consumption, and delicacy, approximate computing has come a promising result to address the power effectiveness problem for error-tolerant operations similar as digital signal processing. To achieve high inflexibility and lower Full Adderult circumstance when using approximate calculation, reconfigurable addition can be salutary by furnishing different modes of approximate and accurate operations inmulti-bit adder circuits. In this paper, we propose a 16- bit transistor to accurate full adder design grounded on a 10- transistor full adder for which the threshold has been reduced to increase the afFull Adderir voltage swing.

This 16 bit transistor full adder is birth for the Full Adderrther proposed configurable bimodal design, which functions as a Lower part of adder (LOA) in the approximate mode. The approximate mode, consumes about 53 lower power than LOA adder. Also, in this accurate mode, the power consumption is reduced by 12 when compared to its birth of 16 bit transistor accurate design [12].

Ashim Gogoi etal.,(2016) has proposed the digital signal processing(DSP) operations like image processing and speech processing, mortal beings can collect useful information from slightly inexact labors. This type of computing is appertained as an inexact computing which doesn't provides an exact correct numerical labors. Approximate circuits consume lower power, which bear lower number of transistors and have lower propagation detention than exact circuits. Approximate adder is the structure block of inexact computing for DSP operations. This paper represents a design of a 32- Bit approximate adder which has low power consumption and requires lower number of transistors than being approximate adders. The proposed approximate adder has power savings of 8 for 32- Bit as when compared to being designs. The proposed adder has significant reduction in area (number of transistors) than being designs [13].

Vaibhav Gupta etal.,(2013) has proposed the low power which is an imperative demand for movable multimedia bias employing colorful signal processing algorithms and infrastructures. thus, we don't need to produce exactly correct numerical labors. former exploration in this environment exploits error resiliency primarily through voltageover-scaling, exercising algorithmic and architectural ways to alleviate the performing crimes. In this paper, we propose sense complexity reduction at the transistor position as an indispensable approach to take an advantage of the relaxation of numerical delicacy. We demonstrate this conception by proposing the colorful squishy or approximate full adder cells with reduced complexity at the transistor position, and use them to design approximatemulti-bit adders. We design infrastructures for videotape and image contraction algorithms by using the proposed approximate computation units and estimate them to demonstrate the effectiveness of our approach. We also decide simple fine models for error and power consumption of these approximate adders. Likewise, we demonstrate the mileage of these approximate adders in two digital signal processing infrastructures(separate cosine Transform and finite impulse response sludge) with specific quality of constraints. Simulation results indicates up to 69 of power savings using the proposed approximate adders, when compared to being executions using accurate adders [14].

Full Adderrzad Full Adderrshchi etal.,(2013) has proposed the low power multiplier in Digital Signal Processing. The proposed multiplier utilizes the Broken- Array Multiplier approximation system on the conventional modified Booth multiplier. This system reduces the total power consumption of multiplier up to 58 at the cost of drop in afFull Adderir delicacy. The proposed multiplier is compared with other approximate multipliers in terms of power consumption and delicacy. For better evaluation of the proposed multiplier effectiveness, it has been used in designing a 30- valve low- pass FIR sludge and the power consumption and delicacy are compared with that of a sludge with conventional cell multipliers [15].

III. BLOCK DIAGRAM

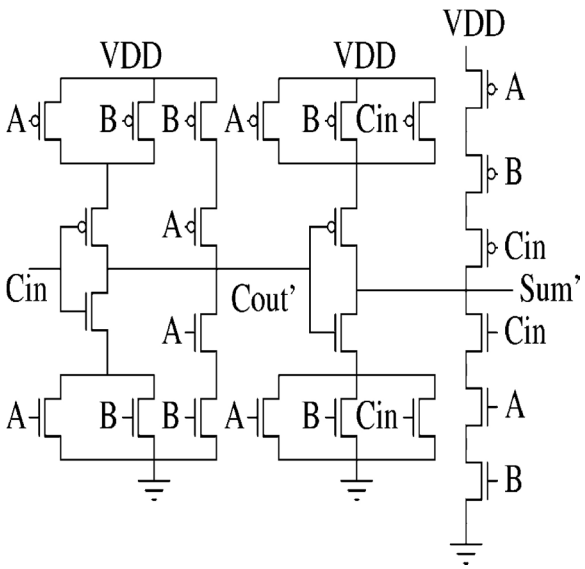
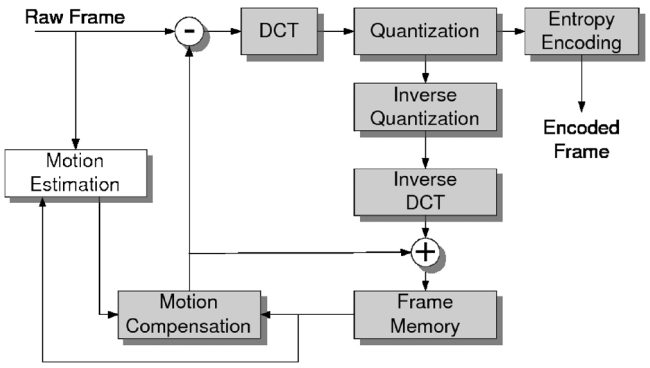


Fig.1 Block Diagram of Modified Approximate Adder

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IV. FLOW CHART



V. METHODOLOGY

A. Approximate Adders

Colorful approximate adders are preliminarily designed to reduce logical complexity and to reduce critical path for designing a digital approximate adder which cut the carry chain and therefore reduce the critical path detention. The perpetration of designing colorful approximate adders reduces the complexity in transistor position and reduces the critical path detention and power. Then the different methodologies for designing the approximate adders, we use RCA's and CSA's. Since the Mirror Adder is one of the extensively used provident executions of an FULL ADDER, we use it as our base for proposing different approximations of an FULL ADDER cell.

B. Implementation Of Approximate Adder

The Previous approximate adders have difficulty in detecting and correcting the errors since they are designed for error acceptable applications with target accuracy. However, accurate computations are still required at certain times, according to the application. VLSA can provide accurate results, but it has large delay and area overhead for the error detection and correction. The central contribution of the work is to propose an approximate adder which supports both accurate and inaccurate computation with error-correction and accuracy-configuration capability. Figure.1 shows our proposed approximate circuit for the case of a 16-bit adder. In the adder, the carry chain is cut to reduce critical path delay, and three sub-adders generate results of partial summations. With the reduced critical-path delay, high performance (by increasing the clock frequency) or low power consumption (by decreasing the operating voltage) is obtained.

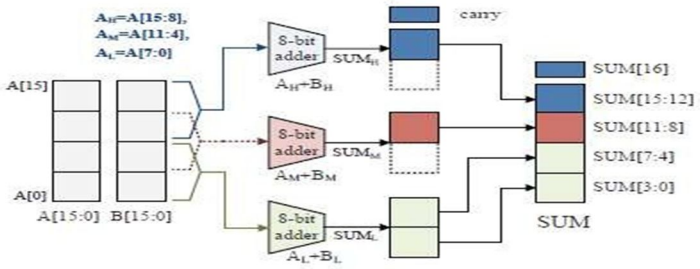


Fig.2: Proposed Approximate Adder 16- Bit Adder Case Delay

The former approximate adders have difficulty in detecting and correcting the crimes since they're designed for error respectable operations with target delicacy, still, accurate calculations are still needed at certain times, according to the operation. VLSA can give accurate results, but it has large detention and area above for the error discovery and correction. The central donation of the work is to propose A middle sub-adder (AM+BM) is introduced to increase delicacy. Without the middle sub-adder error occurs when the eighth carry bit is high, and the arbitrary input patterns the error rate is50.1. On the other hand, the pre-Full Adder of the middle sub-adder, error rate for arbitrary input patterns is reduced to5.5.(In the real perpetration, all spare corridor(four- LSB Full Adder is of AH BH and AM BM sub-adders) are optimized only for carry- generation.) We can generalize the perpetration of the proposed approximate adder. In the adder, each divided sub-module produces a k- bit result except for the last sub-module, which produces a 2k- bit result.

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C. Approximate Adders

In this methodology we're enforcing the approximate adders using glass adder sense. So we're removing the transistors from this adder and constructing approximate adders. We use RCA's and CSA's. Since the MA is one of the extensively used provident executions of an FULL ADDER, we use it as our base for proposing different approximations of an FULL ADDER cell.

Approximation strategies for the Conventional Mirror Adder

In this section, we explain step- by- step procedures for coming up with approximate MA cells with smaller transistors.

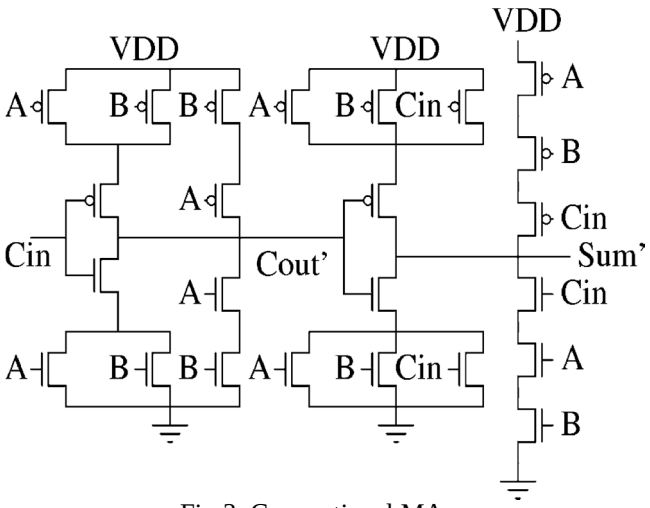


Fig.3: Conventional MA

The junking of some series connected transistors will grease briskly charging/ discharging of knot capacitances. also, the complexity reduction by junking of transistors also aids in reducing the αC term(switched capacitance) in the dynamic power expression as $P_{dynamic}$ = αCV2DDf

1) Approximation 1

In order to get an approximate Ma with lower transistors, we have to remove transistors from the conventional schematic bone by one. still, we can't do this in an arbitrary system. We need to make sure that any input combination of A, B and Cin does not affect in short circuits or open circuits in the simplified schematic. Another important criterion is that the performing simplification should introduce minimal crimes in the FULL ADDER verity table. A judicious selection of transistors is removed(icing no open or short circuits) results in a schematic shown inFig.3.2, fluently, this schematic has eight lower transistors when compared to the conventional MA schematic. In this case, there is one error in Cout and two crimes in Sum.

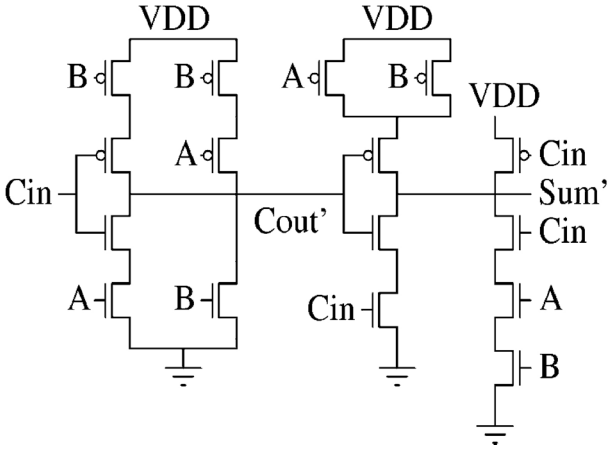


Fig.4: MA approximation 1.

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2) Approximation 2

The verity table of an FULL ADDER shows that Sum = Cout for six out of eight cases, except for the input combinations A = 0, B = 0, Cin = 0 and A = 1, B = 1, Cin = 1. Now, in the conventional MA, Cout is reckoned with the first stage. Therefore, the simplified schematic is to set Sum = Cout. still, we introduce a buffer stage after Cout to apply the same functionality. However, the total capacitance at the Sum knot would be a combination of four source- drain prolixity and two gate capacitances, If we set Sum = Cout as it's in the conventional MA. This is considerable as increased when compared to the conventional case or approximation 1. Then, Sum has only two crimes, while Cout is correct for all cases.

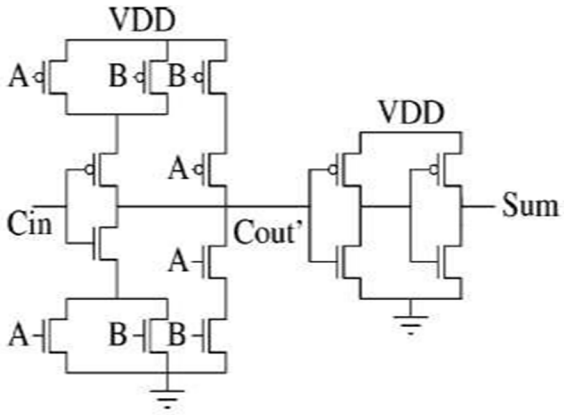


Fig.5: MA Approximation 2.

3) Approximation 3

Further simplification can be obtained by combining approximations 1 and 2. Note that this introduces one error in Cout and three errors in Sum.

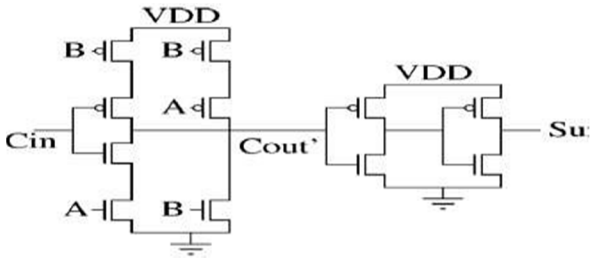


Fig.6: MA Approximation 3.

4) Approximation 4

The Full Adder varity table shows that Cout = A for six out of eight cases. also, Cout = B for six out of eight cases. Since A and B are exchangeable, we consider Cout = A. therefore, we propose a fourth approximation where an inverter with input A to calculate Cout and Sum is calculated analogous to approximation 1. This introduces two crimes in Cout and three crimes in Sum. In all these approximations, Cout is calculated by using an inverter with Cout as input.

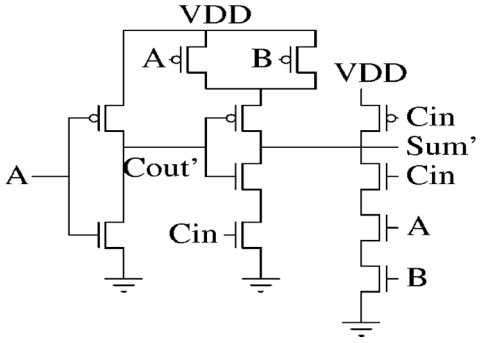


Fig.7: MA Approximate 4

Inputs			Accurate Outputs		Approximate Outputs							
A	*B*	C_{in}	Sum	C_{out}	Sum_1	C_{out1}	Sum_2	C_{out2}	Sum_3	C_{out3}	Sum_4	C_{out4}
0	0	0	0	0	0 ✓	0 ✓	1 ×	0 ✓	1 ×	0 ✓	0 ✓	0 ✓
0	0	1	1	0	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓
0	1	0	1	0	0 ×	1 ×	1 ✓	0 ✓	0 ×	1 ×	0 ×	0 ✓
0	1	1	0	1	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓	1 ×	0 ×
1	0	0	1	0	0 ×	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	0 ×	1 ×
1	0	1	0	1	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓
1	1	0	0	1	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓	0 ✓	1 ✓
1	1	1	1	1	1 ✓	1 ✓	0 ×	1 ✓	0 ×	1 ✓	1 ✓	1 ✓

Fig. 8 : Truth Table For Conventional Full Adder and Approximate Adder 1-4

VI. IMAGE COMPRESSION

In Approximate Adders, the approximate FULL ADDER cells were introduced. Using this approximate FULL ADDER cells we also introduces crimes in FULL ADDER. When approximate FULL ADDER cells are used to design multi-bit adders, the labors of these adders will be incorrect. Multimedia DSP algorithms substantially consists of additions and proliferations. Proliferations can be treated as shifts and adds. Thus, adders can be considered as introductory structure blocks for these algorithms. Atmost of the DSP algorithms are used in multimedia systems are characterized by essential error forbearance. Hence, occasional crimes in intermediate labors might not satisfy as a substantial reduction in the final Full Adder is quality. So we concentrate on image contraction algorithms, and present the results of using our approximate FULL ADDER cells in these algorithms.

A. Discrete Cosine Transform

The DCT and inverse separate cosine transform (IDCT) are integral Full Adder of a common Photographic Experts Group(JPEG) image contraction system. One- dimensional integer DCT y(k) for an eight- point sequence x(i) is given

$$y(k) = \sum_{i=0}^{7} a(k, i)x(i),\ k = 0,1, \ldots .7$$

Then, a(k, i) are cosine functions converted into original integers, The integer labors y(k) can also be right shifted to get the Full Adder actual DCT labors. analogous expression can be set up for 1- D integer IDCT. We alter the integer portions a(k, i), k = 1,..., 7 so that the addition a(k, i) x(i) is converted to two left shifts and an addition(using an RCA(Ripple carry adder). Since a(0, i) corresponds to the dc measure, which is most important, we leave it unaltered.

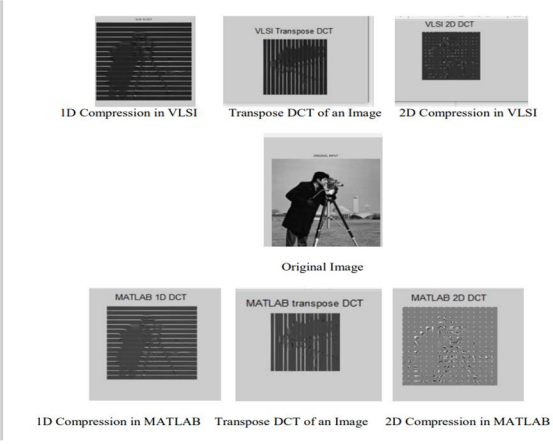


Fig.8: MATLAB Output of Modified Approximate Adders for Image Compression

This is done using a carry- save tree adder using a 42 compressor followed by an RCA. Also, each integer DCT and IDCT Full Adder is the sum of eight terms. Therefore, these labors are calculated using a carry- save tree system.

a changeable volume) the PSNR is expressed in terms of the logarithmic rattle scale. Using PSNR value for the same set of tests images, different image improvement algorithms can be compared totally to identify whether a particular algorithm produces better results. The confines of the correct image matrix and the confines of the degraded image matrix must be identical.

VII. RESULTS

The Low Power Digital Image Processing Using Approximate Adder is implemented in VHDL programming language, MATLAB and simulated. It has been synthesized. Power is reduced and image quality is maintained.

Power Summary	Conventional Approximate Adder		Modified Approximate Adder	
Power Consumption	I(mA)	P(mW) (45 mW)	I(mA)	P(mW) (40 mW)
Vdd(in) 1.8 V	21	38	19	34
Vcc(out)	2	7	2	7
Clock	6	12	5	9
Input	1	2	1	2
Logic	4	7	3	6
Quiescent Vdd(in)	10	18	10	18
Quiescent Vcc(out)	2	7	2	7

Fig.10. Comparison Table Power Accuracy in Conventional and Modified Approximate Adders

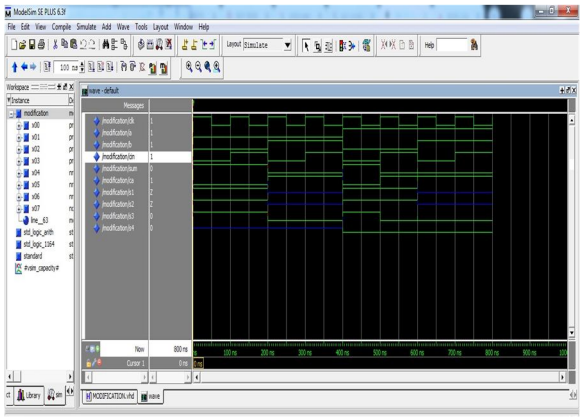


Fig.11. Waveform of Modified Approximate Adder using VHDL

VIII. CONCLUSION

Design of approximate adders, their error values and the complexity reduction are reduced. A separate cosine transform algorithm for image contraction is synthesized. The 2Dimensional separate cosine transform is applied on rows and columns ways to input image to get the converted values. Also image is reconstructed using inverse separate cosine Transform. Image quality is maintained.

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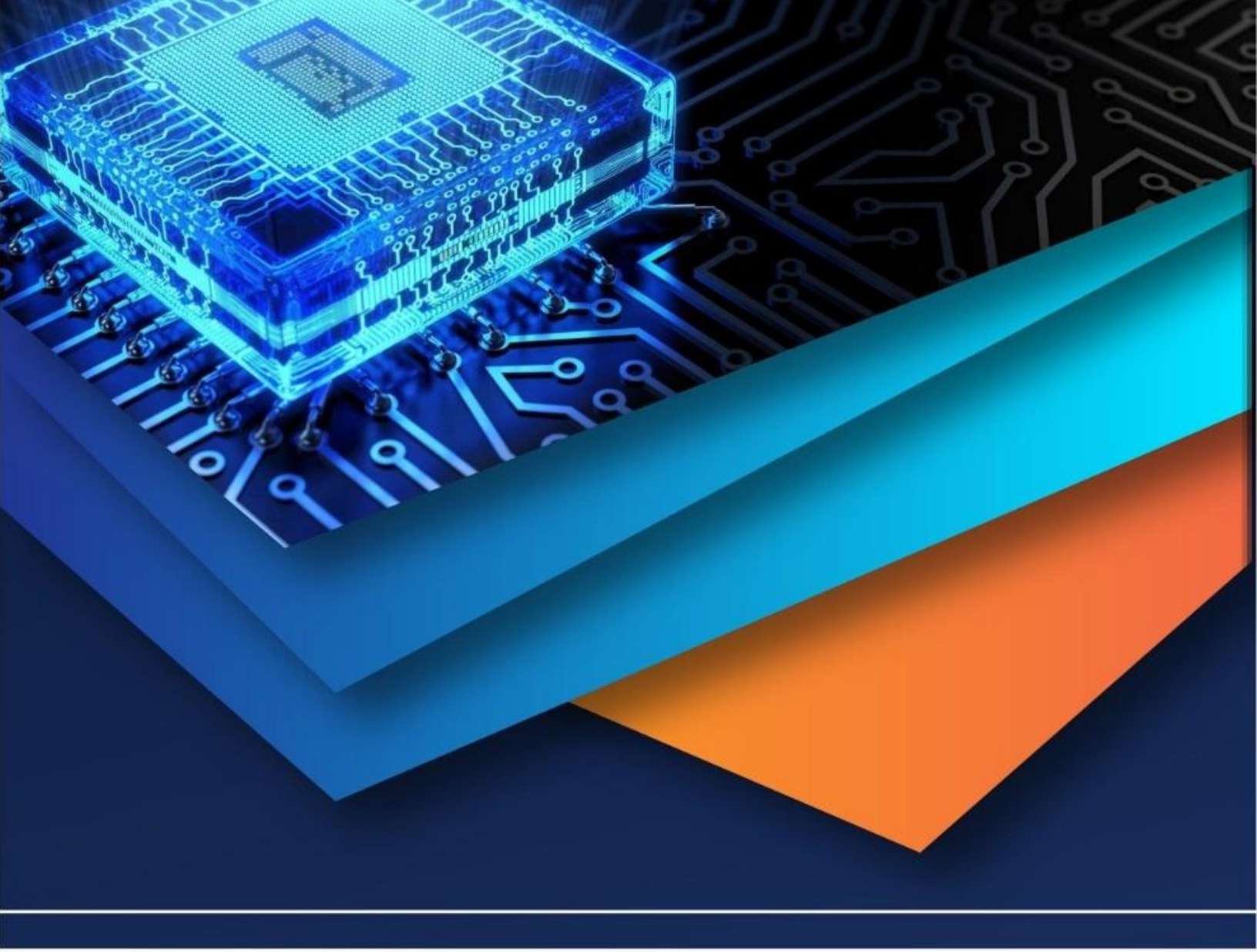
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