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A Low Power High Speed Accuracy Controllable Approximate Multiplier Design

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Abstract: ***For energy effective and high performance design, the low power VLSI circuit is used. Multiplier is an essential part of low power VLSI design, since the effectiveness of the digital signal processor depends upon the multiplier. In multiplier circuit, utmost of the power is dissipated across in full adder circuits. Multiplication is one of the important process in micro-processor and there will be a lot of delay because of array multiplier, which can be compressed with the help of the column compressor approach. It uses a selection of half adders, full adders and compressors to sum the partial products in stages until two numbers are left. An 8 * 8 and 16 * 16 bit multiplier design is executed by assigning the adder and compressor. Partial product totality is the speed limiting operation in multiplication due to the propagation detention in adder networks. In order to reduce the propagation detention, compressors are introduced. Compressors calculate the sum and carry at each position concurrently. The attendant carry is added with a advanced significant sum bit in the coming stage. This is continued until the final product is generated. The partial product tree of the multiplier is estimated by the proposed tree compressor (High Speed Compressor, Dual Stage Compressor, Exact Compressor).***

Keywords: Partial Products, Half Adder, Full Adder, High Speed Compressor, Dual Stage Compressor, Exact Compressor.

I. INTRODUCTION

Multiplication is the crucial computation operation which is extensively used in numerous microprocessors and digital signal processing operations. Microprocessors use multipliers within their computation reasoning units, and digital signal processing systems take multipliers to apply DSP algorithms similar as filtering.

Since the multiplier falsehoods directly within the critical path in utmost systems, the demand for high speed multiplier is continuously accelerating. Nevertheless, with the fast growing of movable computing tendency, the power consumption of the multiplier has come similarly important.

All this has responded in the pursuit of high speed low power multiplier design approaches. Previous to exploring the colorful multiplication algorithms, and the uses of each, it's imperative to present the essentiality of digital multiplication, and the standard title. Just as in the paper and pencil methodology of carrying a multiplication of two values, digital multiplication entails a sequence of additions carried out on partial products.

The means by which this partial product array is added to yield the final product is the crucial identifying factor amongst multiplication scheme.

II. LITERATURE SURVEY

K. C. Bickerstaff, E. E. Swartzlander, and M. J. Schulte [1] proposed a method on Analysis of column compression multipliers. The column compression technique reduces the delay in the circuit. Column compression multipliers are faster than array multipliers. The paper studies the area, delay and power characteristics of Dadda and Wallace multipliers and found that the ratios of power to area increases with operand word length due to longer interconnect lines and may also increase the chances of occurrence of fault.

C. Liu, J. Han, and F. Lombardi[7] published A Low-Power, High-Performance approximate multiplier with configurable partial error recovery. This multiplier uses a new type of approximate adder that limits the carry propogation to the nearest neighbor for quick partial product accumulation, because of this the power consumption reduces as the critical path is shorter. The proposed multiplier has high accuracy and low error, lower power consumption as compared to traditional Wallace multiplier.

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III. EXISTING SYSTEM

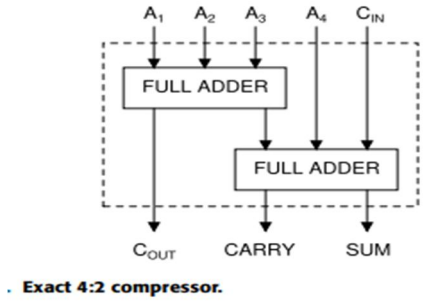
```
      0 0 1 0 1 1
      0 1 0 0 1 1
      0 0 1 0 1 1
    0 0 1 0 1 1
  0 0 0 0 0 0
0 0 0 0 0 0
0 0 1 0 1 1
0 0 1 1 0 1 0 0 0 1
```

Fig :1 Basic Multliplier Process

The multiplier multiplicates multiplicand therefore the paritial products are obtained.So the partial products are given to full adders to get the final result.By using full adder area and power will be more with high delay.

IV. PROPOSED SYSTEM

The column compacting approach reduces the detention in the circuit. Column compacting multipliers are briskly in nature than array multipliers. This paper studies Column compressor techniques for 8 * 8 bir and 16 * 16 bit multiplier.In 8 * 8 bit multiplier Exact Compressor is Used.



. **Exact 4:2 compressor.**

Fig :2 Exact Compressor

The general block diagram of an exact 4 : 2 compressor comprises of five inputs, three outputs and two cascaded full adders. A1, A2, A3, A4 and CIN are are the inputs and COUT , CARRY and SUM are the outputs of the exact 4:2 compressor.

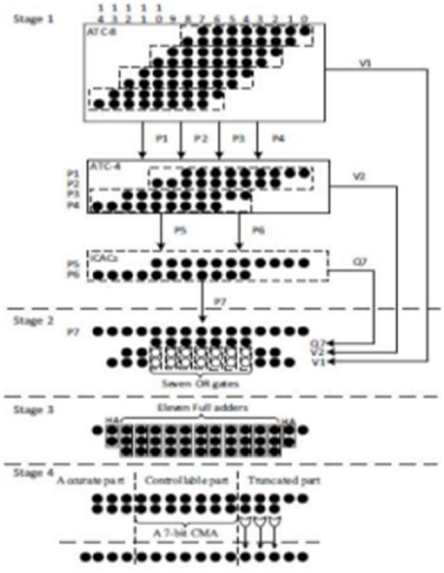


Fig : 3 Structure of 8*8 bit Multiplier

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A. Flow Charts

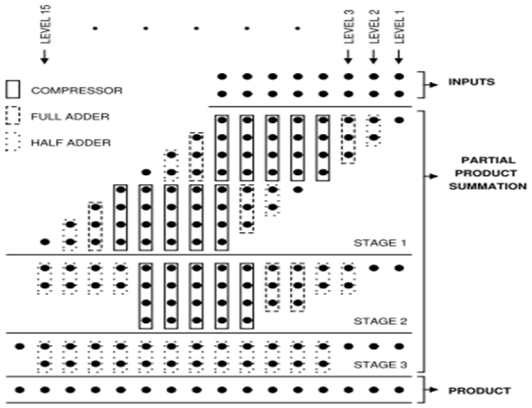


Fig:4 Flow chart for 8*8 bit multiplier

1) Multiply each bit of input1 by each bit of input2 , yielding results, grouped by weight in columns
2) Reduce the number of partial products by stages of full and half adders and compressors until we are left with at most two bits of each weight.
3) Add the final result with a conventional adder.

For 16*16 bit multiplier further two more compressors are used .Ther are High Speed Compressor and Dual stage Compressor

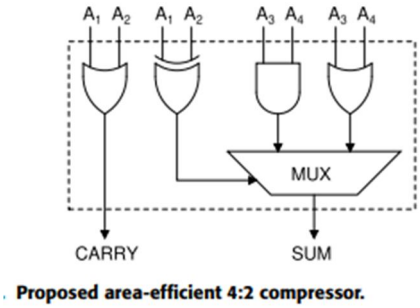


Fig:5 High Speed Compressor

The proposed high speed area-efficient 4:2 approximate compressor. The compressor inputs are A1, A2, A3 and A4, outputs are CARRY and SUM. In the high speed area-efficient compressor architecture apart from the MUX, one XOR, one AND & two OR gates are required. OR and gates each need 6 transistors in CMOS logic implementation.

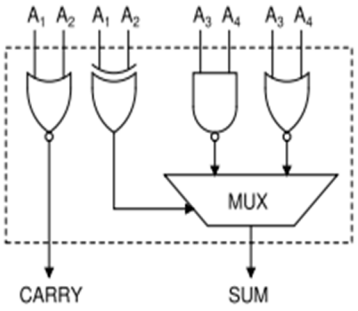


Fig:6 Dual Stage Compressor

In order to reduce the transistor count, this paper proposes an architecture with NAND and NOR gates (dual stage). The modified dual-stage 4 : 2 compressor reduces area, delay and power dissipation compared to the proposed high speed area-efficient 4 : 2compressor and other compressors in the literature due to the reduction in transistor count.

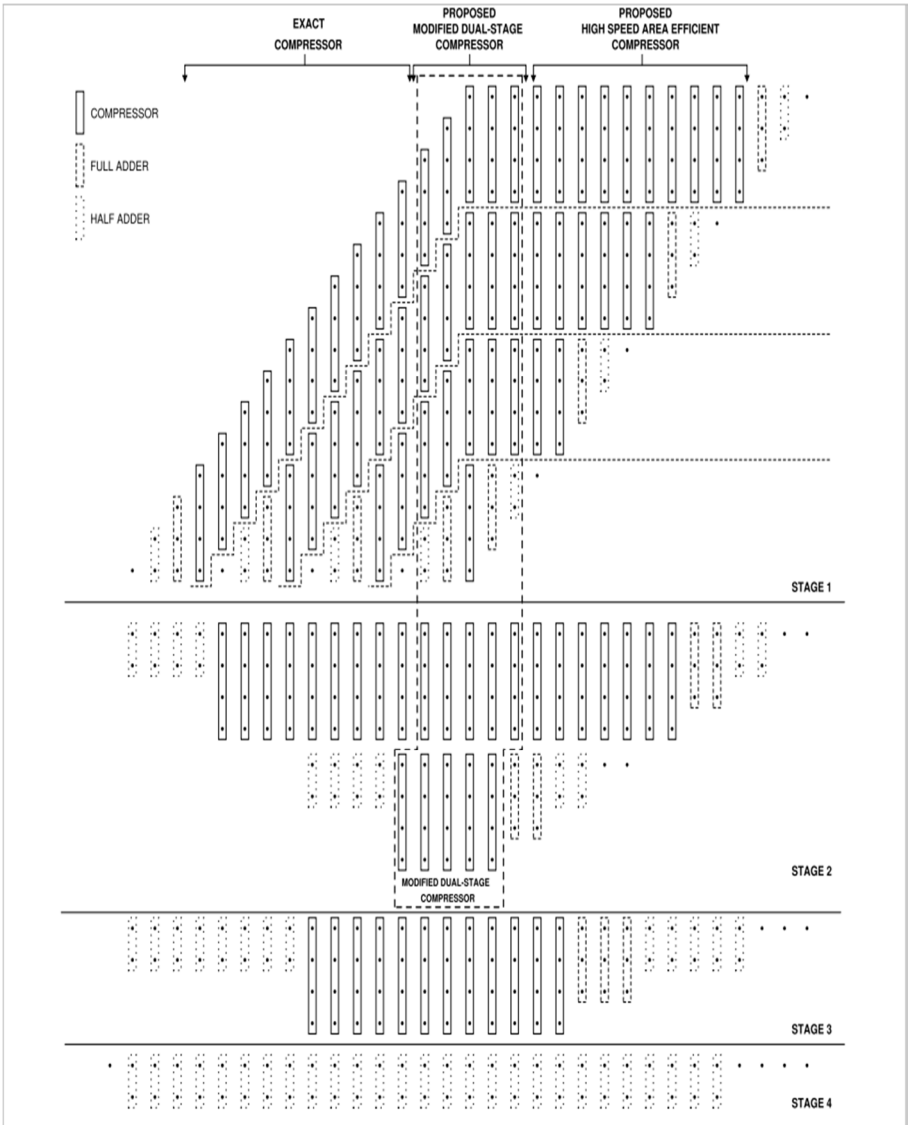
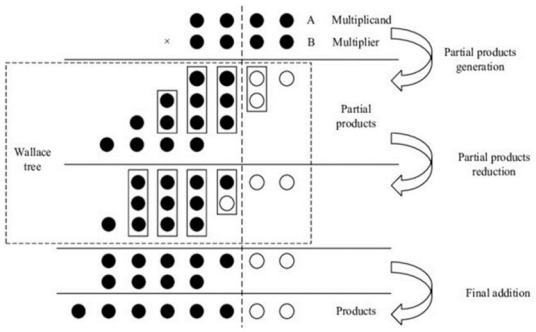


Fig:7 Flow chart for 16 * 16 multiplier

In the 16 × 16 bit multiplier, position 18 to position 32 employ exact compressors. The proposed modified dual- stage compressors are used where there are two stages of extended partial products for totality. For all other partial product positions lower than 17, proposed high speed area-effective 4 2 compressors, full adders .

Multiplication involves mainly 3 steps

- Partial product generation
- Partial product reduction
- Final addition



V. SIMULATION RESULTS

The 8 * 8 bit multiplier design and 16 * 16 bit multliplier design is simulated by using the tool Xilinx ISE(Integrated Synthesis Environment) and the results are shown in the below

A. Results

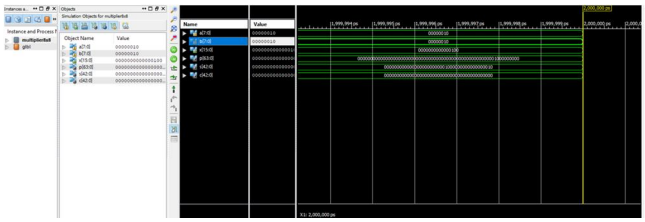


Fig:8 Outputs for 8 * 8 bit Multiplier

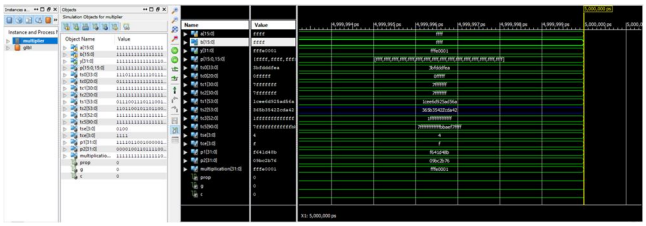


Fig:9 Outputs for 16 * 16 bit Multiplier

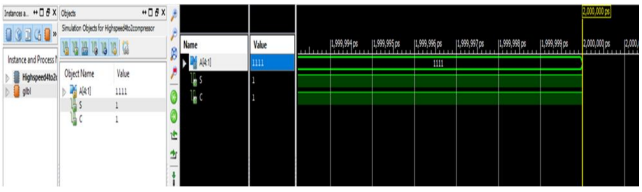


Fig:10 Output for sub module High speed 4 to 2 compressor

Fig:11 Output for sub module Dual stage compressor

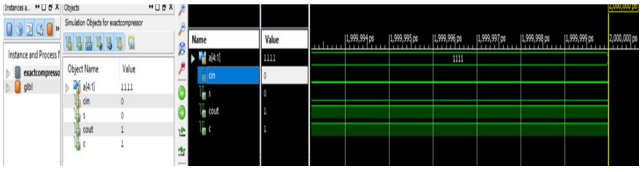


Fig 12 Output for exact compressor

VI. CONCLUSION

In this paper 8 * 8 bit and 16 * 16 bit multiplier is proposed .The 8 * 8 bit and 16 * 16 bit multiplier is simulated with the tool Xilinx ISE 14.7 and results are verified. Array multliplier produces more delay and this delay is reduced in column compressor technique due to Compressors Used.

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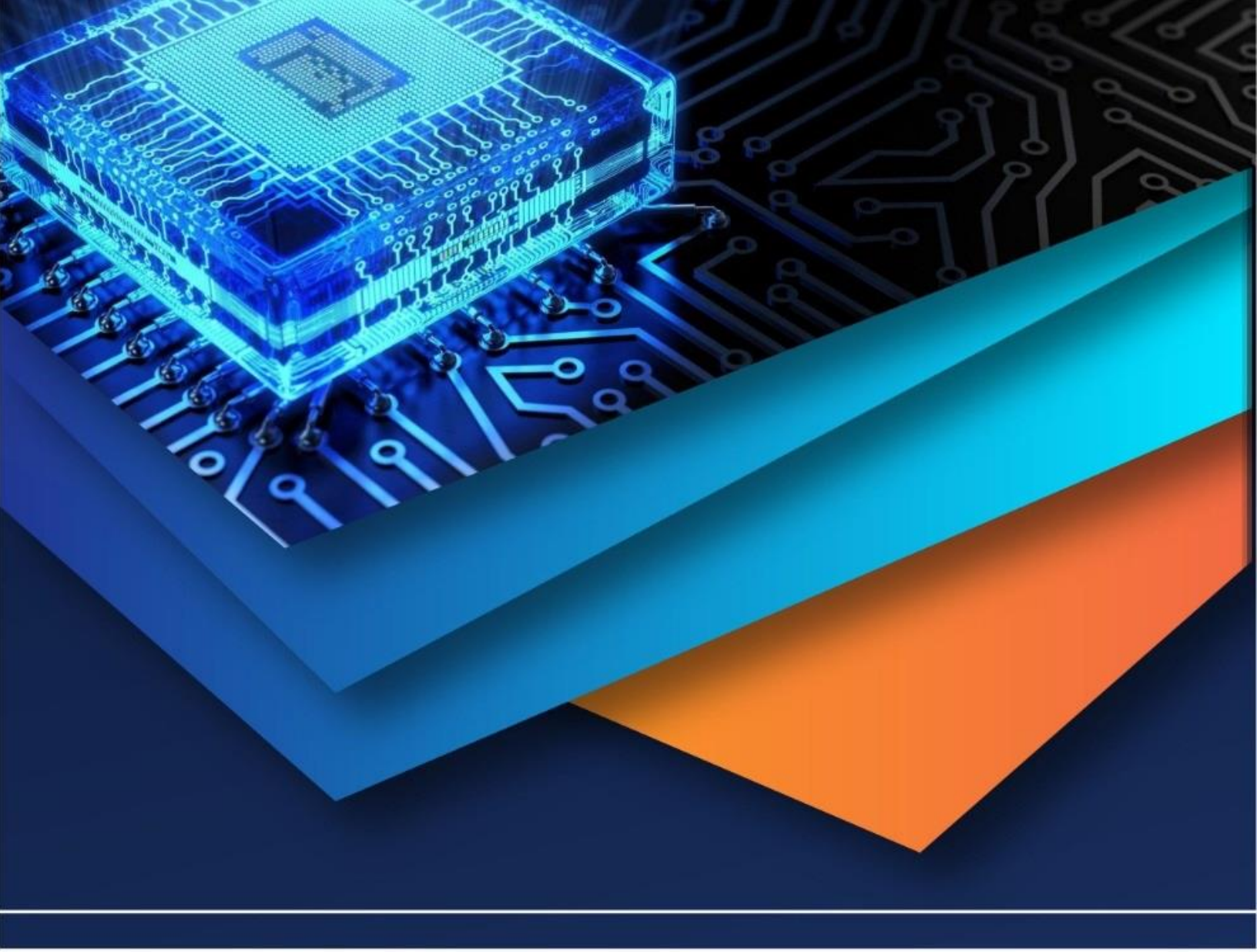

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