iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 10 **Issue:** IV **Month of publication:** April 2022

DOI: https://doi.org/10.22214/ijraset.2022.41193

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International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 10 Issue IV Apr 2022- Available at www.ijraset.com

A Review on Design and Analysis of Low Power PLL for Digital Applications and Multiple Clocking Circuits

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Abstract: ***A phase locked loop (PLL) is a basic element of many communication and instrumentation domain. This paper discusses the challenges in designing the low power PLL for multiple frequency output for digital applications. PLL is a key element providing clocking scheme in many electronic circuits raises the requirement of decreasing the power, with the advancement in CMOS technology. In this work, we provide review on low power PLL with good stability.***
Keywords: Phase-locked loop, CMOS, Clocking, low Power, Digital Applications, etc.

I. INTRODUCTION

PLL is a basic building block used in communications system such as mobile phones, motor speed control, optical disk drive etc. The primary goal of the PLL is to produce a clock which has same phase and frequency as that of reference clock. Once the phase and frequency are matched PLL goes into locked state. This is accomplished by correcting error between the reference and feedback signal. For modern IC designing, the important element need to be considered while designing is its low power consumption and increased operating speed. For this paper the focus is more commonly on reduction of power consumption. The PLL is a feedback control system consisting of many components in designing. These circuitry can be modified to obtain the desired outcomes, without effecting different fundamental phenomenon.

The Phase locked loop is a feedback control system which maintains the phase and frequency of output signal and reference signal constant [1]. In the synchronizing state, which is also referred to as “the locked state”, the phase error which occurs between the output signal and the input or reference signal remains either constant or is zero However, if in the process due to some discrepancy a phase error have some value rather than zero or constant, a control mechanism gets triggered, which acts upon oscillator to counter-balance the obtained resulted phase error in such a way that it will reduced to minimum until it will matched [2].

With the continuous advancement of CMOS technology, the need for low complexity, low-power and high stability PLL has increased as more and more functions on the chip implemented [2] [3] [5]. Along the same, with an increasing trend to a system-on-chip, in order to achieve low manufacturing cost, PLL has to be implemented in a low-voltage submicron CMOS technology [6]. With aspect to this, we have proposed a low power and high stability PLL design.

A typical design of PLL consists of three basic blocks as phase detector, a low pass filter (LPF) and a Voltage Controlled Oscillator (VCO).

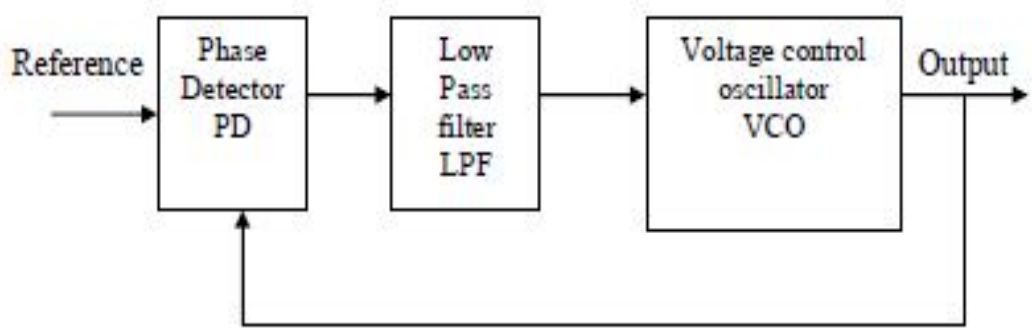

Fig. 1 Basic Building Block diagram of PLL

The Block diagram of PLL basically consist of following sub-circuits as,

A. Phase Detector

The phase detector output voltage proportional to the phase difference between the VCO's output signal and the reference. The phase detector output produces a regular square oscillation when the clock input and signal input have one quarter of period shift or 90 (PI/2).

B. Low Pass Filter

The filter of PLL is used to transform the instantaneous phase difference into an analog control voltage which is equivalent to the average output of phase detector. The rapid variations of the phase detector output are converted into a slow varying signal by filter, which will later control the voltage controlled oscillator.

The filter may simply be a large capacitor C, charged and discharged through the Ron resistance of the switch. The RonC delay creates a low-pass filter.

C. Voltage Controlled Oscillator

The VCO is the most important functional unit in the PLL. The voltage controlled oscillator (VCO) generates a clock with a controllable frequency. The VCO is commonly used for clock generation in phase lock loop circuits. Its output frequency determines the effectiveness of PLL. In addition to operating at highest frequency, this unit consumes the most of the power in the system. Obviously, this unit is of particular focus to reduce power consumption. PLL with multiple outputs means to design VCO with multiple outputs.

II. MOTIVATION

In recent years, continuous development in VLSI technology is going on. With the development in VLSI, power has become one of the most important paradigms of design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. Hence the design must be implemented with very low power consumption. The current leading-edge technologies such as low bit-rate video and cellular communications already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications on VLSI and systems design.

III.PROBLEM DEFINITION / FORMULATION

In this project we are going to proposed low power phase locked loop with multiple output frequencies. The modern communication Engineering applications are designed to work on multiple frequencies, so the proposed PLL with four multiple output using CMOS technology will be the best solution assuming low power and high stability for multiphase clocking circuits.

Also till now, the significant work is done mainly describes the modification on design of VCO and PFD. However the low pass filter plays major role in PLL design, the charging and discharging of loop filter's capacitor must be controlled in a way so that power dissipation can be further reduced.

IV. OBJECTIVES

The basic objectives are associated with an aim of project and analyzed to design PLL as Low Power, High performance with multiple frequency output phase locked loop, using VLSI technology

The following objectives:

1) To Study CMOS VLSI Design Issues, ASIC design flow, Deep-Submicron CMOS cell design, different nanometers technology.
2) To design different PLL using CMOS VLSI technology.
3) To design PLL using 45nm
4) Modification on design of VCO and PFD
5) Charging and discharging of low pass filter's capacitor have to control.
6) Comparative analysis of designed PLL various earlier design PLL.

V. LITERATURE REVIEW

The rigorous review for related work and published literature, it is observed that many researchers have designed Phase Locked Loop (PLL) by applying different techniques like analog and digital simulation, applying mathematical/logical relations. Since in the real world today VLSI/CMOS is in very much in demand, from the careful study of reported work it is observed that very few researchers have taken a work for designing PLL with CMOS/VLSI technology.

Prashant Thane Patil, Dr. Mrs. Vaishali Ingale [1] reported a PLL is design implementation in Virtuoso tool by Cadence in Analog Design Environment using GPDK 90 CMOS technology with D.C. supply voltage of 1.8V simulated with Spectre simulator. Total power consumption is of 4.2mW VCO control voltage is 1.4V in locked state with locked time at 100ns [1].

T.Nirmalraj, Radhakrishnan [2] proposed a dynamic logic based CMOS to design phase detector, VCO and loop filter. In the dynamic CMOS logic PLL the power is reduced to O.l3mW and speed is improved to O.50GHz. The proposed CMOS dynamic PLL operates at very high speed with less power dissipation. In the design the number of transistors are predominantly reduced with area.

Nagris Akhatar and Md Tawfiq Amis [3] represents an area efficient low power Phase frequency detector for phase locked loop applications in 90nm CMOS technology. The author design two gate diffusion input cells based simple PFD, chip area, power consumption and delays is reduced compared with the conventional design flow. The implemented model has been improved for performance in terms of low DC power consumptions [3].

Nilesh D. Patel, Gunjankumar R. Modi, Priyesh P. Gandhi and Amisha P. Naikin [4] presents design and analysis of PLL, which is simulated in CMOS 0.18µm technology. The digital phase locked loop achieves locking within about 100 reference clock cycles. The PLL circuit successfully achieved 1.55GHz frequency. Jitter is 1.09ns.

Yating Zhang, Zhao Xing, Yu Peng, Tian Zhang, Huihua Liu, Yunqiu Wu, Chenxi Zhao, Kai Kang [5] proposed a 2.9 GHz phase-locked loop (PLL) based on a three-stage CMOS ring oscillator is presented. A simplified ring voltage-controlled oscillator is used in the PLL fabricated in 110-nm CMOS technology. The delay cell of the VCO only consists of six transistors and the wide tuning range of the proposed ring VCO is from 1.6 GHz to 7.8 GHz

G. Parameswara Rao, U. Geeta Lakshmi, K. Saisuguna, A. Sateesh [6] proposed work to design pll using latest 50nm technology, which offers high speed performance at low power. Divya Patel, Prof. Yash Kshirsagar [7] designing is basically the designing of Low Power PLL by reducing power consumption of VCO using 0.25 µm CMOS technology. The results are verified for both circuit and system level. Amruta M. Chore1, Shrikant J. Honade, [8] in this proposed paper designs a phase locked loop is using VLSI technology. Their work is basically for high speed performance at low power.

Zafer Ozgiir Gursoy (2003) [9] designed, verified, system integrated and physically realized a high speed monolithic phase locked loop (PLL) based high performance clock and data recovery (CDR) circuit using conventional 0.13-pm digital CMOS Technology which operates up to 3.2 GHz of sampling frequency and can achieve the robust phase alignment with overall power consumption of 18.6mW having silicon area of the CDR is approximately 0.3 mm2 with its internal loop filter capacitors.

Ashish mishra (2014) [10] has analysed that by using 5-stage CSVCO (Current starved VCO), lock range from 357MHz-900MHz has increased with large VCO gain, lock time has reduced and got improved around (54ns) with oscillation frequency range 431.683 MHz-1.7966 GHz because of more number of inverter stages with PLL power dissipation of 7.08mW. Also the phase noise performance for the 5-stage VCO has improved.

Jeng-Han Tsai et.al (2015) [11] designed and fabricated an X-band 9.75/10.6GHz fully integrated low power PLL on 180nm CMOS process. Nearly 24mW power has consumed, with output frequency of 9.75GHz and 10.6GHz which has successfully synthesized with a reference source of 12.5MHz, through band control circuit of VCO and modulus frequency divider.

Kruti P. Thakore (2011) [12] presented three types of PFDs- traditional, modified and high speed, on comparing these with each other in respect of low power and low jitter it has detected that high speed PFD has achieved it. High speed PFD has operated at input frequency of 1GHz with 1.8V supply voltage, total power consumed is 0.39nW and resulted only 2ps of jitter. It has been simulated with 350nm CMOS technology

VI. PROPOSED WORK

The proposed work is aimed to design transistorized CMOS physical layout of Phase locked loop to achieve for Low power, area efficient, high stability Phase Locked Loop. The design of Multiple Frequency Output Phase Locked Loop is a new concept and also found superior to all the conventional techniques with four multiple outputs as PLL8x, PLL4x, and PLL2x & PLL1x.

The proposed project is also plan to work on low supply voltage of 1volt. By observing the output of PLL at each node with the voltage variation of supply voltage from 0.6 volt to 1 volt. The expected output frequency of each node must be remained same. This results will prove the stability of the proposed PLL. The care is taken for very high efficient, low power and optimum area.

The process steps for achieving the design optimized parameter areas;

1) Schematic design of proposed PLL using CMOS transistors (BSIM4).
2) Performance verification of the above for different parameters.
3) CMOS layout for the proposed PLL using VLSI backend.
4) Verification of CMOS layout and parameter testing.
5) If the goal is achieved for all proposed parameter including detail verification, sing off for the design analysis and design will be ready for IC making.
6) If detail verification of parameters would not completed then again fallow the first step with different methodology.

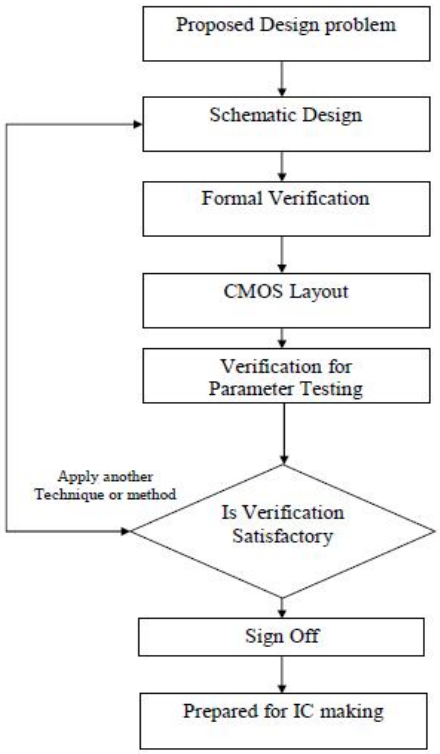

Figure 2: Design Flowchart

VII. PROBABLE OUTCOME

The probable outcome for the proposed design is the low power, area optimized and highly stable and efficient phase locked loop. The design will provide four multiple output frequencies as PLL8x, PLL4x, and PLL2x & PLL1x.

The PLL is implemented in it transistorized Physical Design. The more focus is commonly on reduction of power consumption. The sub circuits are designed in CMOS for each element and converted into physical layout using lambda based rules using CMOS EDA tool combined to form a PLL. These circuitry are modified to obtain the desired outcomes, without effecting different fundamental phenomenon. The measured tuning range of the proposed High performance VCO design will be in the range for PLL. The measured tuning range of the proposed high performance VCO design will be totally dependent on input DC supply as clock input. The on screen power estimation for physical design of PLL will be optimized in order to get the better stability.

VIII. CONCLUSIONS

CMOS technology is the need of today's world. With the advancement in CMOS, more and more complex functions have been designed and implemented in a very smaller size. The CMOS based PLL is discussed here with design trend of 45nm technology. BSIM4 MOS modelling design concept is used in the design with 300 MOS parameters taking in consideration. The low power PLL design circuits discussed in this paper mainly describes the modification on design of VCO and PFD. The new approach of multiple output PLL is proposed considering the physical design implementation. Herein we also found that the phased locked loop with low power consumption, good stability and optimized area with improved tuning range as compared to other phase locked loop circuits have vast application like communication, networking, control system and also our daily life.

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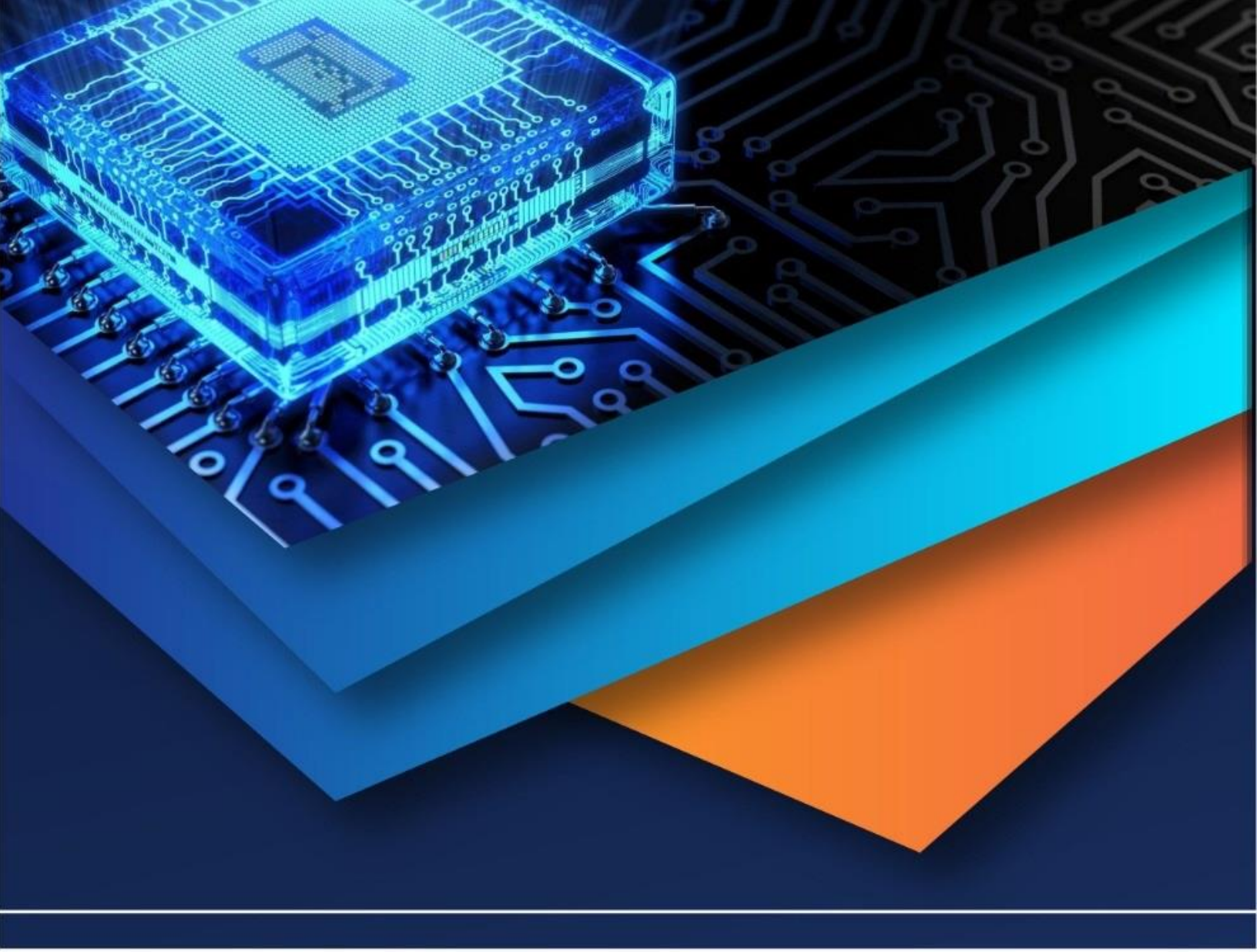

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