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Low Power Two Stage CMOS Operational Amplifier

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Abstract: ***Operational amplifier (Op-Amp) circuits play a critical role in computation, instrumentation, and a variety of industrial applications. With the growing demand for precision Op-Amps in automotive and industrial environments, there is an increasing need for designs that offer enhanced accuracy and robust performance across wide temperature ranges. The shift towards integrating both analog and digital circuits on a single chip has made Complementary Metal-Oxide Semiconductor (CMOS) technology the preferred choice over traditional bipolar technologies for analog circuit design in mixed-signal systems.***
Among various Op-Amp topologies, the two-stage architecture remains one of the most widely adopted due to its favorable gain and output swing characteristics. This paper presents the design and simulation of a CMOS-based two-stage fully differential operational amplifier, optimized for low-power and low-voltage operation. The amplifier is biased with a current of 20 µA and is implemented using both 180 nm and 90 nm CMOS process technologies. Special emphasis is placed on operation in the sub-threshold region, where the unique behavior of MOS transistors facilitates ultra-low-voltage and low-current operation.
The proposed Op-Amp is intended for on-chip applications with capacitive load requirements in the picofarad range. Simulation results are obtained using the Cadence Virtuoso design environment and demonstrate the performance of the amplifier across key parameters in both technology nodes.
Tools: Cadence Virtuoso

I. INTRODUCTION

The increasing demand for compact, energy-efficient electronic systems with extended battery life has accelerated the trend toward low-voltage, low-power silicon chip design. This trend spans a wide range of market segments, including telecommunications, medical devices, computing, and consumer electronics. In such systems, operational amplifiers (Op-Amps) play a fundamental role due to their versatility and essential functionality in analog signal processing.

Operational amplifiers are integral components in analog electronics, used for tasks ranging from simple DC bias generation to high-speed amplification and complex signal filtering [1]–[3]. As one of the most widely utilized building blocks in electronic circuits, Op-Amps are found in countless consumer, industrial, and scientific applications [4]. Their ability to perform a variety of mathematical operations—such as addition, subtraction, integration, and differentiation—makes them indispensable in signal conditioning and processing tasks [5].Modern Op-Amps are linear, high-gain, DC-coupled devices typically designed for use with negative feedback to establish precise closed-loop transfer functions. These characteristics make them ideal for a broad range of analog applications. Notably, many general-purpose Op-Amps are cost-effective, with prices often below one dollar, and are engineered with features such as short-circuit protection for enhanced durability [6]–[9].A standard Op-Amp consists of two input terminals—non-inverting (positive) and inverting (negative)—along with a single output terminal and dual supply voltages, typically denoted as +V_CC and –V_CC. The basic symbol of an operational amplifier is illustrated in Figure 1.One of the fundamental principles that underpins the versatility of operational amplifiers (Op-Amps) is feedback, particularly negative feedback, which forms the basis of nearly all automatic control systems [10]–[12]. The theoretical foundations of feedback extend well beyond electronics and are essential to many areas of engineering. A solid understanding of these concepts is invaluable for students and practitioners in the field [13].Op-Amps also find utility in digital logic through comparator circuits. Comparators can be classified as full (total) or equality comparators. Full comparators evaluate and identify the relative magnitude between two n-bit binary inputs (A and B), whereas equality comparators simply determine whether the two inputs are identical.One common configuration that illustrates the principles of Op-Amp operation is the voltage follower (or buffer). In this configuration, the input and output voltages are equal:

Vin = Vout

At first glance, a voltage follower may appear redundant—functioning seemingly like a simple wire. However, its significance becomes clear when the core operational principles of Op-Amps are considered. Two ideal assumptions govern Op-Amp behavior:

No current flows into the input terminals (V+ and V–), implying infinite input impedanceThe voltages at the non-inverting (V+) and inverting (V–) terminals are equal when negative feedback is applied—a condition known as the virtual short approximation.The high input impedance of the voltage follower ensures that it draws negligible current from the source signal. This property makes the configuration ideal for buffering and isolating stages in analog systems, as it allows signal measurement or transfer without affecting the original circuit conditions.Additionally, due to the virtual short approximation (V+ = V–) and the negative feedback connection between the Op-Amp's output and inverting input, the output voltage follows the input precisely (Vout = Vin). This feature is especially useful for impedance matching and signal buffering applications [14]–[16].As their name suggests, operational amplifiers are designed to amplify input signals. The amplification factor, or gain, is the ratio of output to input signal amplitudes. In theory, the gain of an ideal Op-Amp is infinite, allowing for the amplification of even the smallest signals to significant levels. While practical Op-Amps have finite gain, the assumption of infinite gain is useful for initial analysis and understanding of common configurations such as the inverting amplifier.

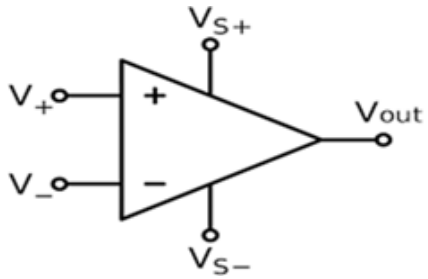

Fig.1.Operational Amplifier

II. EXISTING SYSTEM

This paper proposes a novel two-stage CMOS operational amplifier design optimized for high-speed and area-efficient performance. With the growing demand for high-performance digital systems, there is a critical need for operational amplifiers and comparators that deliver rapid response times while maintaining a compact footprint. The proposed architecture addresses these requirements through scalable design principles and effective circuit optimization, tailored specifically for CMOS-based amplifier and comparator applications.

Key features of the proposed design include the use of advanced circuit techniques to reduce propagation delay, thereby enhancing speed without increasing the silicon area. Implementations in both 180 nm and 90 nm CMOS technologies are explored, demonstrating adaptability across process nodes. Additionally, the design employs low-power techniques, contributing to greater energy efficiency—a crucial factor in modern portable and battery-operated systems.

The proposed amplifier incorporates scalable elements, making it flexible for a range of bit-widths and suitable for integration into various high-speed digital signal processing applications. Simulation results indicate superior performance in terms of speed, bandwidth, and area utilization when compared to traditional architectures. The 90 nm CMOS implementation, in particular, exhibits promising results for applications requiring high slew rates, wide bandwidth, and efficient digital comparison capabilities.Relevant prior work includes the design presented by Priyanka et al. [1], which features a two-stage CMOS operational amplifier operating at a 1.8 V supply in a 180 nm process. The design utilizes a bias current-dependent input stage and achieves a gain of 63 dB and a bandwidth of 140 kHz when driving a 1 pF capacitive load. Additional performance metrics include a common-mode gain of -25 dB, a slew rate of 32 V/µs, and a power consumption of 300 µW.

Another notable design approach was proposed by Swami and Rai [3], emphasizing a structured methodology for achieving high gain, wide output voltage swing, and high common-mode rejection ratio. Their process involved iterative adjustment of transistor width-to-length (W/L) ratios to establish appropriate DC operating points, ensuring all MOSFETs remain in the saturation region. Subsequent AC and transient simulations were used to evaluate gain, phase margin, and overall stability of the design.These existing systems provide valuable foundations for high-performance Op-Amp design. However, the proposed work extends these efforts by offering a scalable, low-power solution with improved speed and area efficiency, validated through simulation in both 180 nm and 90 nm technologies.

III.PROPOSED SYSTEM

A two-stage complementary metal-oxide-semiconductor (CMOS) operational amplifier was designed and simulated utilizing a 90nm process technology. The corresponding schematic diagram is illustrated in Figure 2.

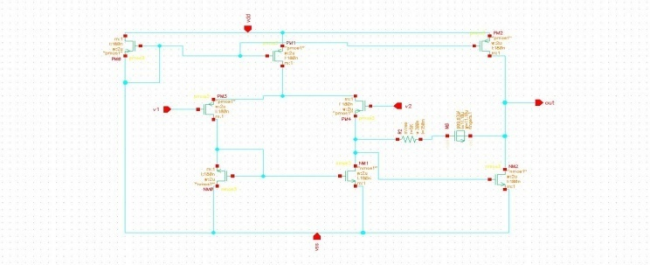

Fig.2.Schematic of two stage CMOS op-amp

IV. SIMULATION RESULTS

The peak-to-peak operating voltages and currents of the circuit were determined through transient analysis. This simulation utilized an input pulse with a 1 µs width and a 3 µs period, and the resulting transient behavior is visualized in Fig. 3

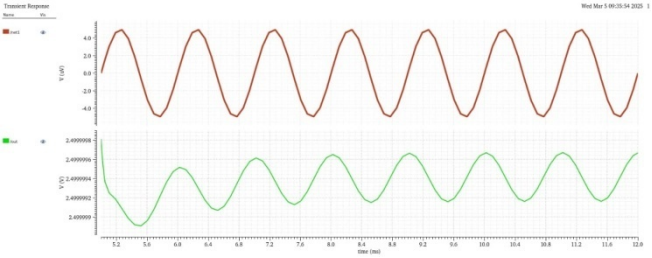

fig3:Transient analysis

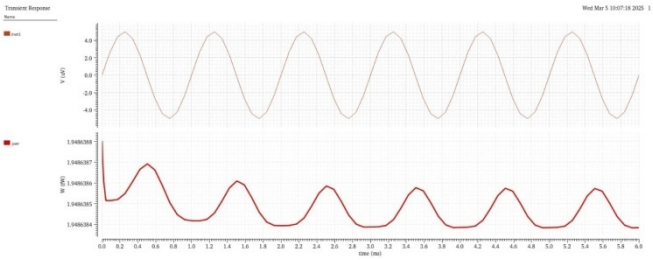

Fig4: Power analysis

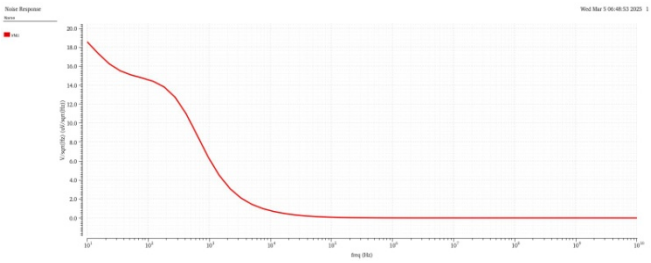

Fig5: Noise analysis

V. CONCLUSION

"This work presents the design and characterization of a high-performance two-stage CMOS operational amplifier in a 90nm CMOS process, successfully meeting all specified design parameters. Notably, the design achieves enhanced gain, slew rate, and a wide unity-gain phase margin, demonstrating its suitability for demanding analog applications. While minor discrepancies between simulation and theoretical calculations were observed, attributable to simplifications inherent in analytical modeling, the theoretical framework provided a robust foundation for the design process. Comprehensive simulations, conducted using Cadence Virtuoso, validated the design's functionality, showcasing a near rail-to-rail output voltage swing achieved by operating current-sourcing transistors in the deep triode region.

The key performance metrics, including DC gain, phase margin, settling time, power dissipation, common-mode rejection ratio (CMRR), unity-gain bandwidth (UGB), and slew rate, were rigorously evaluated and found to be in close agreement with theoretical predictions. Furthermore, the UGB was effectively tuned by adjusting the widths of critical transistors, demonstrating the design's flexibility and potential for optimization. This study contributes a practical and well-characterized operational amplifier design, highlighting the trade-offs and optimization techniques involved in achieving high performance in nanoscale CMOS technology."

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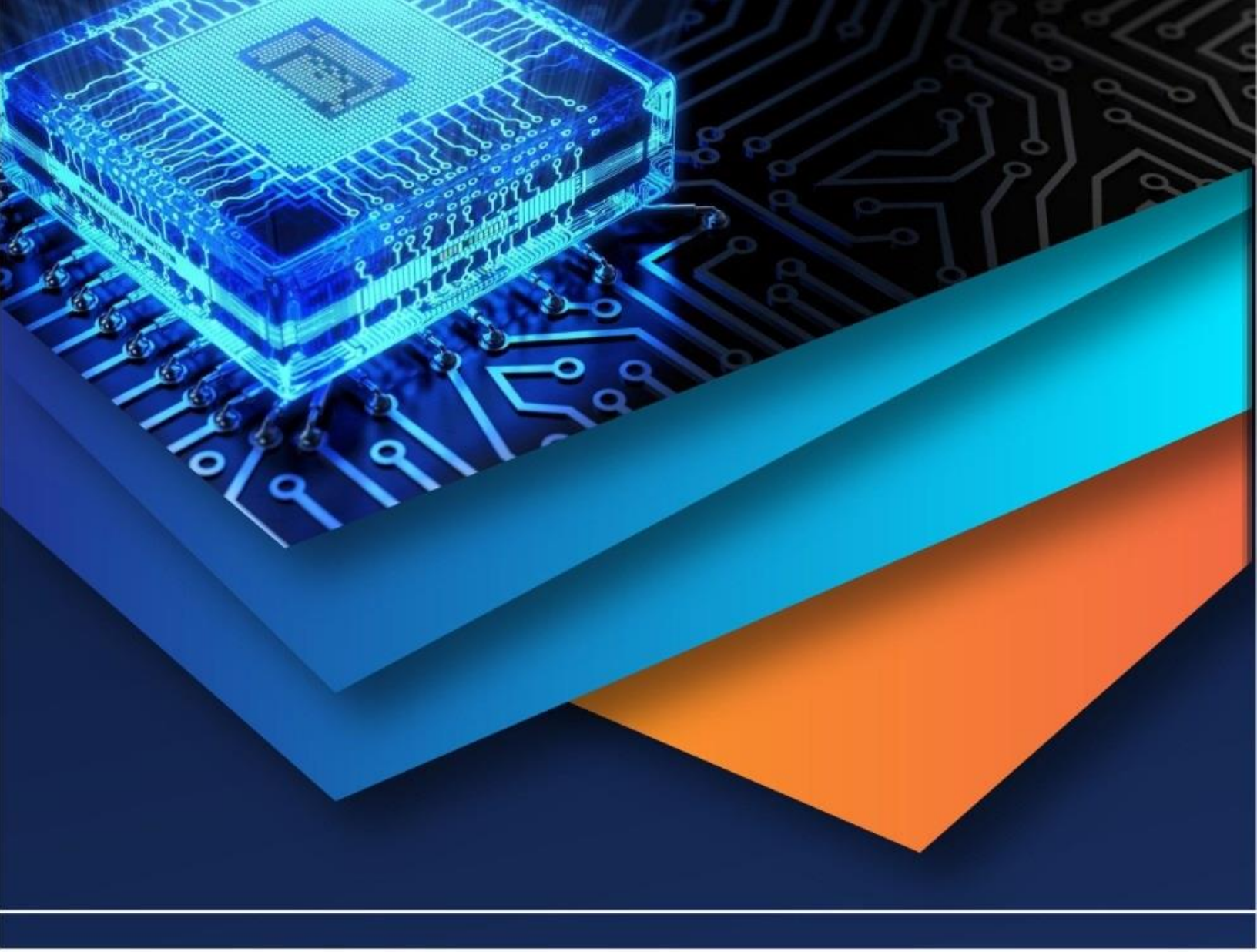

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