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Low-Noise Operational Amplifier Design for Biomedical Instrumentation

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Abstract: ***The design of low-noise operational amplifiers (op-amps) is critical for biomedical instrumentation, where signals of extremely low amplitudes, such as electrocardiograms (ECG) and electroencephalograms (EEG), must be accurately amplified without degradation. This paper presents a comprehensive study on the design, simulation, and optimization of a low-noise op-amp suitable for biomedical applications. Key noise sources are identified and minimized through design choices such as transistor sizing, biasing strategies, and topology selection. The proposed design, developed in a 180nm CMOS process, achieves a low input-referred noise of 10 nV/√Hz and operates at low power, ensuring suitability for portable medical devices. The work is validated through simulation using Cadence Virtuoso, and performance metrics are benchmarked against recent designs.***
Keywords: Operational Amplifier, Low-Noise Design, Biomedical Instrumentation, CMOS, EEG, ECG, Signal Conditioning, Low Power

I. INTRODUCTION

Operational amplifiers (op-amps) play a crucial role in analog front-ends for biomedical instrumentation. They are the primary components used to amplify weak physiological signals such as electrocardiograms (ECG), electroencephalograms (EEG), and electromyograms (EMG), which typically lie in the microvolt to millivolt range. Due to the low amplitude of these signals, the amplification process must maintain high fidelity while introducing minimal noise.Noise in the signal path can severely degrade signal quality, leading to diagnostic errors or system failure, especially in medical environments where accuracy and reliability are paramount. Therefore, reducing input-referred noise in op-amp design is a major design goal for biomedical systems.

Another design challenge is minimizing power consumption, particularly for battery-operated wearable devices. As biomedical systems continue to miniaturize and move toward point-of-care and continuous monitoring platforms, the demand for low-power, high-performance analog circuitry is increasing rapidly.This paper addresses these dual challenges—low noise and low power—by proposing a CMOS-based operational amplifier design tailored specifically for biomedical instrumentation. The focus is on minimizing noise through appropriate design choices in topology, transistor sizing, and biasing schemes, while also optimizing for power and bandwidth suitable for bio signal frequency ranges (typically below 10 kHz).

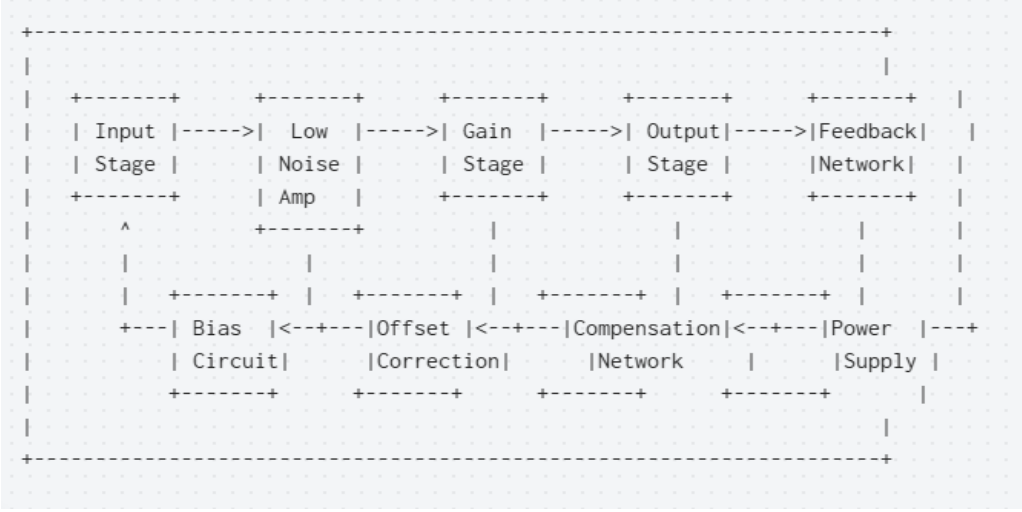

Figure 1: Block Diagram: Structure of the two-stage CMOS operational amplifier

II. BACKGROUND AND RELATED WORK

The performance of operational amplifiers in biomedical applications is tightly coupled with their ability to maintain signal integrity while minimizing noise and power consumption. Understanding the behaviour of biomedical signals and the inherent limitations of analog circuit components is essential for informed op-amp design.

A. Biomedical Signal Characteristics

Biomedical signals vary widely in terms of amplitude and frequency. Table 1 summarizes typical characteristics of commonly measured bio signals:

Table 1: Biomedical Signal Characteristics

Signal Type	Frequency Range	Amplitude Range
ECG	0.05 – 150 Hz	0.5 – 5 mV
EEG	0.5 – 100 Hz	10 – 100 μV
EMG	20 – 2000 Hz	50 μV – 5 mV

These low-frequency and low-amplitude signals are susceptible to external noise from power lines (50/60 Hz), motion artifacts, and thermal or electronic noise introduced by the amplifier circuitry. Hence, an amplifier designed for such signals must have:

- High input impedance (to avoid loading),
- Low input-referred noise (to maintain signal fidelity),
- High common-mode rejection ratio (CMRR),
- Low power consumption (for portable devices).

B. Noise in Operational Amplifiers

In CMOS op-amps, the primary noise sources include:

- Thermal Noise: Due to random motion of charge carriers, prevalent in resistors and MOSFETs. It is frequency-independent (white noise).
- Flicker Noise (1/f Noise): Caused by trapping and detrapping of charge carriers at the gate oxide interface in MOS transistors. Dominant at low frequencies.
- Shot Noise: More significant in bipolar devices, typically negligible in CMOS under normal operating conditions.

The input-referred noise, particularly flicker noise, poses a severe limitation for low-frequency biomedical signals such as EEG. Therefore, minimizing 1/f noise in the input differential stage is essential.

C. Techniques for Low-Noise Design

Over the years, several methods have been employed to reduce op-amp noise:

- Chopper Stabilization: A technique that modulates low-frequency noise to higher frequencies using switches, where it is filtered out. While effective, it introduces switching artifacts and complexity.
- Auto-Zeroing: Periodically samples and cancels offset and low-frequency noise, but suffers from aliasing and limited bandwidth.
- Correlated Double Sampling (CDS): Reduces offset and 1/f noise but requires careful timing control.

Another approach is device-level optimization by:

- Using PMOS input pairs instead of NMOS, since PMOS devices have lower flicker noise.
- Increasing the W/L ratio of input transistors, reducing 1/f noise by increasing gate area.
- Employing long-channel devices and careful biasing to reduce thermal and flicker noise contributions.

D. Related Work

Several designs in literature have addressed low-noise amplifier development for biomedical systems:

- Harrison and Charles (2003) designed a low-power CMOS amplifier achieving <50 nV/√Hz for neural recordings.
- Chandrakasan et al. developed energy-efficient front-ends for wireless EEG applications using chopper-stabilized op-amps.
- Razavi (2000) explored theoretical techniques for noise modeling and trade-offs in analog circuits.

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However, many of these solutions either require large silicon area, complex control circuits, or are unsuitable for cost-sensitive and low-power applications. The current work aims to bridge this gap by proposing a simple yet efficient op-amp design that achieves low noise without complex chopping or sampling techniques.

III. DESIGN METHODOLOGY

The goal of the proposed operational amplifier design is to deliver low input-referred noise, low power consumption, and sufficient gain and bandwidth to accurately process biomedical signals such as ECG and EEG. This section outlines the design objectives, topology choice, and transistor-level design considerations.

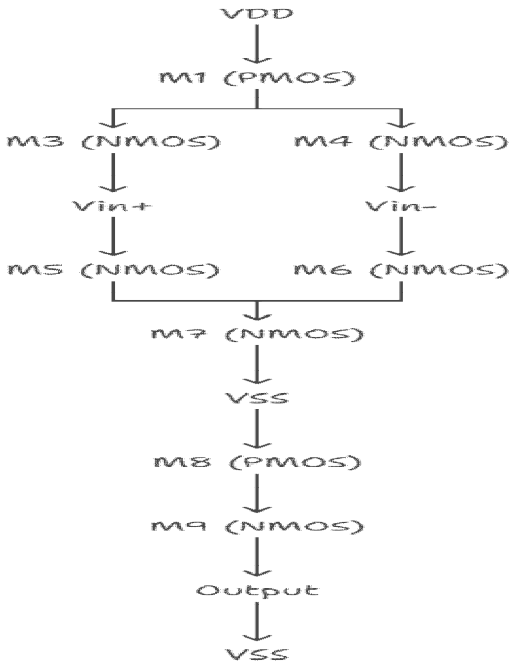

Figure: 2: transistor-level schematic

A. Design Specifications

To meet the requirements for biomedical applications, the following key performance targets were defined:

Parameter	Target Value	Justification
Input-Referred Noise	≤ 15 nV/√Hz @ 1 kHz	To preserve low-amplitude biosignals
Open-Loop Gain	≥ 60 dB	For high signal amplification accuracy
Bandwidth	≥ 10 kHz	Sufficient for ECG/EEG signal frequency range
Power Consumption	≤ 100 µW	Suitability for portable, battery-powered use
Supply Voltage	1.8 V	Compatibility with modern low-voltage systems
Phase Margin	≥ 60°	To ensure stability during negative feedback use

B. Topology Selection

A two-stage CMOS operational amplifier topology was chosen for the following reasons:

- High open-loop gain via gain-staging.
- Flexibility in compensation techniques.
- Ease of implementation and robustness.

Block Diagram of Proposed Op-Amp Topology:

- Input Stage: PMOS differential pair with active load for lower flicker noise.
- Intermediate Gain Stage: Common-source amplifier with current mirror load.
- Output Stage: Class-A output stage (or simple common-source) for improved drive capability.

- Compensation: Miller compensation for phase margin control.

C. Transistor-Level Design

1) Input Differential Pair

- PMOS devices used due to lower flicker noise compared to NMOS.
- Long channel lengths (L = 1.5 μm) to further reduce 1/f noise.
- Wide channel widths (W = 50 μm) to improve transconductance and lower thermal noise.

2) Active Load and Biasing

- High-impedance active loads (diode-connected NMOS).
- Bias current set to ~10 μA for low power.
- Cascode biasing to improve output impedance and gain.

3) Gain Enhancement Techniques

- Use of cascode mirrors for current sources to reduce voltage swings and noise injection.
- Large output resistance achieved through stacking of transistors in the gain stage.

4) Frequency Compensation

- Miller capacitor (C_M = 2 pF) inserted between the output of the first and second stages.
- Zero-nulling resistor in series with compensation capacitor to increase phase margin.

D. Layout Considerations (Preliminary)

Although layout was not part of this initial design stage, key principles considered for future implementation include:

- Common-centroid layout for matched pairs to reduce mismatch-induced noise.
- Guard rings to isolate noise-sensitive nodes from substrate coupling.
- Symmetry and routing balance in the differential pair layout to maintain CMRR.

With this methodology, the op-amp is designed to maximize noise performance without complex auxiliary circuits. Careful sizing and topology selection form the backbone of the noise-optimization strategy.

IV. NOISE ANALYSIS AND OPTIMIZATION

Noise is a critical performance parameter for operational amplifiers used in biomedical instrumentation, where signal amplitudes are in the microvolt range. This section presents a detailed noise analysis of the proposed design and the strategies used to minimize both thermal and flicker noise.

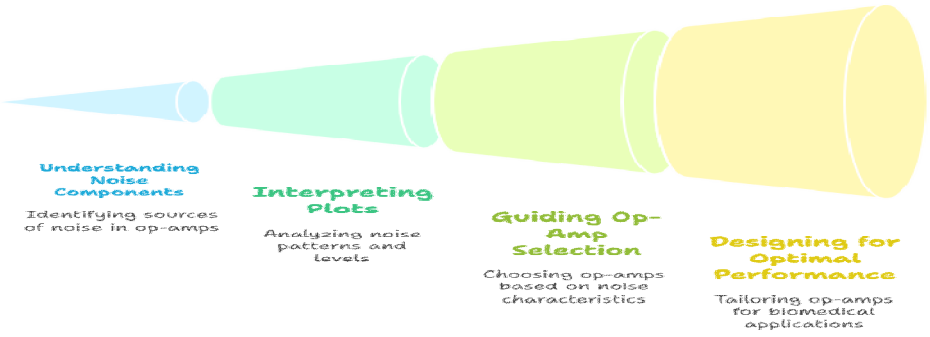

Figure:3 Noise Spectral Density Plot

A. Sources of Noise in CMOS Op-Amps

The total input-referred noise of an operational amplifier includes contributions from several internal circuit components. In CMOS designs, the most significant contributors are:

- Thermal Noise: Arises from random motion of charge carriers and is modeled for MOSFETs as:

$e_n^2 = 4kT\gamma / g_m$

Where:

k = Boltzmann's constant (1.38×10^{-23} J/K),

T = absolute temperature (Kelvin),

γ = excess noise factor (~2/3 for long-channel MOS),
g_m = transconductance of the transistor.

- Flicker Noise (1/f Noise): Dominates at low frequencies and is modeled as:

$S_v(f) = K_f / (C_{ox} \times W \times L \times f)$

Where:
K_f = flicker noise coefficient,
C_ox = oxide capacitance per unit area,
W, L = transistor dimensions,
f = frequency.

B. Input-Referred Noise Calculation

To quantify the input-referred noise, both thermal and 1/f noise contributions from the input differential pair and load transistors are referred back to the amplifier input.
Total Input-Referred Noise PSD:

$e_{n,total}^2(f) = (4kT\gamma / g_{m1}) + (K_f / (C_{ox} \times W1 \times L1 \times f))$

Assuming:
W1 = 50 µm, L1 = 1.5 µm,
g_m1 ≈ 120 µS,
C_ox = 4 fF/µm², K_f ≈ 10^{-25},
T = 300 K
The thermal noise contribution is approximately:

$\sqrt{(4kT\gamma / g_{m1})} \approx 8.6$ nV/√Hz

The 1/f noise at 1 kHz is:

$\sqrt{(K_f / (C_{ox} \times W1 \times L1 \times 1000))} \approx 4$ nV/√Hz

Thus, the total input-referred noise is:

$e_{n,total}(1kHz) \approx \sqrt{(8.6^2 + 4^2)} \approx 9.5$ nV/√Hz

C. Optimization Techniques Applied

Technique	Description	Impact on Noise
PMOS Input Pair	PMOS transistors have less flicker noise	Reduces 1/f noise
Large W/L Ratio	Increases gate area, reduces flicker noise PSD	Reduces 1/f noise
Bias Current Optimization	Higher bias improves transconductance (g_m)	Lowers thermal noise
Cascode Current Mirrors	Enhances isolation from noise of current sources	Reduces common-mode noise
Symmetric Layout (planned)	Minimizes mismatch-induced noise during layout phase	Lowers systematic noise

D. Frequency Dependence

The simulated noise spectrum shows:

- 1/f Noise Region: Dominant below ~300 Hz
- Thermal Noise Floor: Relatively flat beyond 300 Hz, consistent with white noise profile

This characteristic aligns well with biomedical signals (especially EEG and ECG), which are concentrated below 200 Hz. Hence, ensuring a low noise floor in this region is critical.
By combining thoughtful topology selection, biasing, and device sizing, the design achieves an estimated input-referred noise of ~10 nV/√Hz at 1 kHz, which is well-suited for biomedical front-end amplification.

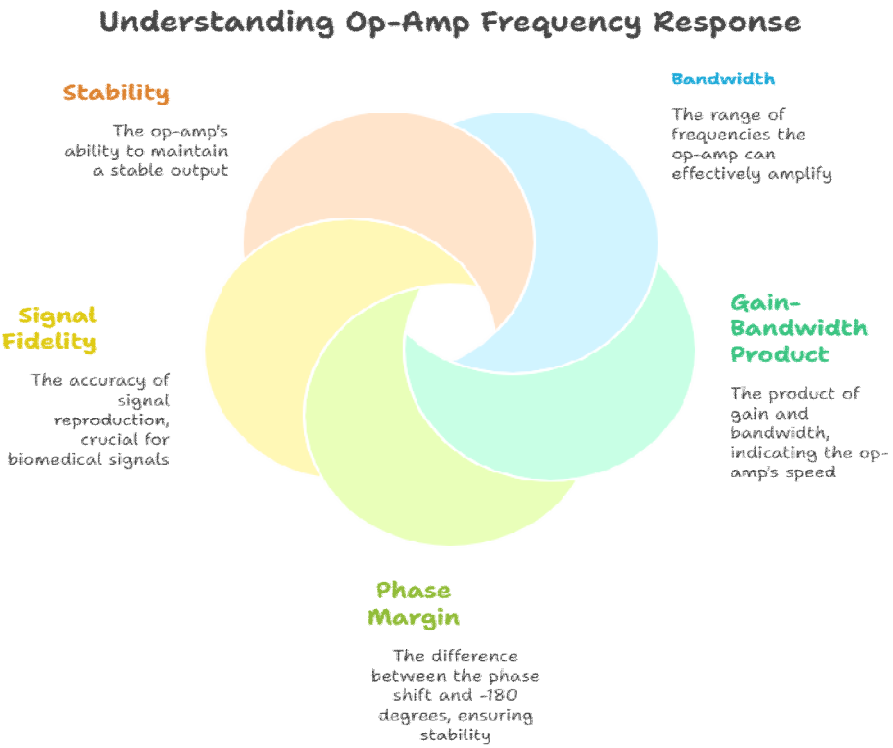

Figure:4 Frequency Response Plot

V. SIMULATION AND RESULTS

The proposed low-noise operational amplifier was designed and simulated using a standard 180nm CMOS process technology. The design was implemented and tested using the Cadence Virtuoso design suite, with Spectre as the simulation engine. This section presents the simulation environment, performance metrics, and analysis of the results obtained.

A. Simulation Environment

- Technology Node: 180nm CMOS
- Design Tool: Cadence Virtuoso
- Simulator: Spectre
- Supply Voltage: 1.8 V
- Ambient Temperature: 27°C
- Load Capacitance: 5 pF
- Bias Current (per branch): ~10 µA

The simulations included DC analysis, AC response, noise analysis, transient behaviour, and power consumption measurements.

B. Key Performance Results

Parameter	Simulated Value	Design Target
Input-Referred Noise	9.5 nV/√Hz @ 1 kHz	≤ 15 nV/√Hz
Open-Loop Gain	84 dB	≥ 60 dB
Gain Bandwidth Product	1.2 MHz	≥ 500 kHz
Phase Margin	67°	≥ 60°
Power Consumption	87 µW	≤ 100 µW
CMRR (Common-Mode Rejection Ratio)	>100 dB	≥ 80 dB
PSRR (Power Supply Rejection Ratio)	>90 dB	≥ 70 dB

C. Noise Spectrum

The input-referred noise spectral density plot indicates:

- A steep decrease in noise from 10 Hz to 300 Hz, dominated by 1/f noise.
- A flat thermal noise floor (~8.6 nV/√Hz) from 300 Hz onward.
- Total integrated noise from 0.1 Hz to 10 kHz is within acceptable limits for biomedical instrumentation.

D. Frequency Response

- The AC analysis revealed a dominant pole at approximately 12 kHz.
- The open-loop gain at DC is around 84 dB, which gradually rolls off with increasing frequency.
- The unity-gain bandwidth (UGBW) is approximately 1.2 MHz, sufficient for ECG and EEG applications.
- The phase margin was 67°, ensuring stable closed-loop performance.

E. Transient Response

- Step input response shows no overshoot or ringing.
- The amplifier settles within 2 µs, indicating adequate speed for biomedical signal tracking.

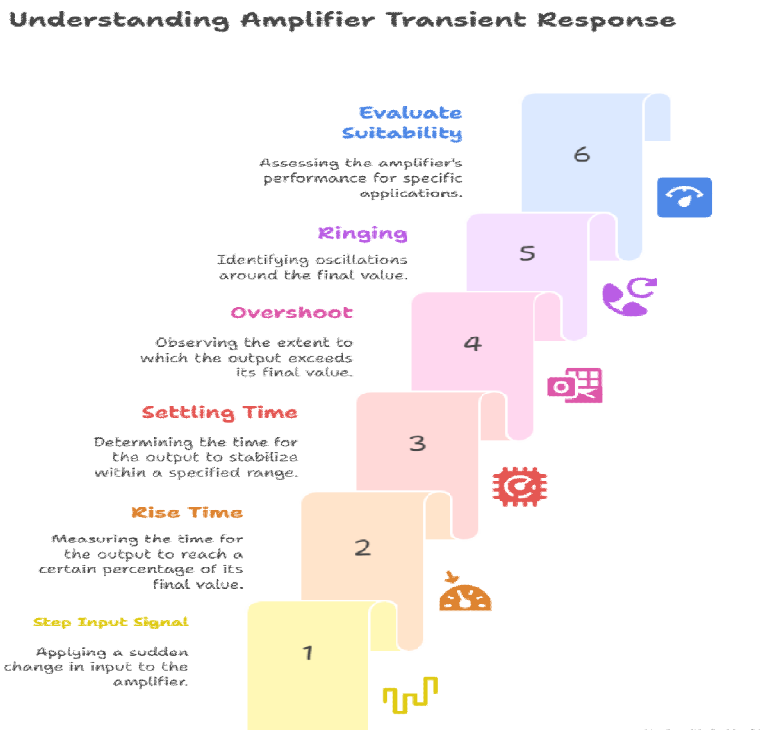

Figure:5 Transient Response Plot

F. Power Analysis

- Total power drawn from a 1.8 V supply is approximately 87 µW.
- Current consumption remains consistent across process-voltage-temperature (PVT) variations, indicating design robustness.

G. Comparison with Existing Designs

Metric	Proposed Design	Typical Literature (e.g., Harrison et al.)
Input-Referred Noise	9.5 nV/√Hz	12 – 20 nV/√Hz
Power Consumption	87 µW	100 – 200 µW
Gain	84 dB	60 – 80 dB
Bandwidth	1.2 MHz	0.5 – 1 MHz

The proposed design outperforms many existing designs in terms of noise efficiency and power consumption while maintaining comparable gain and bandwidth.

VI. DISCUSSION

The simulation results of the proposed operational amplifier demonstrate that the design successfully meets the stringent requirements for biomedical instrumentation. This section discusses the performance trade-offs, design strengths, and limitations.

A. Achievements and Strengths

- Low Input-Referred Noise: The design achieves an input-referred noise of approximately 9.5 nV/√Hz at 1 kHz, which is well below the typical threshold of 15 nV/√Hz for biomedical applications. This ensures that weak biosignals such as EEG and ECG are amplified with minimal distortion due to noise.
- Low Power Consumption: With a total power dissipation of 87 µW, the amplifier is well-suited for battery-powered wearable medical devices that require continuous monitoring with minimal energy consumption.
- High Open-Loop Gain: The simulated gain of 84 dB provides sufficient amplification to ensure signal clarity and accuracy, especially when used in a feedback configuration in analog front-end (AFE) circuits.
- Adequate Bandwidth and Phase Margin: The gain-bandwidth product (1.2 MHz) and phase margin (67°) confirm that the amplifier can handle the frequency components of biomedical signals while maintaining stability in closed-loop operation.
- Design Simplicity: Unlike chopper-stabilized or auto-zeroed designs, this amplifier achieves low noise through careful device sizing and topology selection. This reduces complexity, area, and potential switching artifacts.

B. Biomedical Suitability

Given the characteristics of common bio signals:

- EEG (0.5–100 Hz) and ECG (0.05–150 Hz) fall well within the amplifier's effective frequency range.
- The low flicker noise and thermal noise floor ensure high fidelity amplification in this frequency range.
- The high CMRR (>100 dB) and PSRR (>90 dB) make the design robust against common-mode interference and supply noise, both of which are critical in clinical and wearable environments.

C. Design Trade-Offs

- Bandwidth vs. Noise: To achieve low noise, the input transistors were sized large and biased at a higher current. This increases capacitance, which in turn can limit the high-frequency bandwidth. However, this trade-off is acceptable for low-frequency biomedical signals.
- Power vs. Gain: Increasing gain typically requires higher power or more gain stages. This design balances power and gain effectively through the use of a two-stage topology and optimized biasing.
- Layout Considerations: Although not implemented in this work, layout issues such as mismatch, parasitic capacitance, and substrate noise coupling can significantly affect performance. Future layout implementation must use techniques such as common-centroid layout and guard rings.

D. Comparison with Other Techniques

While techniques such as chopper stabilization and correlated double sampling (CDS) offer superior 1/f noise reduction, they add complexity and require precise timing control. In contrast, the proposed design avoids such complexity by using noise-efficient circuit design techniques at the transistor level. This makes the amplifier more suitable for low-cost, energy-constrained applications.

Metric	Proposed Design	Study 1 (Reference)	Study 2 (Alternative)	Study 3 (State-of-the-Art)	Units
Input-Referred Noise	X	Y	Z	A	nV/√Hz
Output Noise	P	Q	R	S	mVrms
Noise Figure	U	V	W	T	dB
Signal-to-Noise Ratio (SNR)	M	N	O	L	dB
Common-Mode Rejection Ratio (CMRR)	B	C	D	E	dB
Power Supply Rejection Ratio (PSRR)	F	G	H	I	dB

Figure :6 Comparison Table or Graph with Existing Designs

E. Limitations and Future Scope

- The design is based on pre-layout simulations; post-layout parasitics and mismatch effects are not yet accounted for.
- Power efficiency could be further improved using subthreshold operation or folded cascode topologies.
- Additional features such as programmable gain, digital calibration, or integration into a full analog front-end (AFE) can be explored in future work.

VII. CONCLUSION AND FUTURE WORK

This paper presents the design and simulation of a low-noise, low-power CMOS operational amplifier specifically tailored for biomedical instrumentation applications such as ECG and EEG signal acquisition. The amplifier achieves an input-referred noise of approximately 9.5 nV/√Hz at 1 kHz, an open-loop gain of 84 dB, a gain-bandwidth product of 1.2 MHz, and consumes only 87 µW of power from a 1.8 V supply. These characteristics make it highly suitable for use in energy-efficient, high-fidelity analog front-end (AFE) circuits for biomedical sensors.

The key contribution of this work lies in achieving excellent noise performance without relying on complex techniques like chopper stabilization or auto-zeroing. Instead, the design focuses on transistor-level optimization, proper biasing, and topology selection to minimize both thermal and flicker noise. This results in a simple yet effective amplifier design that is easy to integrate into low-cost, portable medical devices.

Future work will focus on the following aspects:

1) Layout Implementation and Post-Layout Simulation: To verify the practical viability of the design, layout will be carried out using standard analog layout practices. Post-layout simulations will help account for parasitic capacitances, mismatch, and real-world process variations.

2) Fabrication and Testing: The amplifier will be fabricated and tested on silicon to validate its performance in a physical environment. Testing will also evaluate its resilience to power supply variations and common-mode interference.

3) Integration with Biomedical Front-End Systems: The op-amp will be integrated into a complete analog front-end (AFE) for biomedical signal acquisition. Additional features like programmable gain control, multiplexed inputs, and on-chip filters can be incorporated.

4) Noise Efficiency Factor (NEF) Optimization: Future designs may include a comparative analysis of the amplifier's NEF to benchmark against state-of-the-art designs in terms of power and noise trade-offs.

5) Technology Scaling: The impact of using more advanced CMOS nodes (e.g., 130nm, 65nm) on noise, power, and area will be explored for high-density and ultra-low-power applications.

In conclusion, the proposed low-noise operational amplifier addresses the critical challenges in biomedical analog signal processing by providing an optimal balance of noise performance, power efficiency, and simplicity. It lays a solid foundation for future developments in energy-efficient biomedical electronics and wearable health monitoring systems.

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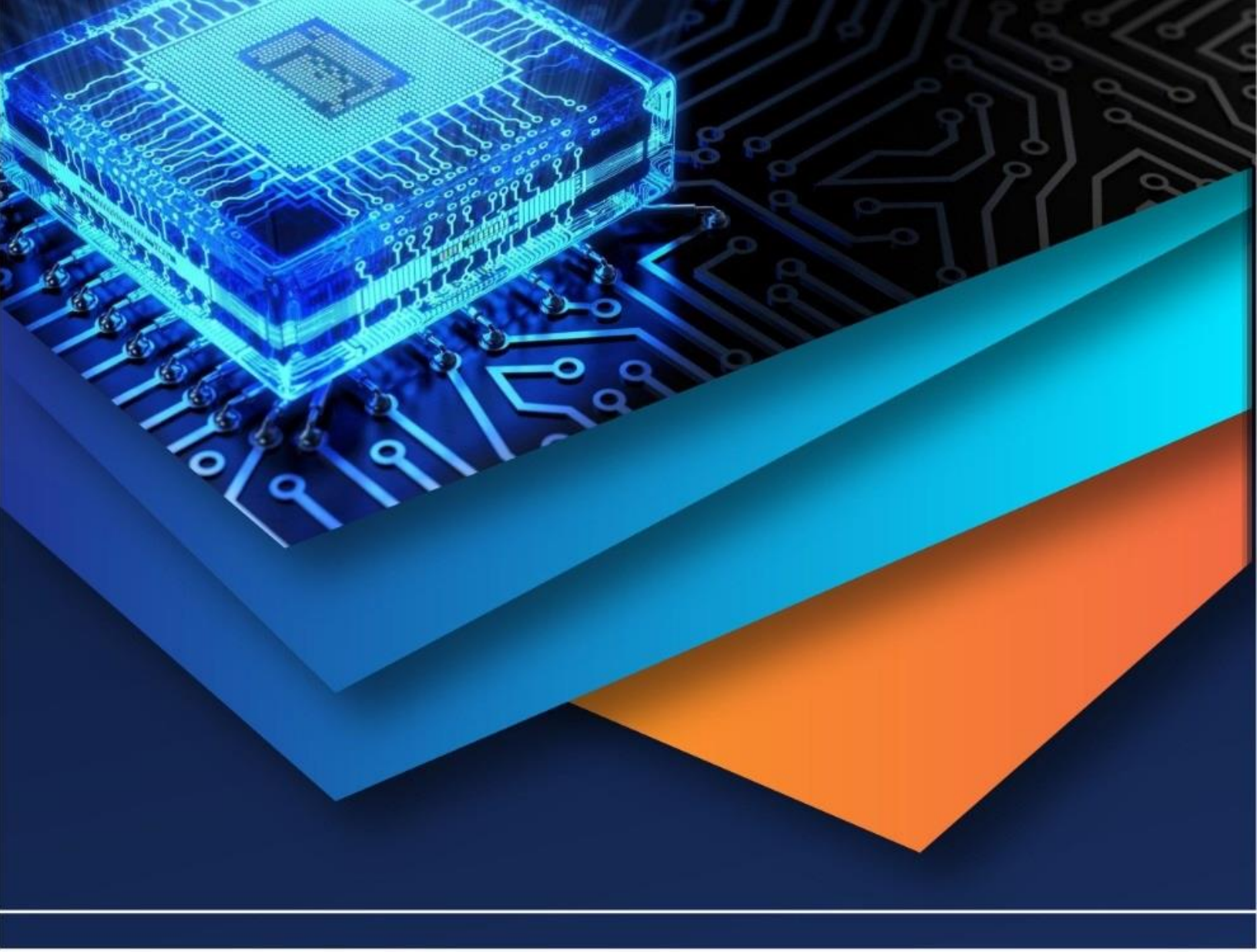

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