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Low-Power Retentive True Single Phase Clocked(TSPC) D-Flip-Flop with Redundant Precharge Free Operation

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Abstract: ***In this paper, optimizing power consumption of flip-flops (FFs) can significantly reduce the power of digital systems. In this article, an energy-efficient retentive true single- phase-clocked (TSPC) FF is proposed. With the employment of input-aware precharge scheme, the proposed TSPC FF precharges only when necessary. In addition, floating node analysis and transistor level optimization are employed to further ensure the high energy efficiency of the FF without significantly increasing the area.***

As The proposed Low power Retentive TSPC FF consumes less power which can be used in application like PLL (phased Lock loop) The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. The main Block For this is To design Phase frequency Circuit, Which is designed by using Low power Retentive TSPC FF To Give the better Results compare to conventional Circuit with a power Supply of 1.2 V by using Tanner EDA Tool.

Keywords: Flip-flop (FF), low voltage operation, low-power, redundant-precharge-free, true-single-phase-clocked (TSPC).

I. INTRODUCTION

Flip-flops are the basic building block of the data path structure. They allow for the storage of data, processed by combinational circuit and synchronization of operation at a given clock frequency. They are the fundamental building block of the digital electronics systems used in computers and many other types of systems. Flip flop can be either simple or clocked; simple devices are known as latches. A latch is level sensitive, and mainly used as storage element. And clocked devices are known as flipflop.

Flip-flop is edge sensitive means their output only changes on a single type of clock edge (positive or negative going edge). Flip-Flop is an electronic circuit that stores the logical state of one or more data input signal in response to a clocking pulse. They are often used in computational circuits to operate in selected sequences during recurring clock intervals to receive and maintain data for a limited time period sufficient for other circuits within a system to further process data [1]. Data is stored in flip-flop at each rising and falling edge of clock signal so that it can be applied as inputs to other combinational or sequential circuits, such flip-flops that store data on rising or falling edge of clock are referred as single edge triggered flip flops and the flip-flops that store data on both the rising and falling edge of a clock pulse are referred as double edge triggered flip-flops.

In CMOS circuit there are 3 sources of power dissipation, first static (leakage) power dissipation which is related to the logical states of the circuits and independent of switching activity. Second is short circuit power dissipation when both NMOS and PMOS transistor in the circuit is turned on simultaneously for short duration of time during switching. And as a result, direct current path between powers supply and ground is formed. And third is Dynamic (switching) power dissipation which is caused by power dissipation during switching activity [4]. Another important timing value for a flip-flop is the clock-to-output delay (t_p) i.e. the time taken by a flip-flop to change its output after the clock edge.

In digital electronics, the power-delay product which is also known as switching energy, is FOM (figure of merit) correlated with the energy efficiency of a logic gate. Power delay product is used to evaluate the performance of CMOS process. When the technology scales down, total power dissipation decreases and at the same time delay varies depends upon supply voltage, threshold voltage, aspect ratio, oxide thickness, and load capacitance [5].

II. RELATED WORK

1) Low power flip-flop designs featuring efficient embedded logic

A DML mode logic is introduced here which improves the speed performance of the design, also achieving significant energy consumption reduction.

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The large capacitance in precharge node is eliminated by the DDFF and DDFF-ELM designs by following a split dynamic node structure. The DDFF offers power reduction. The DDFF-ELM reduces pipeline overhead. 4-b Johnson up-down counter is used to magnify the performance improvement of the designs, to which the DML logic is introduced. An area, power, and speed efficient method are presented here that incorporates complex logic functions into the flip-flop. The DML logic used in DDFF-ELM helps to achieve low power and high-speed requirements.

2) Designing and Evaluating Redundancy-Based Soft-Error Masking on a Continuum of Energy versus Robustness

Near-threshold computing is an effective strategy to reduce the power dissipation of deeply-scaled CMOS logic circuits. However, near-threshold strategies exacerbate the impact of delay variations on device performance and increase the susceptibility to soft errors due to narrow voltage margins. The objective of this work is to develop and assess design approaches that leverage tradeoffs between performance and the resilience of fault masking coverage for various soft-error mitigation techniques. The primary insight from this work is identification of redundancy-based hardening techniques that can deliver increased benefits in terms of the fault coverage energy ratio (FCER) for the leveraged tradeoffs within iso-energy constraints at near-threshold voltage (NTV). Simulation results demonstrate that temporal redundancy approaches offer favorabletradeoffs in terms of FCER. They exhibit reduced impact on performance variations and achieve extensive soft fault masking, therefore improving the system robustness within acceptable delay constraints. Meanwhile, it is shown that a hybrid redundancy approach can be used to protect a low-power system to maintain throughput while tolerating soft errors. We demonstrate how the FCER metric can be used as an optimization parameter to guide circuit synthesis to meet performance and robustness goals. Finally, the impact of design diversity on spatial and hybrid redundancy at NTV is assessed in terms of FCER and delay variation to form overall recommendations regarding soft-error mitigation at NTV.

III. EXISTING SYSTEM

In existing system, several state-of-the-art low-power FFs are reviewed and the limitations are analyzed. All the listed FFs are single-phase-clocked FFs, which optimize the number of transistors related to the clock signal compared to TGFF.

In [13], a cross-charge control FF (XCFF) is proposed to reduce charged gate capacitance so as to reduce power consumption. As shown in Figures there is strong current contention at the output node of XCFF, so XCFF is not suitable for low voltage operation. Furthermore, XCFF needs to precharge some internal nodes no matter what the input data is, and extra power is wasted during the precharge and discharge operation.

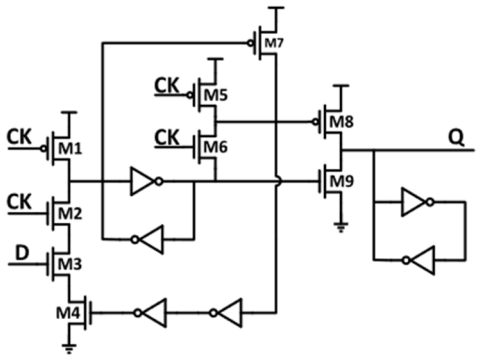


Figure – 1: XCFF

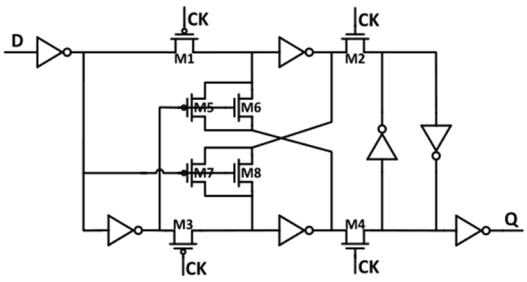


Figure – 2: ACFF

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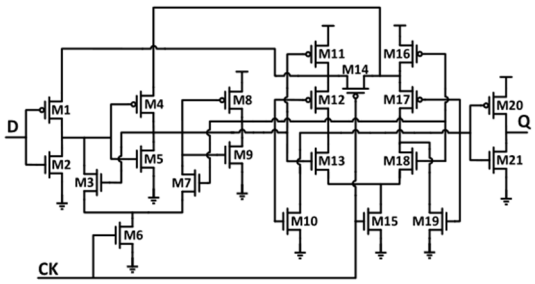


Figure – 3: TCFF

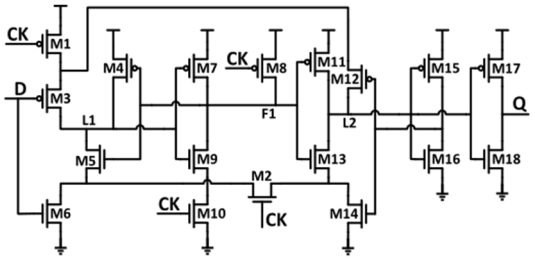


Figure – 4: SPC-18T

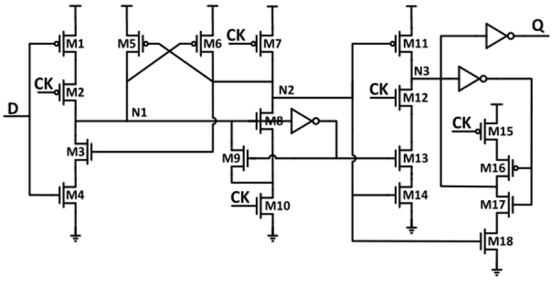


Figure – 5: S^2CFF

Table – 1: Existing System Limitations

Flip-flop	Limitation
TGFF	Large clock network, high power consumption
XCFF	Not suitable for low voltage operation, power is wasted during the precharge
ACFF	It fails at the low supply voltages
TCFF	Not suitable for the low power operation
SPC-18T FF	There is a chance of voltage leakage
S^2CFF	Not suitable for the low power operation
RTFF	It fails at the low supply voltages

IV. PROPOSED SYSTEM

In the proposed system, the structure of the proposed FF is described in detail. In order to minimize the power consumption of FF, any unnecessary transitions of internal nodes should be removed. We start with S^2CFF which is retentive TSPC and suitable for low voltage operations. To eliminate the redundant precharge and discharge operations, the FF is optimized by following steps. Firstly, unnecessary precharge operation of the internal node N2 is totally removed by the input-aware precharge scheme. Secondly, the floating node is under consideration to avoid short current which would greatly increase power consumption. Finally, unnecessary transistors are merged or removed to decrease the area.

Since the voltage of floating nodes may change after transition due to the leakage current, it is necessary to carefully analyze floating nodes to avoid the generation of short-circuit paths. With the insertion of the input-aware transistor, the voltage of the node N2 is no longer precharged to VDD at the negative half cycle of CK when the input is 0.

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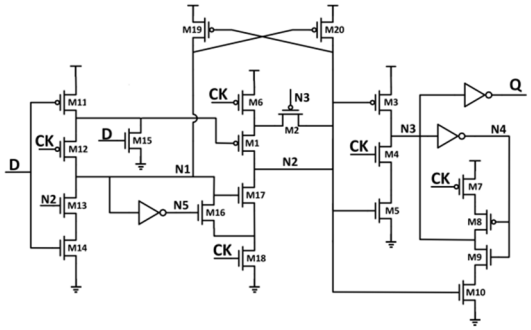


Figure-6: Schematic of the proposed System

When the output Q = 1, which means N3 = 0, the state of N3 is maintained by M9 and M10. To keep the transistor M3 OFF and the transistor M10 ON at that time, the voltage of N2 needs to keep high. In order to avoid N2 becoming floating while the next input data is 0, a transistor M2 is inserted to keep the voltage of N2. M2 is controlled by N3 and provides a precharge path for N2 when q = 1.

When the output Q = 0, N3 = 1, the state of N3 is maintained by M7 and M8. If the precharge path of N2 is cutoff at that time, which means the input data is 0 and the voltage of N2 does not charge to high when CK is low, the only effect is that M3 is ON, which will not lead to a short circuit path. When N3 = 1, CK = 0, and D = 0, the node N3 is isolated from its pull-down path (M4 and M5) through M4 (CK = 0), so the voltage of N2 has no effect on the node N3. Similarly, N1 is isolated from its pull-down path (M13 and M14) through M14 (D = 0), and the voltage of N2 has no effect on the node N1. Therefore, the floating of the node N2 is negligible in this case.

The function of the FF is correct and the redundant precharge operation is removed after adopting the input-aware precharge scheme and floating node analysis, but the FF can be further improved. The PMOS M11_1 which is used to generate the inversion of the input data can be merged into M11. But the NMOS M15 cannot be merged into M14 at the same time. Once both PMOS and NMOS are merged, which means the drain of M11 and M14 is directly connected, which can lead to functional failures of the FF. Thus, the NMOS M15 is reserved. The transistor M13 in S^2CFF is removed because it no longer plays a significant role in the proposed structure.

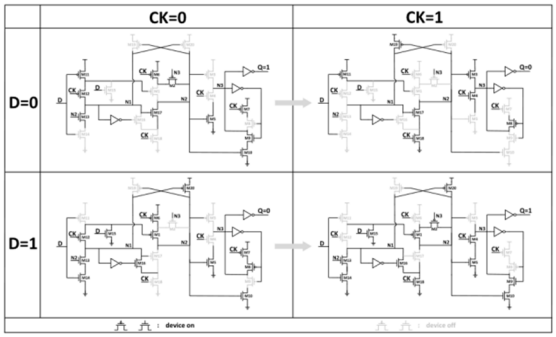


Figure-7: Operation diagram of the proposed FF at different D and CK

1) *High-to-Low Transition:* When CK is low, the node N1 is charged to VDD through M11 and M12, the node N2 is charged to VDD through M6 and M2, the node N3 keeps low through M9 and M10, and the output Q keeps high. At the rising edge of CK, N2 is discharged to GND through M17 and M18, and then M13 is turned off to isolate the FF from changes in the input data. At the same time, the node N3 is charged to VDD through M3, and then the output Q changes to 0. The voltage of N1 keeps high through M19, while the voltage of N2 keeps low through M17 and M18 during the positive half cycle of CK.
2) *Low-to-High Transition:* When CK is low, N2 is charged to VDD through M6 and M1, N1 is discharged to GND through M13 and M14, the node N3 keeps high through M7 and M8, and the output keeps low. At the rising edge of CK, the input data is isolated through M12, and the node N3 is discharged to GND through M4 and M5, then the output Q changes to 1. The voltage of N1 keeps low through M16 and M18, while the voltage of N2 keeps high through M20 during the positive half cycle of CK.

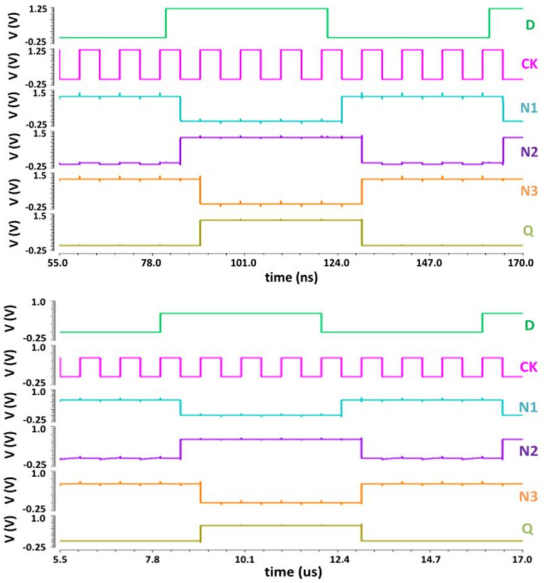


Figure-8: Transient waveform of the proposed FF

Algorithm

- Create the project in the S-edit
- Import all the library files.
- Construct the circuit by using the library files.
- And then for that circuit generate the Tspice file. 5. Then the code will be generated.
- Then we have to give the input and the operating 7. Signals by inserting the code.
- Print the output responses by giving the appropriate commands.
- Execute the code If there is any error check and rectify it and the execute the code.
- The responses will be displayed in the W-edit.

V. RESULTS

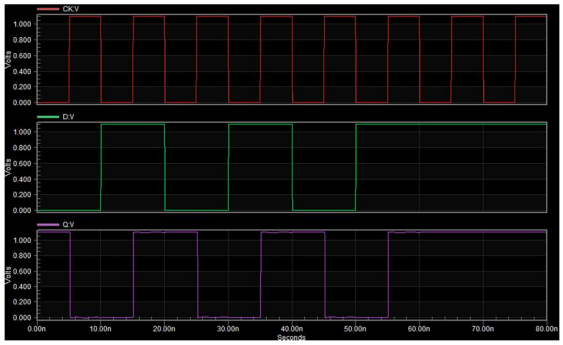


Figure-9: Proposed System outputs

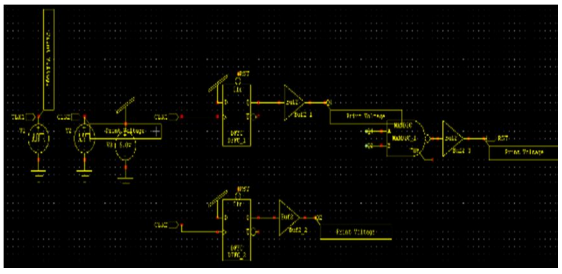


Figure-10: phase detector

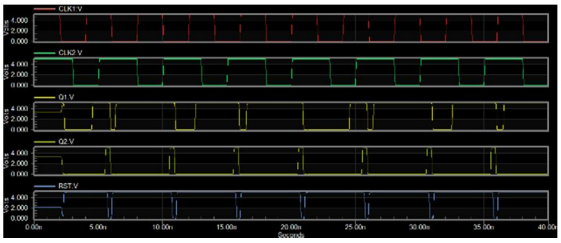


Figure-11: Waveforms

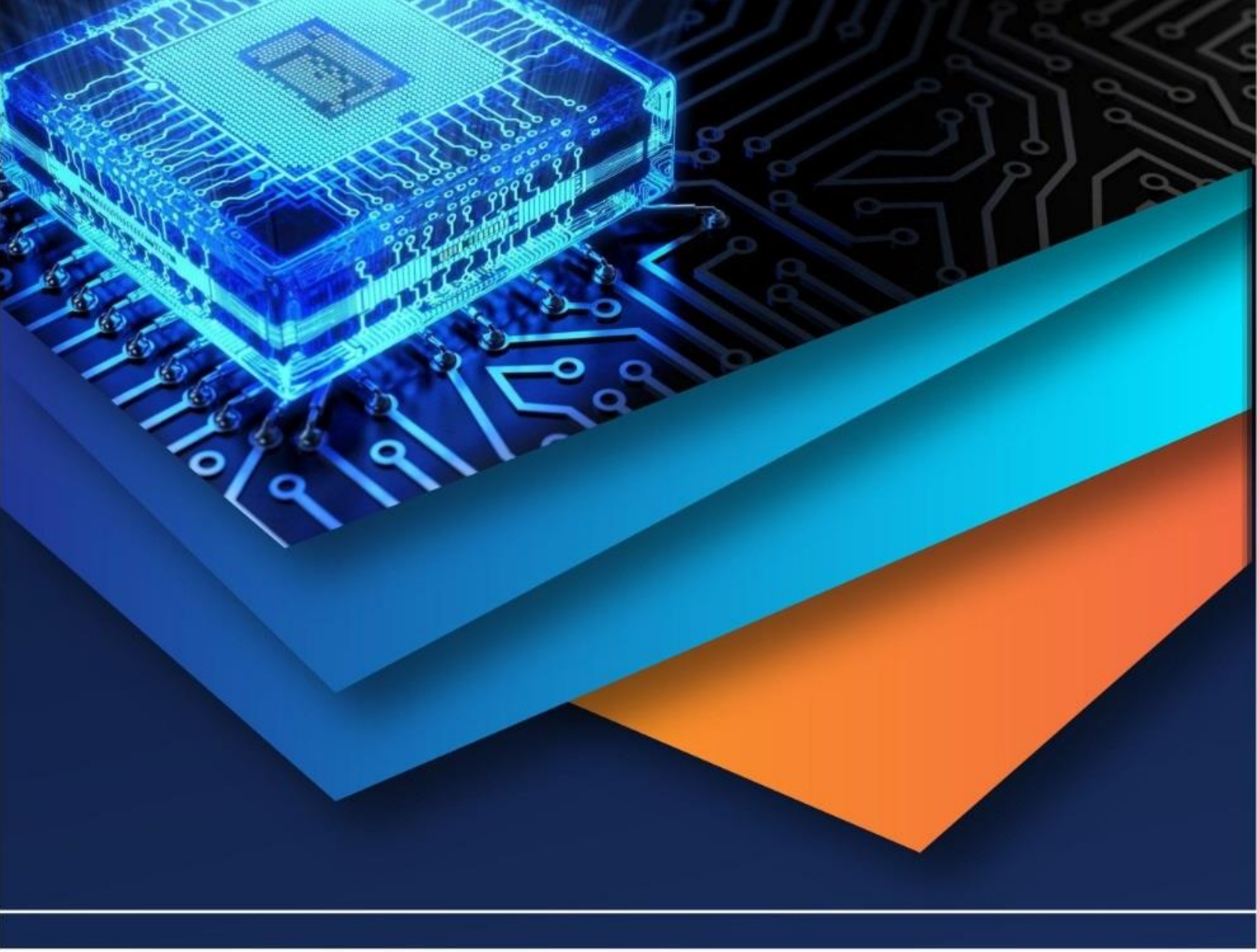
VI. CONCLUSION

By removing the redundant precharge and discharge operations, the power of the proposed flip-flop is greatly reduced and it will avoid the generation of the short-circuit paths.

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