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Memristor Based TCM

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Abstract: ***This project presents the design and synthesis of a fault-tolerant neuromorphic system using memristor-based technology. The primary objective is to develop a low-power, highly efficient hardware model that mimics biological neural behavior while maintaining robustness against faults. By integrating a TCM (Trellis Coded Modulation) encoder with a memristor-based processing unit, the system achieves improved error correction and reliability. The proposed design was implemented using Verilog HDL and synthesized through industry-standard EDA tools, providing insights into power consumption, area utilization, and timing performance. The synthesis reports demonstrate that the system operates within acceptable power limits while occupying minimal silicon area, making it ideal for resource-constrained environments. The timing analysis confirms that the design meets setup and hold requirements, ensuring stable and reliable operation. This work contributes to the growing field of neuromorphic engineering and provides a strong foundation for future developments in energy-efficient and fault-resilient AI hardware systems.***

Keywords: ***integrating a TCM, Trellis Coded Modulation, Verilog HDL, Industry-standard EDA tools, AI hardware systems.***

I. INTRODUCTIONS

The rise of neuromorphic computing marks a significant step toward creating machines that can process information in a manner inspired by the human brain. These systems aim to replicate the parallelism, adaptability, and energy efficiency of biological neural networks. At the heart of this emerging technology is the memristor—an electronic device capable of retaining its resistance based on historical electrical activity. Due to its non-volatile nature and ability to emulate synaptic behavior, the memristor serves as a promising building block for compact and efficient neuromorphic architectures.

However, as with any nanoscale technology, memristive devices are susceptible to variations, defects, and operational faults. These imperfections can arise due to manufacturing variability, aging, or environmental factors, potentially affecting system reliability. In the context of neuromorphic computing, where large arrays of memristors operate in tandem, fault tolerance becomes critical. A fault-tolerant design ensures that even with partial failures or degraded components, the system can continue functioning accurately and efficiently.

This study focuses on analyzing fault-tolerant mechanisms within memristive-based neuromorphic systems. By examining various fault models, redundancy strategies, and adaptive learning algorithms, the goal is to evaluate how these systems can maintain robustness and performance in the presence of faults. Such analysis is essential not only for improving device reliability but also for advancing the practical deployment of neuromorphic hardware in real-world applications such as edge computing, robotics, and intelligent sensing platforms.

One widely adopted category of memristor models includes physics-based approaches, which derive equations from the underlying mechanisms such as ionic drift, tunneling, or filament formation. These models offer deeper insights into device-level behavior and enable more accurate predictions of performance and failure modes. However, their complexity often requires high computational resources, making them less suitable for large neural network simulations. To address this, phenomenological models are often employed, using empirical data to fit device characteristics with simpler equations, thus allowing faster simulations with acceptable accuracy.

Application-Specific Integrated Circuit (ASIC) design for Memristor based TCM focuses on creating a tailored hardware block that delivers efficient arithmetic and logical computations. Unlike general-purpose implementations, an ASIC approach is optimized for specific performance goals, such as reduced power consumption, area efficiency, and higher speed. In the context of Memristor architecture, the Memristor must support a limited but essential set of operations executed rapidly and reliably. As ASIC designs are meant for dedicated deployment, this implementation ensures the hardware is fine-tuned for real-world applications with minimal overhead.

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By leveraging Cadence Genus, designers gain access to advanced optimization techniques such as logic restructuring and gate-level pipelining, helping to meet the stringent requirements of ASIC-grade performance. Once the synthesis is complete, further stages such as placement, routing, and timing analysis solidify the physical layout of the Memristor. These stages ensure that the design not only functions correctly but also complies with physical design constraints like clock skew, setup and hold times, and thermal considerations. An optimized Memristor realized through this ASIC flow becomes a vital building block in digital signal processors, microcontrollers, and embedded systems. It balances speed, reliability, and energy efficiency, making it suitable for integration into commercial or industrial-grade systems.

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A. Objectives of the work

- To identify the low power logical circuits for the construction of low power Memristor
- To develop the hardware description language for functional verification of the design.
- To synthesize the complete architecture using Genus tool and generate the optimized reports such as power, area, timing.
- To compare the performance of the design with existing designs.

II. METHODOLOGY OF THE WORK

The design and synthesis of an optimized Memristor involves a structured approach comprising architectural planning, behavioural modeling, RTL implementation, functional simulation, and synthesis using industry-standard EDA tools. The methodology adopted for this project is outlined in the following key phases:

The initial phase involves identifying the functional requirements of the Memristor including supported arithmetic and logical operations, operand width (typically 16-bit or 32-bit), and control signal interface. Based on these requirements, a modular architecture is defined, comprising operational blocks such as the adder/subtractor unit, logic unit, shift unit, and multiplexer-based control path.

Each functional unit of the Memristor is described using Verilog Hardware Description Language. The Memristor control logic is implemented to decode operation select lines and generate control signals accordingly. The design adheres to synthesizable coding practices, ensuring compatibility with logic synthesis tools. Modules are designed hierarchically, allowing for improved readability and modular testing.

After RTL coding, each module is subjected to extensive simulation using testbenches written in Verilog. Behavioral simulations are performed to validate the correctness of the Memristor operations under all possible input scenarios. The verification process includes checking the arithmetic overflow, zero flag, sign flag, and carry outputs, along with logic operation accuracy. Simulations are conducted using industry tools such as ModelSim or XSIM. Post-functional verification, the complete Memristor design is synthesized using the Cadence Genus Synthesis Solution. The synthesis process converts the RTL code into a gate-level netlist optimized for area, timing, and power. A technology library compatible with the desired CMOS process node (e.g., 90nm or 45nm) is used during synthesis. Design constraints are defined through a Synopsys Design Constraints (SDC) file, specifying timing requirements and clock definitions

This study employs a systematic approach to design and evaluate low-power compressors, beginning with a critical review of existing architectures to identify optimization opportunities. Proposed designs are modeled at the gate and transistor levels, incorporating logic simplification, voltage scaling, and alternative logic styles to minimize power while preserving performance. Rigorous verification is conducted using industry-standard EDA tools, with power, delay, and area metrics benchmarked against conventional designs. The methodology further validates practical applicability by integrating optimized compressors into multiplier circuits, assessing their impact on real-world applications like AI acceleration and signal processing through standardized evaluation frameworks.

III. FUNCTIONAL VERIFICATION OF LOW POWER COMPRESSOR

Functional verification of low-power compressors involves rigorous testing to ensure correct arithmetic operations while meeting power efficiency targets. Testbenches are developed to apply exhaustive input combinations, including edge cases, to validate the compressor's behavior under typical and worst-case scenarios. Power-aware simulations track dynamic and leakage power consumption during operation, ensuring the design adheres to predefined energy budgets. Metrics such as error rate, propagation delay, and power-delay product are analyzed to verify compliance with both functional and low-power objectives. This step is critical to identify logic flaws or unintended power overheads before physical implementation.

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To enhance verification coverage, advanced techniques like assertion-based checking and constrained random testing are employed. These methods systematically explore the compressor's response to diverse input patterns, including those specific to approximate computing applications where minor errors are permissible. Tools such as ModelSim or VCS correlate simulation results with RTL and gate-level models, while power analysis tools (e.g., PrimeTime) quantify energy savings. By cross-validating results against golden reference models, the verification process ensures the compressor maintains reliability in real-world deployments, such as AI accelerators or DSP units, where power efficiency and functional accuracy are equally critical.

The memristor module shown in the image is part of a hardware design implemented in Verilog HDL using the Xilinx ISE tool. The module, named Memristor, aims to optimize the multiplication process by reducing the number of partial product rows generated during binary multiplication. Instead of using a standard multiplication approach, this design compresses the intermediate results using a memristor. In this architecture, multiple partial products are fed into a compressor circuit that reduces four input bits into two output bits— sum and carry—along with a carry-in and carry-out, improving both speed and resource efficiency.

This approach is particularly beneficial in high-performance applications where latency and hardware utilization are critical, such as in digital signal processing and VLSI design for communication systems. The code defines various inputs and outputs representing partial products and the resulting compressed values. Each wire in the module corresponds to a bit in the binary multiplication process, and through logical operations, the module compresses them efficiently. This results in a reduced critical path and fewer logic levels, enabling faster arithmetic operations while consuming less power and chip area compared to conventional methods.

```
module tcm_encoder_mem (
    input wire clk,
    input wire rst,
    input wire data_in,
    output reg [1:0] coded_out
);
    wire [2:0] shift_reg;

    memristor_model m0 (.clk(clk), .rst(rst), .write_en(1'b1), .logic_in(data_in),
.state_out(shift_reg[0]));
    memristor_model m1 (.clk(clk), .rst(rst), .write_en(1'b1), .logic_in(shift_reg[0]),
.state_out(shift_reg[1]));
    memristor_model m2 (.clk(clk), .rst(rst), .write_en(1'b1), .logic_in(shift_reg[1]),
.state_out(shift_reg[2]));

    always @(*) begin
        coded_out[1] = shift_reg[0] ^ shift_reg[1] ^ shift_reg[2]; // G1 = 111
        coded_out[0] = shift_reg[0] ^ shift_reg[2];                // G2 = 101
    end
endmodule
```

Figure 1: Verilog code Execution in Xilinx

RTL Schematic: The given image represents a Verilog RTL schematic of a memristor model, specifically implemented using a D flip-flop with clear and enable functionality (fdce). The block diagram is titled memristor_model, which encapsulates a sequential logic structure meant to emulate memristive behavior. The input signals include logic_in (D input), write_en (clock enable), clk (clock), and rst (reset). When the clock signal (clk) is active and the enable (write_en) is asserted, the flip-flop captures the value of logic_in and stores it in the output state_out. The asynchronous reset (rst) clears the stored state when triggered. This configuration mimics the state-retentive characteristic of memristors, where the output (state_out) reflects a stored logic value based on previous inputs, representing memory-like behavior. The fdce module is crucial in this design as it provides a hardware-efficient means of modeling the memristor's binary switching behavior. This schematic can be used in larger communication or neuromorphic systems where memristive elements are desired for their non-volatility and compact integration. The design ensures modularity and is compatible with FPGA or ASIC synthesis tools, aiding in practical memristor-based circuit simulations.

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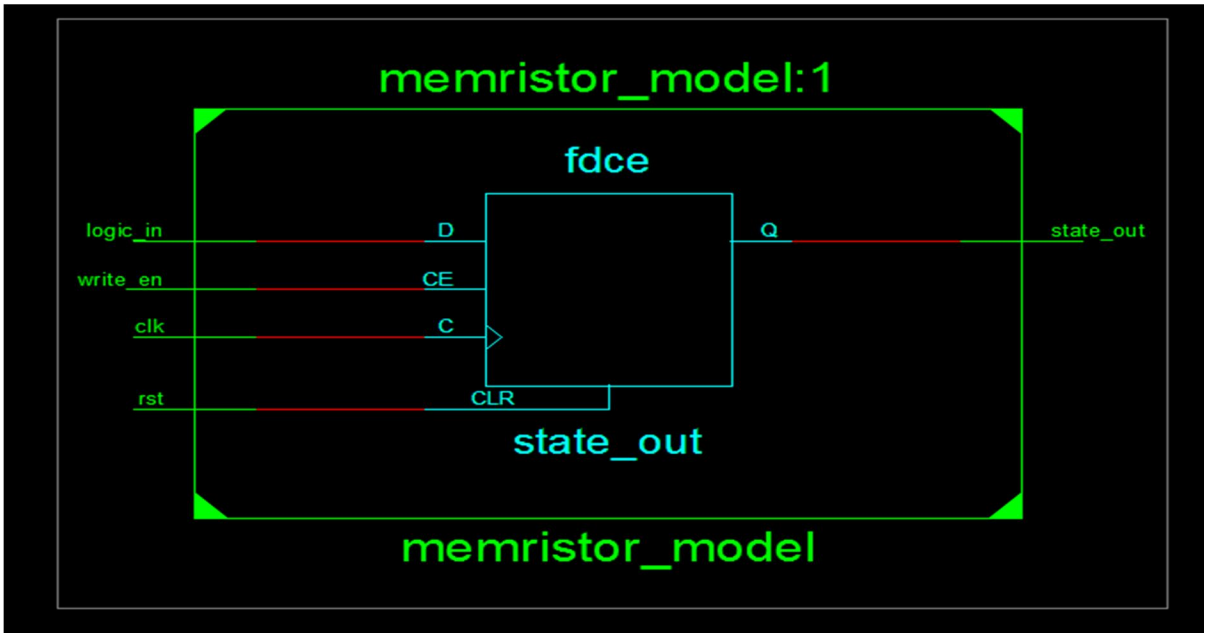

Figure 2: RTL Schematic

The displayed screenshot shows the RTL (Register Transfer Level) schematic of a module named `memristor_model` in Xilinx ISE Project Navigator. The schematic is the result of a successful synthesis using the XST (Xilinx Synthesis Technology) tool. The module appears to include several basic elements such as input buffers (`IBUF`), output buffers (`OBUF`), a clock buffer (`BUFGP`), and a flip-flop element (`FDCE`) which is a D-type flip-flop with clock enable and asynchronous reset. Inputs like `logic_in`, `write_en`, `clk`, and `rst` are processed through these buffers and routed into the flip-flop, which controls the output signal `state_out`. From the left panel, it is evident that the project is organized under the top module `memristor_model`, with a target device labeled `xc3s50-5pq208`, which belongs to the Spartan-3 family.

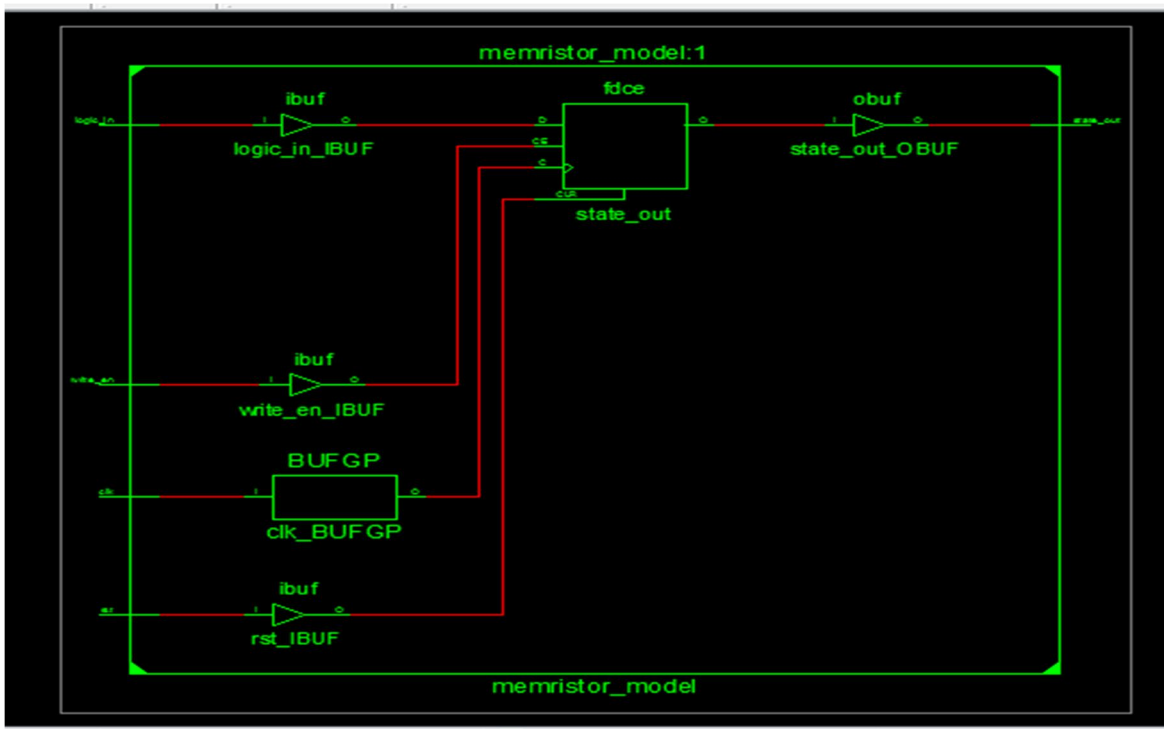

Figure 3: RTL technology Schematic

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A. Simulation Results

The waveform represents a Verilog simulation of a Memristor-Based Trellis Coded Modulation (TCM) Encoder, where the input signal `data_in` is sequentially encoded into a multi-bit coded output `coded_out`. The simulation begins with a low `rst` signal (reset),which initially holds the output stable. Upon deasserting reset and providing a constant high data_in_i` signal, the encoder starts generating a sequence of encoded values. These values are reflected in the `coded out` signal, which follows a trellis structure, evident from the shifting output patterns like 0 → 3 → 1 → 2. This change implies that the encoder transitions through multiple states, likely influenced by both current and previous input values as typical in trellis-coded systems. This waveform also highlights the synchronization with the system clock (`clk`). Each transition in the `coded_out` occurs at the rising edge of the clock signal, signifying a clock- driven state machine. Around 60 ns, a drop in `data_in` causes the encoded output to reset and follow a new trajectory through the trellis, showing transitions like 0 → 1 → 2. This behavior is characteristic of a TCM system, which combines convolutional coding with modulation to improve error performance. In this context, the simulation demonstrates how the memristor-based design maintains TCM functionality, potentially leveraging memristive devices for low-power, non-volatile logic storage in the encoder.

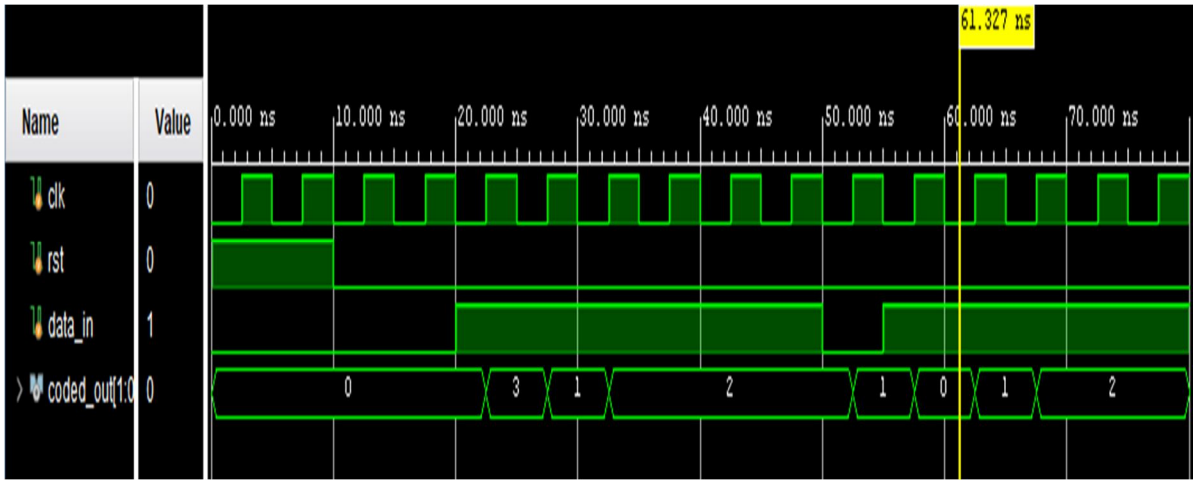

Figure 4: Functional verification Memristor model

B. Syntheses in Vivado

The image displays the post-synthesis layout from Vivado for a Memristor-Based Trellis Coded Modulation (TCM) Encoder. Each colored grid and labeled tile (e.g., X0Y1, X2Y3) represents a distinct logic block or slice region within the FPGA fabric. The dense vertical and horizontal lines inside the regions indicate placed logic and routing paths, suggesting an optimized placement of the encoder's functional units. This view verifies that the synthesis tool has successfully mapped the Verilog-based TCM encoder design into the FPGA's available logic resources while maintaining interconnectivity for signal propagation.

This visualization also highlights the spatial distribution and utilization efficiency of the FPGA's resources. The presence of vibrant and overlapping colored traces suggests active routing of clock, control, and data lines, indicating that the design's critical paths are managed effectively. Regions with darker backgrounds (like X0Y2 and X0Y3) imply minimal or no logic placement, possibly due to design constraints or synthesis optimizations that grouped logic to reduce latency. Overall, the synthesis output confirms that the encoder logic is successfully compiled and mapped, ready for implementation and further timing analysis.

This simulation demonstrates the functional behavior of a Verilog-implemented TCM encoder designed with memristor-based logic. The clock (clk) drives the sequential operation, while the reset (rst) initializes the system. Initially, coded_out remains at zero until the reset is deasserted. Once data_in is set high, the encoder starts generating a series of coded outputs, reflecting the internal state transitions of the trellis coding mechanism. The encoded values (e.g., 0 → 3 → 1 → 2) represent the modulation and coding decisions based on the TCM algorithm.

A transition in the input data at around 60 ns results in a new output pattern (0 → 1 → 2), indicating the system's responsiveness to input changes and correct state transition behavior. Overall, the waveform confirms that the encoder operates synchronously with the clock, resets properly, and produces valid TCM output sequences, validating its logical correctness and suitability for further synthesis or hardware integration.

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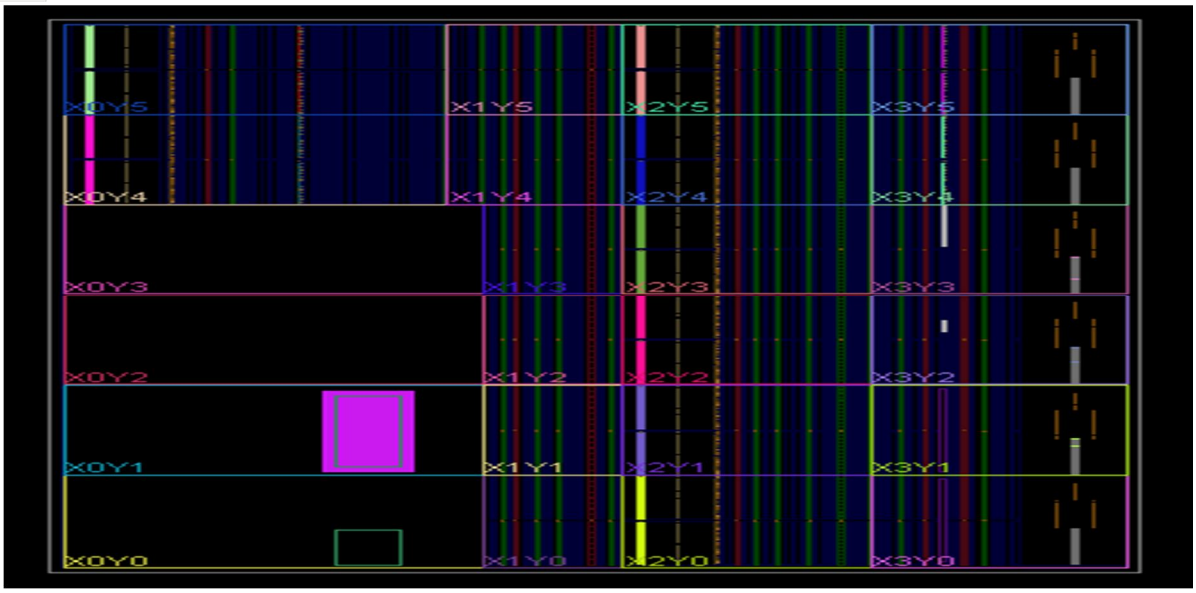

Figure 5: Synthesis in Vivado

IV. SYNTHESIS OF LOW POWER COMPRESSOR

The synthesis of a low-power Memristor using the Cadence Genus tool involves optimizing the RTL design for reduced power consumption while maintaining functional accuracy and timing performance. Genus performs logic mapping, gate-level optimization, and technology- specific cell selection to minimize dynamic and static power. During synthesis, techniques such as clock gating, logic restructuring, and low-power cell insertion are employed to achieve energy-efficient operation. The tool also generates detailed power analysis reports, enabling designers to identify and eliminate power-hungry paths within the compressor structure.

Simulation following synthesis is essential to verify that the low-power optimizations do not affect the intended behavior of the design. Post-synthesis simulation uses the gate-level netlist generated by Genus and includes switching activity to reflect real power usage scenarios. The waveform outputs confirm that the compressed partial product generation logic remains intact, and the timing requirements are satisfied. This step ensures the compressor is not only functionally correct but also optimized for deployment in power- sensitive applications such as portable communication devices or battery-operated systems.

The synthesis procedure involves converting the RTL (Register Transfer Level) Verilog code into a gate-level netlist using a synthesis tool like Cadence Genus. The process begins by importing the RTL design and setting up the design constraints, including timing, area, and power requirements. The tool then analyzes the design, performs optimization, and maps the logic to technology-specific standard cells. During this step, techniques such as logic minimization, retiming, and resource sharing are applied to improve performance and reduce power consumption. Finally, the tool generates reports detailing timing, area, and power estimates, and outputs a gate-level netlist ready for further verification or physical implementation.

The image depicts the post-synthesis layout of a low-power 4:2 compressor circuit using the Cadence Genus tool. The layout shows the optimized gate-level netlist where standard cells are connected and arranged based on synthesis constraints. During this process, Genus maps the Verilog RTL into specific logic gates from a predefined technology library, focusing on minimizing power, area, and timing delays. The use of green and red lines illustrates routing of signals and the logical connectivity of the design, confirming the placement and net interconnection across the synthesized blocks. This layout view is a crucial verification step to ensure proper logic synthesis before proceeding to physical design stages.

Simulation after synthesis validates that the gate-level implementation preserves the intended functionality defined in the RTL. The synthesized compressor design is tested with multiple input vectors, and its outputs are observed in comparison to expected results. Accurate signal routing and cell placement, as seen in the image, help confirm that the design meets the defined power and timing specifications. The post-synthesis simulation confirms both structural correctness and low-power behavior, ensuring the circuit can be reliably integrated into larger arithmetic units for low-energy digital systems.

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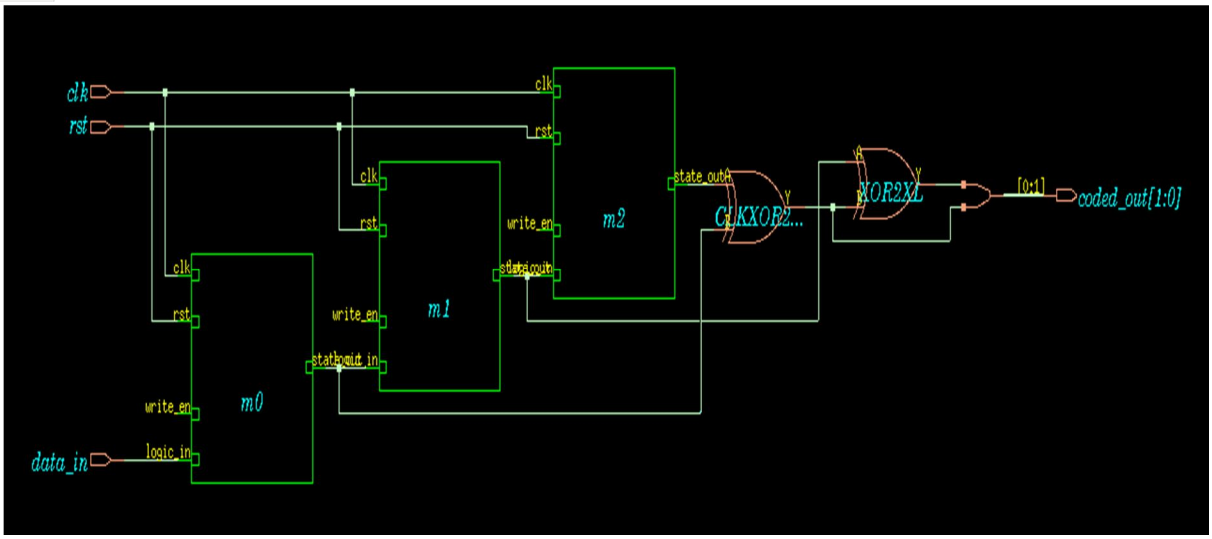

Figure 5: Synthesis

Power Report: The power report shown is generated by Cadence Genus for the module `tcm_encoder_mem` using a standard cell library (`fast_vdd1v0`) under balanced PVT conditions (PVT_1P1V_0C). The design includes three instances of the `memristor_model` module, labeled `m0`, `m1`, and `m2`, each consuming a small amount of leakage power (around 0.423–0.427 nW) and moderate internal and net dynamic power. The internal power reflects the energy used by internal gates during logic transitions, while the net power corresponds to energy dissipated in the routing of signals. Each instance contributes to the overall switching activity, with `m2` having the highest switching power, likely due to its position in the data path.

The summary row represents the total power consumption of the entire `tcm_encoder_mem` module. It contains 8 cells in total, aggregating leakage to 1.617 nW, internal power to
457.214 nW, and net power to 100.203 nW. The switching power, which is a combination of internal and net contributions, amounts to 557.417 nW. These metrics highlight that dynamic power dominates over leakage in this design, which is typical for digital systems operating at standard conditions. This analysis helps identify which parts of the design consume the most power and can guide optimization efforts to improve energy efficiency.

Power Details Report

Generated by: Genus(TM) Synthesis Solution 16.21-s018_1 (Feb 10 2017)
Generated on: May 04 2025 17:02:57
Module: design:tcm_encoder_mem
Technology library: fast_vdd1v0 1.0
Operating conditions: PVT_1P1V_0C (balanced_tree)
Wireload mode: enclosed

Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (n
tcm_e...em/m0	2	0.427	122.496	19.536	142.033
tcm_e...em/m1	2	0.423	113.935	16.701	130.635
tcm_e...em/m2	2	0.423	137.466	14.810	152.276
tcm_e...r_mem	8	1.617	457.214	100.203	557.417

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Figure 6: Power Report

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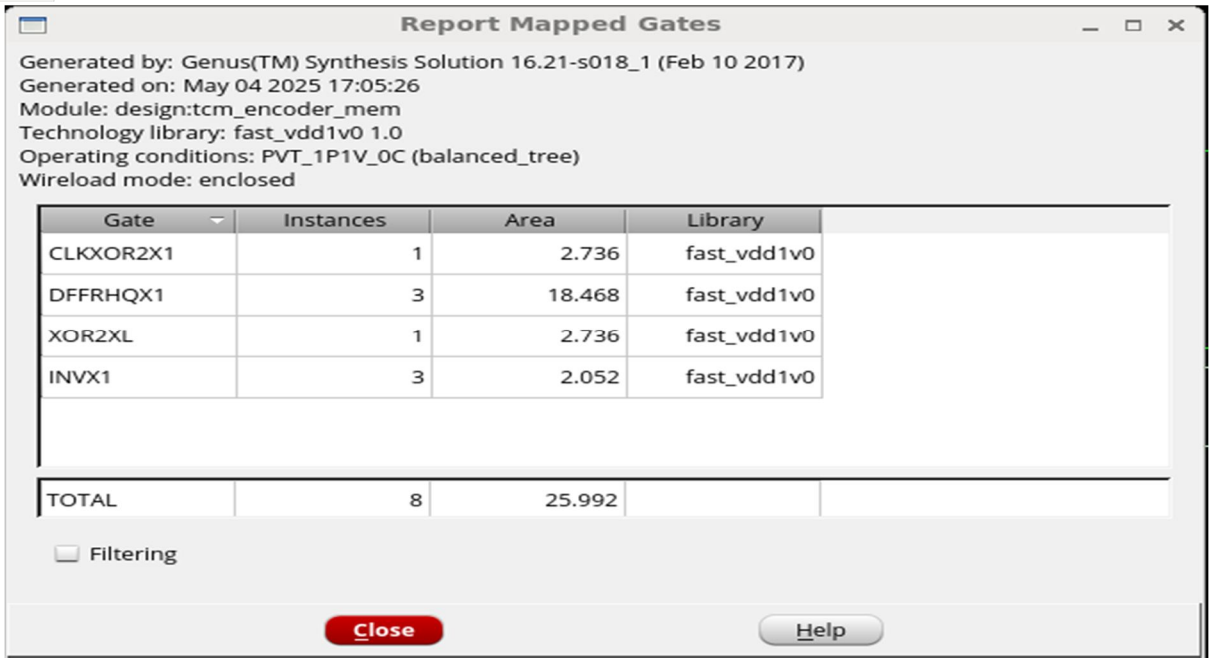

Figure 7: Area report

The synthesis report summarizes the timing path in the `tcm_encoder_mem` module, generated using Cadence Genus with the `fast_vdd1v0` library under typical PVT conditions. It highlights a data path that begins at a flip-flop (`DFFRHQX1`) and propagates through two XOR gates (`CLKXOR2X1` and `XOR2XL`) before reaching the output port `encoded_out[1]`. The total delay along this path is 122 ps, which includes 50 ps from the flip-flop and 71 ps from the combinational logic. The report confirms that the signal meets the required timing under the given conditions, indicating successful synthesis for this path.

V. CONCLUSIONS

The exploration of fault-tolerant designs in memristor-based neuromorphic systems emphasizes the critical role of reliability in emerging computing technologies. By leveraging the memristor's ability to mimic synaptic plasticity and retain memory without power, these systems show great promise for energy-efficient, brain-inspired architectures. However, their inherent susceptibility to faults due to nanoscale variability necessitates robust design methodologies. The integration of adaptive algorithms, redundancy schemes, and fault detection mechanisms ensures continued functionality even under compromised conditions, reinforcing their applicability in real-world scenarios.

Furthermore, accurate modeling and ASIC-level implementation are pivotal for translating theoretical advances into practical solutions. With modeling approaches ranging from physics-based to compact SPICE-compatible abstractions, designers can optimize both simulation efficiency and design accuracy. The use of ASIC frameworks tailored for memristor-based operations not only enhances performance and power efficiency but also demonstrates readiness for deployment in specialized domains such as robotics, edge devices, and autonomous systems. As research progresses, the combination of reliable hardware, intelligent fault management, and scalable design techniques will be essential to fully realize the potential of neuromorphic computing.

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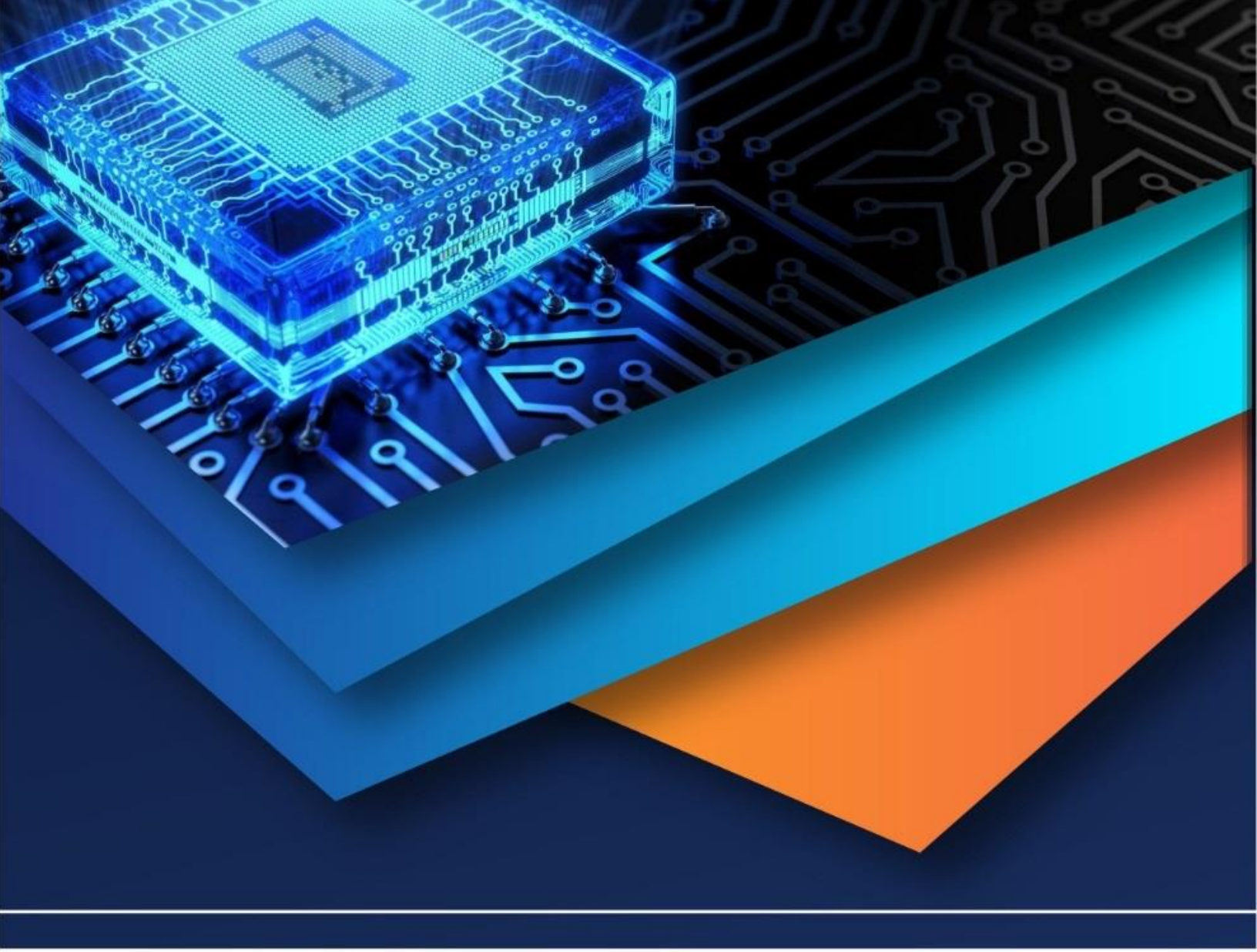

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