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# Multi-Level Inverter Modeling and Simulation Using Various and Complex PWM Modulation in MATLAB/Simulink

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**Abstract:** This paper presents a detailed comparison of several multilevel inverter (MLI) topologies, including Neutral Point Clamped (NPC), Flying Capacitor (FC), Cascaded H-Bridge (CHB), and Modular Multilevel Converter (MMC). Application domains, control schemes, modularity, voltage balancing, and structural complexity are the main topics of the analysis. Each topology's component requirements, modulation techniques, and performance trade-offs are examined. Simulation results validate the theoretical evaluation and show how each topology is suitable for specific applications such as electric drives, renewable energy systems, and high-voltage direct current (HVDC) transmission. The study aims to assist researchers and engineers in selecting the optimal MLI topologies according to the requirements of specific applications.

**Index Terms:** Multi-level Inverter, PWM, SVPWM, SHE, MATLAB/Simulink, THD, Modeling.

## I. INTRODUCTION

The development of power electronic systems has brought about significant changes in power conversion and control. Among these developments, Multi-Level Inverters (MLIs) have gained popularity as a solution for medium- and high- power applications because of their ability to generate a high- quality output voltage with lower harmonic content, lower electromagnetic interference (EMI), and less voltage stress on power semiconductor devices [1], [2].

Conventional two-level inverters' performance is often limited by high switching losses and harmonic distortion, especially in high-voltage applications. Multi-level inverters such as Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) improve voltage resolution by generating a stepped output waveform from multiple DC levels [3]. Large filters are no longer necessary thanks to these topologies, which also improve system efficiency.

The effectiveness of MLIs is directly influenced by the modulation technique employed. Although they are easy to use, simple modulation techniques like Sinusoidal Pulse Width Modulation (SPWM) do not maximize harmonic performance or DC bus utilization [4]. Advanced modulation techniques such as Space Vector Pulse Width Modulation (SVPWM), Level-Shifted PWM (LSPWM), and Selective Harmonic Elimination (SHE) have been developed to address these issues [5], [6]. These methods enhance waveform quality, reduce switching frequency, and enable selective control of harmonic components. Modeling and simulation are key components of MLI system design and performance analysis. MATLAB/Simulink provides a comprehensive environment for accurately and flexibly modeling inverter circuits and implementing control strategies [7]. It enables a detailed analysis of switching behavior, harmonic distortion, and thermal performance under various modulation schemes.

This paper focuses on modeling and simulating three- and five-level inverter topologies using multiple PWM techniques in MATLAB/Simulink. The goal is to evaluate the performance in terms of total harmonic distortion (THD), voltage waveform quality, and control complexity. The rest of the paper is organized as follows: The MLI topologies are explained in Section II, different PWM techniques are described in Section III, the simulation model is presented in Section IV, results and comparison are discussed in Section V, and the paper is concluded in Section VI.

## II. OVERVIEW OF MULTI-LEVEL INVERTER TOPOLOGIES

A power electronic converter known as a multi-level inverter (MLI) creates a stepped AC output by combining several DC voltage levels. They use fewer filters, lower electromagnetic interference (EMI) and  $dv/dt$  stress, and greatly improve the quality of the output waveform [1], [2]. Diode-Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) are the three main multilevel inverter topologies; each has a distinct structure and range of applications.

A. Diode-Clamped(NeutralPointClamped)MLI

The Diode-Clamped Multilevel Inverter (DCMLI), also known as the Neutral Point Clamped (NPC) inverter, is one of the earliest and most widely used multilevel topologies. Clamping diodes are introduced to allow the use of a single DC source for multiple voltage levels while reducing the voltage stress on power devices.

1) Structure and Working Principle: A typical  $n$ -level NPC inverter consists of:

- $2(n-1)$  switching devices per phase.
- $(n-2)$  clamping diodes per phase.
- Single DC source split into  $(n-1)$  equal parts using capacitors.

For a three-level NPC inverter, the output voltage ( $V_o$ ) with respect to the midpoint (neutral) can be represented as:

$$V_o = \begin{cases} +V_{dc}/2 & \text{if } S_1, S_2 = \text{ON} \\ 0 & \text{if } S_2, S_3 = \text{ON} \\ -V_{dc}/2 & \text{if } S_3, S_4 = \text{ON} \end{cases} \quad (1)$$

where  $S_1$  to  $S_4$  are the series-connected switches per phase.

2) Voltage Level Generalization: For an  $n$ -level NPC inverter, the number of distinct output voltage levels is:

$$L = 2n - 1 \quad (2)$$

However, in practical symmetric design using a single DC source split into equal voltages, the output voltage levels are:

$$V_o = -\frac{(n-1)V_{dc}}{2}, \dots, 0, \dots, +\frac{(n-1)V_{dc}}{2} \quad (3)$$

3) Switching Logic Algorithm: A simplified logic to determine the switching states based on desired output voltage level is shown below:

Output Level	$S_1$	$S_2$	$S_3$	$S_4$
$+V_{dc}/2$	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF
$-V_{dc}/2$	OFF	OFF	ON	ON

4) Advantages and Limitations:

Advantages:

- Reduced voltage stress per switch.
- Good harmonic performance.
- Suitable for medium-voltage industrial drives.

Limitations:

- Unequal capacitor voltage balancing in higher levels.
- Diode count increases significantly with  $n$ .
- Applications: This topology is extensively used in:
  - Industrial motor drives.
  - Medium-voltage variable-speed drives.
  - UPS systems and grid-connected inverters

B. Flying Capacitor Multilevel Inverter (FCMLI)

The Flying Capacitor Multilevel Inverter (FCMLI) topology, which employs capacitors as voltage clamping devices rather than diodes, enables higher voltage levels and more adaptable voltage control. This structure allows for better voltage balancing between switching devices, but at the cost of additional components and more complex control. [?], [?].

1) *Structure and Operation Principle*: An  $n$ -level FCMLI consists of:

- $2(n-1)$  switching devices per phase.
- $(n-1)(n-2)/2$  flying capacitors.
- A single or multiple DC sources, typically one, to synthesize the required output voltage level. The output voltage levels for a phase-leg can be expressed as:

$$V_o = \sum_{i=1}^{n-1} a_i \cdot \frac{V_{dc}}{n-1}, \quad a_i \in \{-1, 0, 1\} \quad (4)$$

where  $a_i$  is the state of the flying capacitor stage, determining whether it contributes positively, negatively, or is bypassed.

2) *Voltage Level and Capacitor Count*: For an  $n$ -level FCMLI, the total number of distinct output levels is:

$$L = 2n - 1 \quad (5)$$

The number of required flying capacitors per phase leg is given by:

$$C = \frac{(n-1)(n-2)}{2} \quad (6)$$

3) *Basic Switching Logic*: The switching states are carefully selected to:

- Synthesize the desired output voltage.
- Maintain charge balance across flying capacitors.

An example switching table for a 3-level FCMLI is shown below:

Output Voltage	$S_1$	$S_2$	Flying Capacitor Status
$+V_{dc}/2$	ON	OFF	Charging
0	ON	ON	Idle
$-V_{dc}/2$	OFF	ON	Discharging

4) *Control Algorithm*: A simplified control algorithm for the FCMLI is as follows:

- Measure output voltage  $V_o$  and capacitor voltages  $V_{C_i}$ .
- Determine desired output level based on modulation reference.
- Select switch combinations that achieve desired  $V_o$  while minimizing capacitor voltage error:

$$\min \sum_i |V_{C_i} - V_{ref}| \quad (7)$$

- Unequal capacitor voltage balancing in higher levels.

5) *Advantages and Limitations*:

Advantages:

- Better voltage balancing compared to NPC.
- Increased redundancy allows fault-tolerant operation.
- Capable of generating more voltage levels with fewer sources.

**Limitations:**

- Control is complex due to capacitor voltage balancing.
- Large number of capacitors for higher levels.
- High switching losses due to frequent balancing operations.

**Applications:**

- High-performance motor drives.
- Renewable energy interface systems.
- Aircraft electric propulsion and naval systems.

$$N_{FC} = \frac{(n-1)(n-2)}{2} \tag{8}$$

The requirement for dynamic voltage balancing and capacitor pre-charging adds to the complexity of the control [4]. Due to their cost and space requirements, FC inverters are less feasible for systems that need multiple levels, despite their superior dynamic performance.

**C. Cascaded H-Bridge (CHB) Multilevel Inverter**

The modular and scalable Cascaded H-Bridge Multilevel Inverter (CHB-MLI) topology consists of several H-bridge cells connected in series per phase. Typically, each H-bridge cell is powered by a different DC source. The CHB topology is perfect for renewable energy integration and electric vehicle (EV) propulsion systems due to its high modularity, fault tolerance, and simplicity of implementation. [16], [17].

1) *Structure and Operation Principle:* Each phase leg of an  $m$ -level CHB inverter is composed of  $s = \frac{m-1}{2}$  H-bridge cells, with each cell generating three voltage levels:  $+V_{dc}$ ,  $0$ , and  $-V_{dc}$ .

The output voltage per phase is the sum of voltages produced by each H-bridge cell:

$$V_o(t) = \sum_{i=1}^s v_i(t) \tag{9}$$

where  $v_i(t)$  is the output voltage of the  $i$ -th H-bridge cell. Each H-bridge output voltage  $v_i$  can be:

$$v_i \in \{-V_{dc}, 0, +V_{dc}\} \tag{10}$$

2) *Total Output Levels:* For  $s$  H-bridges per phase, the total number of voltage levels  $m$  is given by:

$$m = 2s + 1 \tag{11}$$

For example, using 3 H-bridges per phase, a 7-level output ( $\{-3V_{dc}, -2V_{dc}, \dots, +3V_{dc}\}$ ) is obtained.

3) *Logic Algorithm for Modulation:* The CHB inverter often uses Phase Shifted Pulse Width Modulation (PS-PWM) or Selective Harmonic Elimination (SHE-PWM) to reduce harmonic distortion. A general algorithm for PS-PWM is:

- Define carrier signals for each H-bridge with equal amplitude and frequency but with phase shifts of:

$$\theta_i = \frac{(i-1) \cdot 180^\circ}{s}, \quad i = 1, 2, \dots, s \tag{12}$$

- Compare each carrier with the same sinusoidal reference signal.
- Generate gate signals for each H-bridge accordingly.
- Sum the outputs to construct a staircase voltage waveform.

*Selective Harmonic Elimination (SHE-PWM):* SHE-PWM calculates switching angles  $\theta_1, \theta_2, \dots, \theta_s$  that eliminate selected harmonics using the Fourier equation of the output voltage:

$$V_o(\omega t) = \sum_{n=1,3,5,\dots}^{\infty} \frac{4V_{dc}}{n\pi} \cos(n\theta_i) \sin(n\omega t) \quad (13)$$

where the goal is to eliminate specific harmonics (e.g., 5th, 7th) by solving a system of transcendental equations for  $\theta$ .

4) *Advantages:*

- High modularity—each H-bridge is identical and independent.
- Scalability to high voltage levels.
- Lower harmonic distortion with proper modulation.
- No need for clamping diodes or flying capacitors.
- Fault-tolerant capability.

5) *Limitations:*

- Requires isolated DC sources for each H-bridge.
- Increased complexity in balancing power among DC sources.
- Higher cost due to separate DC supplies.

6) *Applications:*

- Photovoltaic (PV) systems.
- Battery energy storage systems.
- Medium-voltage motor drives.
- Electric vehicles (EVs) and hybrid EVs.

D. *Hybrid Topologies*

Modern converter systems also explore hybrid topologies by combining the features of different inverters to improve performance. For instance, CHB led to the development of Modular Multilevel Converters (MMC), which offer improved energy balancing and modularity and are suitable for HVDC systems [7].

E. *Comparative Analysis*

Table I provides a comprehensive comparison of the major multilevel inverter topologies in terms of component requirement, voltage balancing, and application suitability.

**III. COMPARATIVE TOPOLOGY ANALYSIS**

The particular application, required output quality, complexity, and cost all influence the choice of MLI topology. While NPC is preferred in industrial motor drives because of its simplicity and resilience, CHB is appropriate for application with multiple independent DC sources (such as PV arrays). In situations where redundancy and dynamic response are crucial, flying capacitor inverters are employed.

**IV. SIMULATION IN MATLAB/SIMULINK**

A powerful platform for planning, simulating, and evaluating multi-level inverters with various PWM techniques is offered by MATLAB/Simulink. This study used both traditional Sinusoidal PWM (SPWM) and sophisticated Space Vector PWM (SVPWM) techniques to simulate three-level NPC and CHB inverters.

A. *Simulation Parameters*

The parameters used in all simulations are listed in Table II

A resistive-inductive (R-L) load was connected at the inverter output to reflect typical industrial conditions.

TABLE I  
COMPARATIVE ANALYSIS OF MULTI-LEVEL INVERTER TOPOLOGIES

Characteristic	Neutral Point Clamped (NPC)	Flying Capacitor (FC)	Cascaded H-Bridge (CHB)	Modular Multilevel Converter (MMC)
Number of DC Sources	Single	Single	Multiple (isolated)	Multiple (distributed)
Switches per Phase	$2(n-1)$	$2(n-1)$	$4s$	$2n$
Voltage Balancing Mechanism	Neutral point clamping	Flying capacitors	Self-balancing	Arm-level control
Component Count	Moderate	High (due to capacitors)	High (modular H-bridges)	Very High
Control Complexity	Moderate	High	Moderate	Very High
Modularity	Low	Medium	High	Very High
Common Applications	Industrial drives, UPS	Motor drives, EVs	Renewable energy, EVs, storage systems	HVDC transmission, smart grids

TABLE II  
SIMULATION PARAMETERS

Parameter	Value
DC Link Voltage ( $V_{dc}$ )	600V
Switching Frequency ( $f_s$ )	10kHz
Fundamental Frequency ( $f_o$ )	50Hz
Load Resistance ( $R$ )	$10\Omega$
Load Inductance ( $L$ )	20mH
Number of Levels	3
Modulation Index (MI)	0.9

B. Simulink Model Overview

Simulink’s Power Electronics toolbox was used to model the inverter circuit. An IGBT block managed by gating pulses from the PWM generator subsystem was used to implement each switch. A sector identification and switching table method based on reference vectors was applied to SVPWM.

Figure 1 shows the developed three-level NPC inverter model with SVPWM logic.

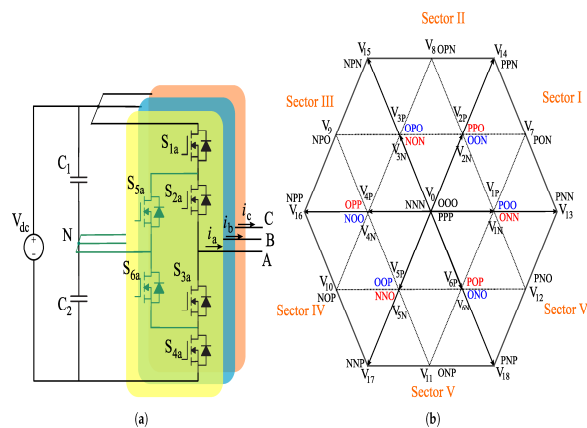


Fig. 1. Simulink model of 3-level NPC inverter using SVPWM

C. Output Voltage Waveform

Figure 2 illustrates the phase voltage waveform of the three-level inverter using SPWM and SVPWM techniques. SVPWM provides a more sinusoidal waveform with fewer switching transitions, improving harmonic performance.

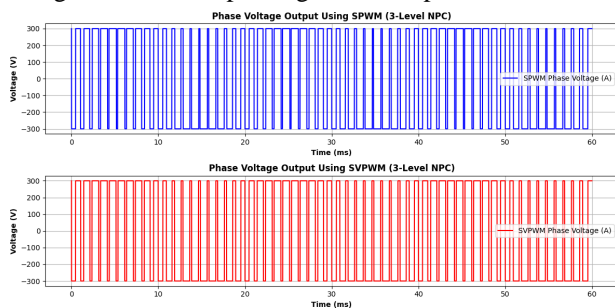


Fig.2. Phase voltage output for SPWM and SVPWM (NPC)

D. Total Harmonic Distortion (THD) Analysis

The THD was calculated using the Fast Fourier Transform (FFT) tool in MATLAB. SVPWM consistently outperformed SPWM in terms of harmonic reduction.

TABLE III  
THD COMPARISON OF PWM TECHNIQUES

PWM Technique	NPC Inverter (%)	CHB Inverter (%)
Sinusoidal PWM (SPWM)	10.25	8.37
Space Vector PWM (SVPWM)	5.62	4.25

Figure 3 shows the harmonic spectrum for SVPWM output.

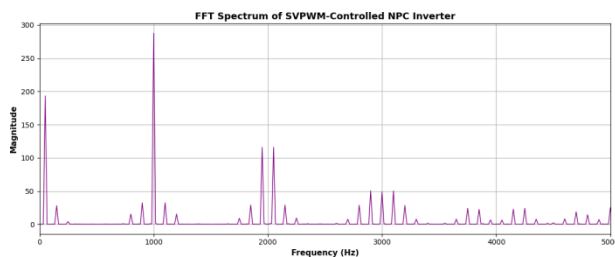


Fig.3. FFT spectrum for SVPWM-controlled NPC inverter

E. Discussion

The simulation results demonstrate that the SVPWM technique has several advantages over SPWM, such as lower THD and better voltage utilization. Furthermore, CHB inverters naturally produce lower THD than NPC due to their modular design and higher number of voltage steps. The results also demonstrate how important it is to select the optimal inverter topology and modulation method to optimize power quality and efficiency.

V. CONCLUSION

In this study, NPC and CHB multi-level inverters were modeled and simulated using MATLAB/Simulink’s SPWM and SVPWM techniques. Comparative analysis shows that SVPWM offers better voltage utilization, lower THD, and high voltage quality. The CHB topology demonstrated better harmonic performance due to its modular design, especially when SVPWM was used for control. Future research will focus on enhancing inverter performance in applications such as electric drives and smart grids by fusing experimental validation with advanced control schemes like MPC and AI-based modulation.

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