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Offline UPS for Regenerative Loads

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Abstract: ***This paper presents describes about a unique DC Discharge System for Offline UPS. Whenever an offline mode UPS is connected to a motor load, as the motor decelerates either through the change of torque or due to the Dynamic braking there will be a regenerative energy produced. If this regenerative energy flows back into the UPS, then over-voltage condition takes place and causes damage to the UPS. This regenerative energy can bypass through the battery in online mode. But online mode operation of UPS needs high cost as large heat sinks are required. So, offline mode of operation is preferred in most of the cases. The proposed system dissipates the regenerative energy through the connected resistors and the remaining energy is used for the gating of semiconductor switches inside the UPS. The detailed principle of the proposed method is discussed in this project. The entire Discharge System and Gate pulse generating System are simulated in Proteus Software and the results are provided.***
Index Terms: Offline UPS, DC Discharge System, IGBT triggering.

I. INTRODUCTION

Today, the world runs on critical infrastructure and technology in Hospitals, Factories, Data centers, Vehicles and the Electrical grid. These are things people depend on every day. An uninterruptible power supply (UPS) is used to protect critical loads from utility- supplied power problems, including spikes, brownouts, fluctuations and power outages, all using a dedicated battery. For the above mentioned reasons, it is important to implement an UPS that has an potential to work under all the conditions. UPS Provides backup power when utility power fails, either long enough for critical Equipment to shut down gracefully so that no data is lost or long enough to keep required loads operational until a generator installed online.
Conditions incoming power so that all-too-common sags and surges don't damage sensitive electronic gear.

II. DC DISCHARGE KIT

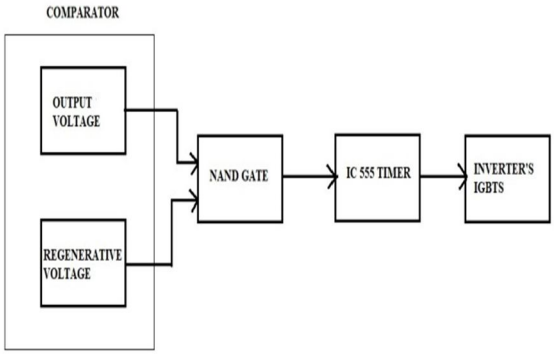


Fig 1., Block diagram of DC Discharging Kit

Block diagram of DC discharging kit consists of comparator which compares the output voltage from the inverter and the regenerative voltage that has been comes from the connected regenerative loads like motor, The NAND gate or "NOT AND" gate is the combination of two basic logic gates, the AND gate and the NOT gate connected in series. The NAND gate and NOR gate can be called the universal gates since the combination of these gates can be used to accomplish any of the basic operations. The function of timer includes As you can see the 555 IC is wired in Monostable mode of operation. Please read the article Monostable Multivibrator using 555 Timer for more details. In this mode the output is LOW (0V) when there is no triggering, when it is triggered via 2nd pin the output goes HIGH (Vcc) for some time. This time period is determined by the expression T=1. 11 RC (R=R2; C=C2 in the diagram). Trigger is applied via a differentiator circuit to make sharp pulses.

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The resistor of differentiator is connectedto Vcc to generate negative trigger pulses and the diode avoids positive spikes. And now this output is modulated using the input voltage applied at the control pin of the IC. So, whenever the Trigger pin pulses become low the output of the IC switchesto high and as a result the discharge transistor (internal to the 555 IC attached to the 7th pin) is disabled. So C2 charges through R2. This capacitor keeps on charging until the voltage is above the input control voltage, at which the IC changes its state. Now the output is low which makes the discharge transistor activated thereby discharging the capacitor C2. Hence the output pulse width is determined by the control voltage. This process continues, and we get a continuous stream of pulses which can be usedfor motor control, driving LED's, transmitting servo signals for remote control applications etc. An insulated gate bipolar transistor (IGBT) is a device in which a IGBT is combined with a bipolar transistor. The utility model has the advantages that the power IGBT is easy to drive, the control is simple, the switching frequency is high, and the power transistor has low on-voltage, large on-state current and small loss. According to Toshiba, the on-resistance of the 1200V/100A IGBT is 1/10 of the power IGBT of the same withstand voltage specification, and the switching time is 1/10 of the GTR of the same specification. Due to these advantages, IGBTs are widely used in the design of uninterruptible power systems (UPS). This online UPS using IGBT has the significant advantages of high efficiency, high impact resistance and high reliability.

III. SIMULATION OUTPUT

1) Circuit 1: +VDC

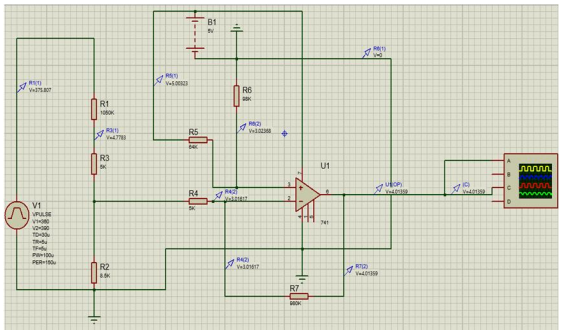


Fig 2., Simulation Diagram of +VDC

+VDC Comparator circuit is designed by using Operational amplifier to compare. The voltages in both control circuit and main circuit. It compares the voltage range of 320V to 400v. When the voltage range exceeds 365V in control circuit then we have to consider +VDC circuit. Comparator triggers the output to the NAND gate. Similarly, when the voltage range exceeds 380V. When regenerative load condition then the main circuit triggers the output to the other NAND gate. This generally compares the output voltage which will be in the positive half cycle. This can be used in both the control circuit and the main circuit. The main objective of designing this circuit is to compare the two voltage ranges from the output and the regenerative load.

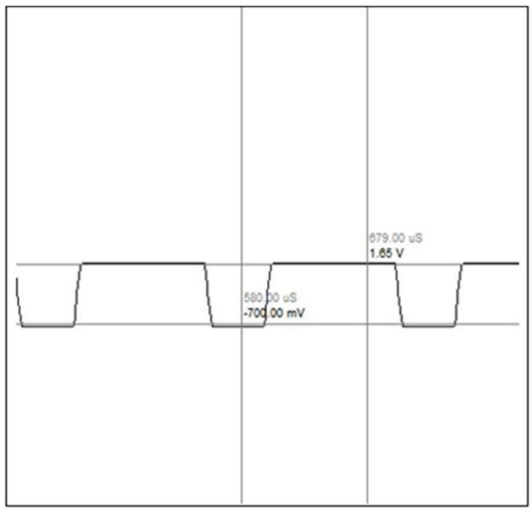


Fig 3., Simulation output of +VDC

Peak to Peak voltage: 4 V
Time period: 480 microseconds
Inference: From this we have inferred that the output voltage of +VDC with amplifier is around 3.5 to 4V. This could be the high input to the NAND gate.The above figure displays the output of the +vdc simulated diagram which feds the input of + 35.805V and results in the output of about 4.01359V due to the resistance and inverting amplifier connected through it.

2) Circuit 2: -VDC

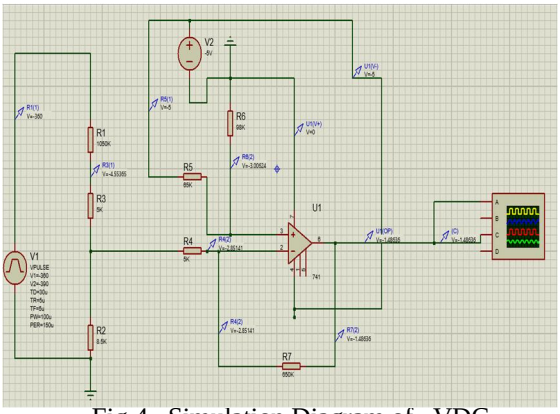


Fig 4., Simulation Diagram of –VDC

- VDC Comparator circuit is designed by using similar components of +VDC circuit and the voltage ranges remains the same as +VDC circuit for both control and main circuit. The control circuit and main circuit triggers the output to NAND gate at the voltage range of -365 and the voltage ranges remains the same as +VDC circuit for both control and main circuit.
But in terms of negative voltage range to -380V. In -VDC circuit the input voltage is given from 320V to 400V in the inverting terminal of operational amplifier and the reference voltage (Vref) is given at the non-inverting terminal by using the voltage divider network.

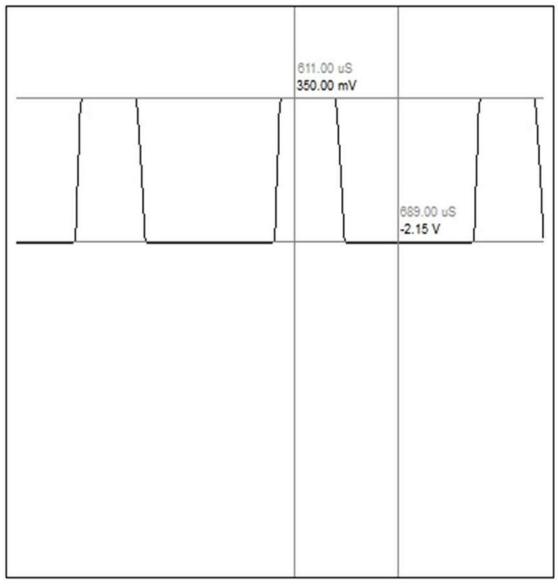


Fig 5., Simulation output of –VDC

Peak to Peak voltage: -3.5V
Time period: 610 microseconds
Inference: From this we have inferred that the output voltage of –VDC with amplifier is around -3 to -3.5.So this has to be amplified with an amplifier. The above figure displays the output of the -vdc simulated diagram which feds the input of -360V and results in the output of about -1.486V due to the resistance and inverting amplifier connected through it.

3) Circuit 3: -VDC with Amplifier

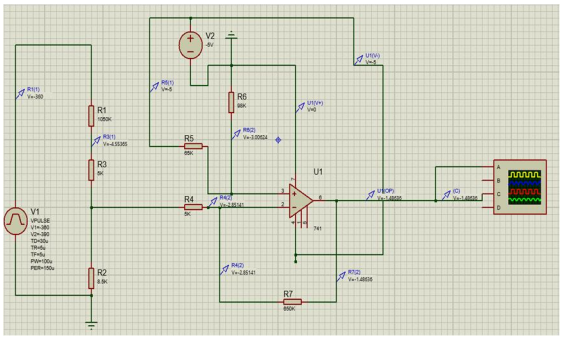


Fig 6., Simulation Diagram of -VDC with amplifier

VDC Amplifier circuit is used in both control and main circuits. This amplifier circuit amplifies the output from the -VDC comparator circuit and sends the amplified output voltage to the NAND gate input terminal. During the amplification process it produces an 180^0 phase shift in the output. Thus, the negative voltage will be changed topositive voltage in the output of amplifier circuit. Then now the positive voltage ranges from -VDC amplifier circuit and +VDC circuit is given to the NAND gate of both control and main circuits and then the NAND gates output is given to the AND gate. The AND gate compares the output from both the NAND gates and when both outputs are high then the AND gate triggers the output to the 555 PWM circuit.

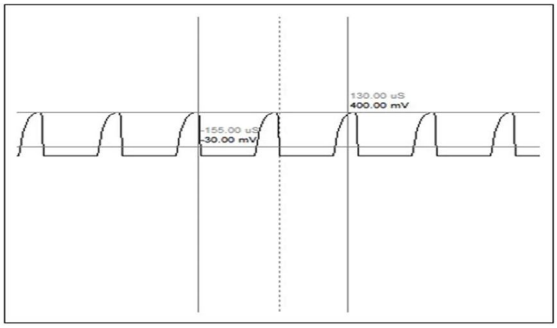


Fig 7., Simulation output of -VDC with Amplifier

Peak to Peak voltage: 4.8 V
Time period: 130 microseconds
Inference: From this we have inferred that the output voltage of –VDC with amplifier is around 4 to 4.85V. This could be the high input to the NAND gate. The above figure displays the output of the -vdc with amplifier simulated diagram which feds the input of -360V and results in the output of about 4.9836 V due to the resistance and non-inverting amplifier connected through it.

4) Circuit 4: Main Circuit

Main circuit diagram is constructed using above the cases used in +VDC, -VDC an –VDC With amplifier in additional to this NAND Gate and IC 555 Timer circuit is added.

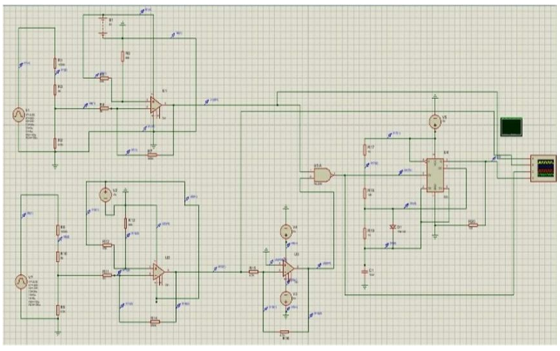


Fig 8., Simulation Diagram of Main circuit

The compared output from the +VDC and -VDC are given into a NAND gate which will get an input of 4.5V on each. So, the entire output of the NAND gate is 0V. This can be given to the IC 555 Timer and the generated output is displayed.

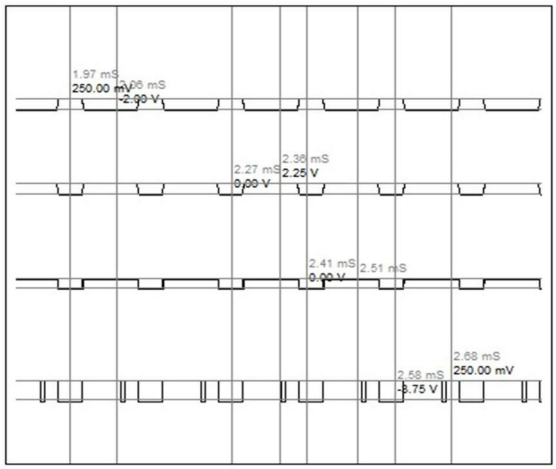


Fig 9., Simulation output of main circuit

Peak to Peak voltage: 0.8 V
Time period: 80 microseconds
Inference: From this we have inferred that the output voltage of the main circuit is 0V.This is generally considered as low input for the logic gates. So, we have to include another main circuit to get a high output. The above figure displays the output of the main circuit simulated diagram which feds the input of 0 and -360V and results in the output of about 2.28V due to the resistance and non-inverting amplifier, NAND gate and 555 timer connected through it.

5) Circuit 5: Final Circuit

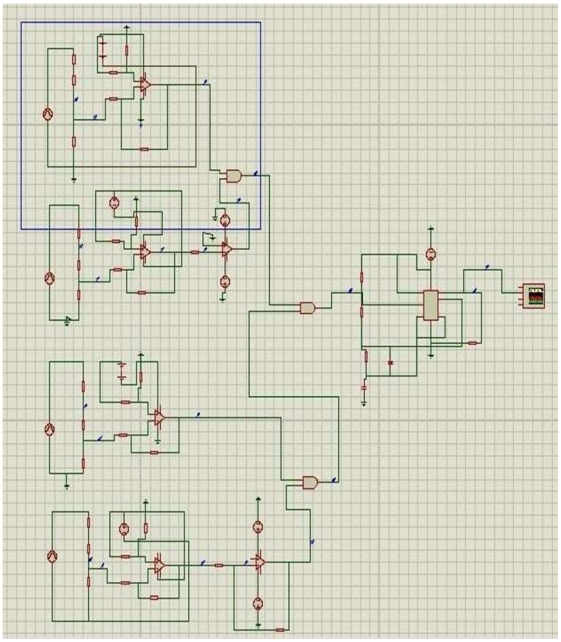


Fig 10., Simulation Diagram of Final circuit

The 555 Timer is configured in Astable Multivibrator mode of operation to produce the PWM signal as output which triggers the gate circuit in the output side. 5V supply is given to the VCC pin of 555 Timer IC. The duty cycle is obtained upto 90% and the ON Time and OFF Time is varied by varying the values of Resistors and Capacitor in the circuit. The output from singe main circuit is not sufficient to trigger an IGBT. So an another control circuit is added and connected through NAND Gate which will provide an output of 4.4V. This is the threshold voltage for IGBTs inside the inverter.

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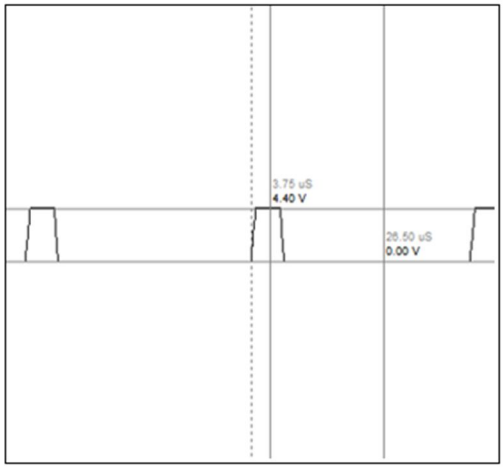


Fig 10., Simulation output of Final circuit

Peak to Peak voltage: 4.4 V
Time period: 3.75 microseconds
Inference: From this we have inferred that the output voltage of the final circuit would be around 4-4.40V.This voltage range is the threshold voltage of any IGBTs gate circuits. So from this the IGBT in the inverter can be triggered.

IV. RESULT AND DISCUSSION

Thus, we have designed the circuit required for DC Discharge kit in order to overcome the damages caused due to the regenerative loads connected to an offline mode or also referred as battery mode. The discharge kit dissipates the regenerative energy through a series of resistance as heat. The remaining undissipated energy is used to generate gate pulse for the semiconductor switches in the inverter of the UPS. Looking to the future, the study accomplished up to date ensures reduced voltage in the software basis. We are going to conduct various studies on offline UPS for regenerative loads in future for the betterment of this project.

Sl. No	Circuit	Output Voltage	Time period
1	+VDC	4V	480 ms
2	-VDC	-3.5V	610 ms
3	-VDC with amplifier	4.8V	130 ms
4	Main circuit	0.8V	80 ms
5	Final Circuit	4.4 V	3.5 µs

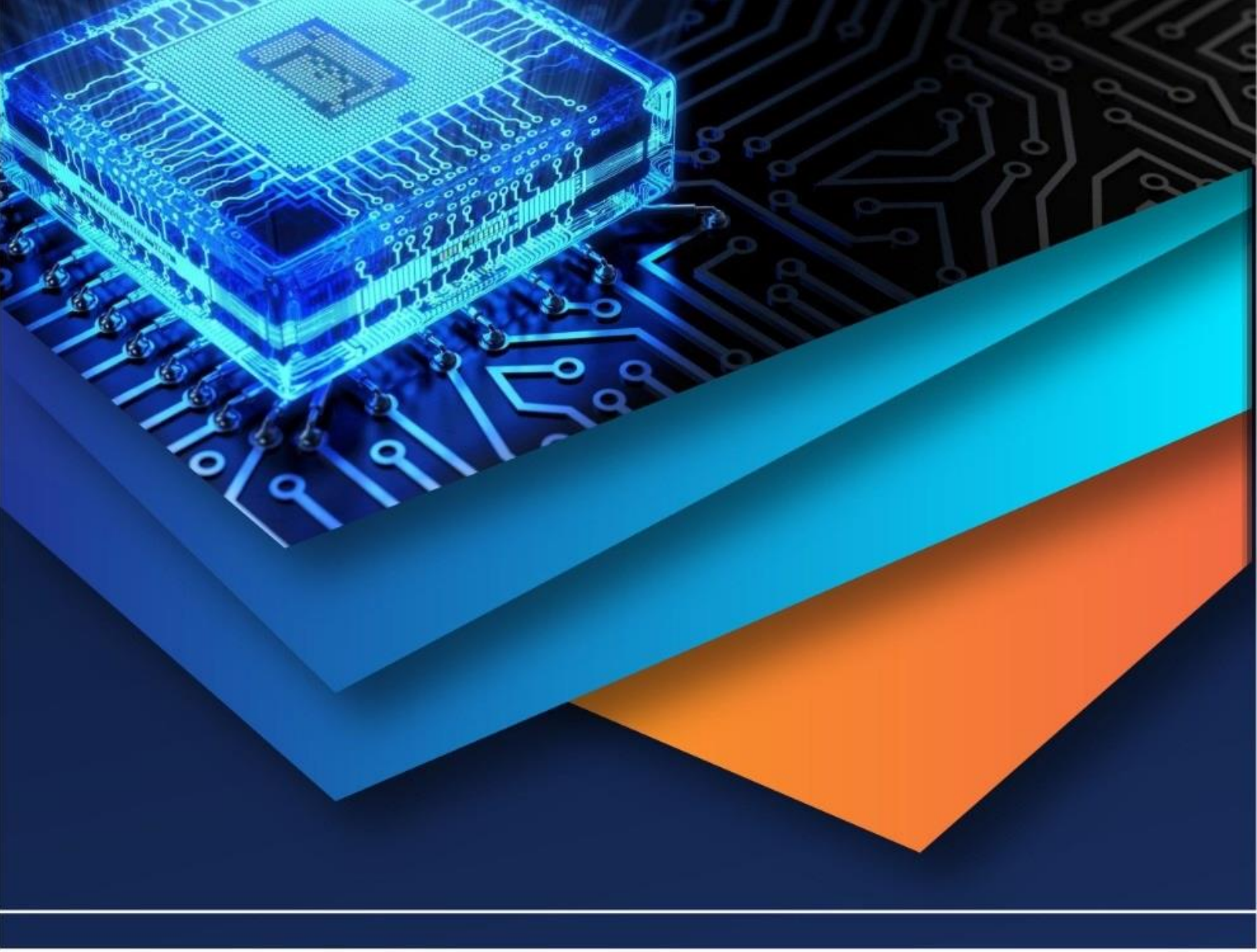
The +VDC, -VDC, -VDC with amplifier, main and final circuit has been simulated in the Proteus software and the results are provided. The ultimate output voltage is around 4.4V. This is the required threshold voltage for the IGBT to get triggered in the inverter circuit of the UPS.

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