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Onboard Charger for Plug-In Electric Vehicles

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Abstract: A compact and high-performance onboard charging system for plug-in electric vehicles is introduced, integrating advanced power conversion stages for improved efficiency and power quality. The proposed architecture employs a bridgeless interleaved boost Power Factor Correction (PFC) converter for the AC–DC interface and a Phase-Shifted Full-Bridge (PSFB) converter for isolated DC–DC power conversion. Through the adoption of Zero Voltage Switching (ZVS), the system effectively suppresses switching losses while simultaneously reducing conduction losses and harmonic distortion, thereby achieving enhanced power factor and conversion efficiency. A laboratory-scale hardware prototype is developed to experimentally validate the proposed design. The obtained results confirm stable output voltage regulation, high operational efficiency, and dependable battery charging characteristics, demonstrating the suitability of the proposed onboard charger for next-generation electric vehicle applications.
Index Terms: Onboard Charger, Electric Vehicle, Bridgeless Interleaved Boost Converter, Power Factor Correction, Phase-Shifted Full-Bridge Converter, Zero Voltage Switching, Battery Management System.

I. INTRODUCTION

The rapid adoption of electric vehicles (EVs) as sustainable alternatives to conventional fuel-based transportation has created a growing demand for efficient, reliable, and flexible charging solutions. This need is particularly critical for smaller EVs such as autorickshaws and e-scooters, which are widely used in urban environments but often lack compatibility with public EV charging stations. As a result, these vehicles are typically restricted to home charging or specific dedicated charging points, limiting charging flexibility, user convenience, and long-distance usability. This limitation primarily arises from the absence of onboard charging capability, forcing reliance on offboard chargers or specialized adapters, which reduces the overall practicality of such EVs. The Onboard Charger (OBC) is therefore a vital component, responsible for converting grid-supplied alternating current (AC) into regulated direct current (DC) for battery charging, while ensuring charging reliability, user convenience, and compliance with grid standards. Conventional onboard charger architectures that use diode bridge rectifiers and DC–DC converters suffer from high conduction losses, poor power factor, and increased total harmonic distortion (THD), which degrade system efficiency and grid power quality. To address these challenges, this work proposes a two-stage onboard charger architecture in which the AC–DC stage employs a Bridgeless Interleaved Boost Power Factor Correction (PFC) converter to minimize losses and improve input current quality, while the DC–DC stage uses a Phase-Shifted Full-Bridge (PSFB) converter to provide galvanic isolation and achieve Zero Voltage Switching (ZVS), thereby reducing switching losses. The proposed system achieves high efficiency, near-unity power factor, improved power quality, and stable battery charging performance, making it well suited for modern electric vehicle applications and enabling compatibility of small EVs with public charging infrastructure.

II. METHODOLOGY

The proposed onboard charger (OBC) is designed using a simple two-stage power conversion structure to convert AC power from the grid into regulated DC power for charging the electric vehicle battery. The system consists of an AC–DC conversion stage followed by an isolated DC–DC conversion stage, ensuring efficient energy transfer and safe battery charging operation

In the first stage, the AC input supply is converted into DC using a Bridgeless Interleaved Boost Power Factor Correction (BLIL Boost PFC) converter. This stage performs both rectification and voltage boosting while improving the input power quality. The bridgeless structure reduces conduction losses by eliminating the conventional diode bridge, and the interleaved operation allows current sharing between converter phases. This results in reduced current ripple, improved efficiency, and better thermal performance. The control of the converter ensures that the input current follows the input voltage waveform, achieving improved power factor and stable DC-link voltage. The DC output from the PFC stage is then supplied to the second stage, which is an isolated DC–DC conversion stage implemented using a Phase-Shifted Full-Bridge (PSFB) converter. This stage steps down the DC-link voltage to a suitable level required for battery charging and provides galvanic isolation through a high-frequency transformer. Power flow is controlled using phase-shift modulation between the bridge switches, enabling smooth regulation of output voltage and current. The converter operates with soft-switching, which reduces switching losses and improves overall efficiency.

The overall operation of the onboard charger follows a simple and structured energy conversion process from AC input to regulated DC output through the two conversion stages. This methodology ensures efficient power conversion, improved power quality, electrical isolation, and reliable charging performance, making the proposed onboard charger suitable for plug-in electric vehicle applications.

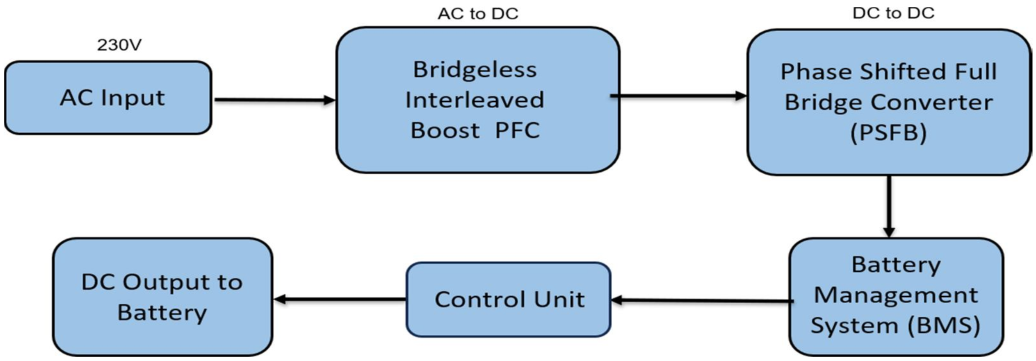

Fig.1 Block Diagram of Onboard Charger

III. STAGES OF ONBOARD CHARGER

A. Bridgeless Interleaved Boost PFC

The circuit diagram of the Bridgeless Interleaved Boost Power Factor Correction (PFC) converter represents the AC–DC conversion stage of the onboard charger. The converter operates without a traditional diode bridge rectifier, which reduces conduction losses and improves overall efficiency. It consists of two interleaved boost converter legs with switches Q1, Q2, Q3, and Q4 and inductors L1, L2, L3, and L4, each handling alternate half cycles of the AC input voltage. During the positive half-cycle, switches Q1 and Q2 with the corresponding inductors conduct and transfer energy to the DC-link capacitor through the diodes. During the negative half-cycle, switches Q3 and Q4 with their inductors operate in a similar manner, ensuring continuous energy transfer to the DC output. The interleaved configuration allows current sharing between the two paths, which reduces input current ripple, component stress, and thermal losses. The output of this stage is a unregulated DC voltage that is suitable for feeding the next conversion stage

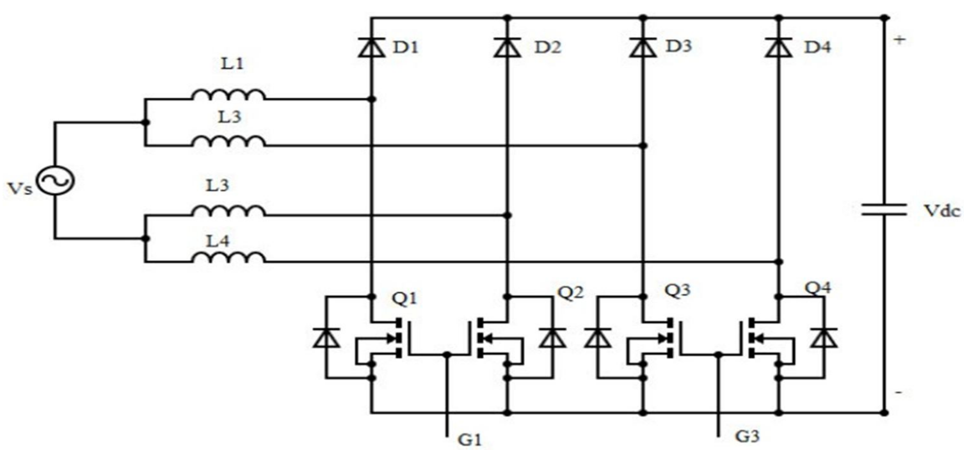

Fig.2. Circuit Diagram of Bridgeless Interleaved Boost PFC

B. Phase Shifted Full Bridge Converter

The circuit diagram of the Phase-Shifted Full-Bridge (PSFB) converter represents the isolated DC–DC conversion stage of the onboard charger. It consists of four power switches S1, S2, S3, and S4 arranged in a full-bridge configuration on the primary side of a high-frequency transformer. The DC-link voltage from the PFC stage is applied to the transformer through controlled switching of these bridge switches. By introducing a phase shift between the bridge legs (S1–S2 and S3–S4), the power transferred to the secondary side is regulated. The high-frequency transformer provides electrical isolation and voltage step-down. On the secondary side, the transformer output is rectified using diodes D5–D8 and filtered using an LC filter to obtain smooth DC output. This stage provides regulated and isolated DC power suitable for battery charging

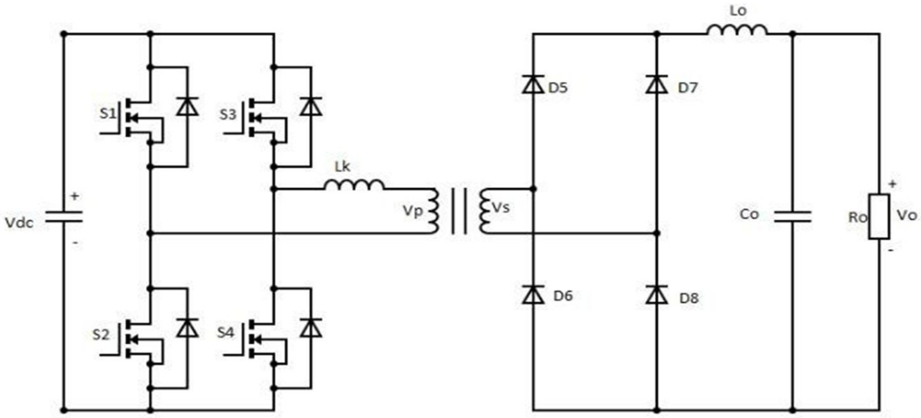

Fig.3 Circuit Diagram of Phase Shifted Full Bridge Converter

IV. SIMULATION

A. Simulation Circuit of Bridgeless Interleaved Boost PFC Converter

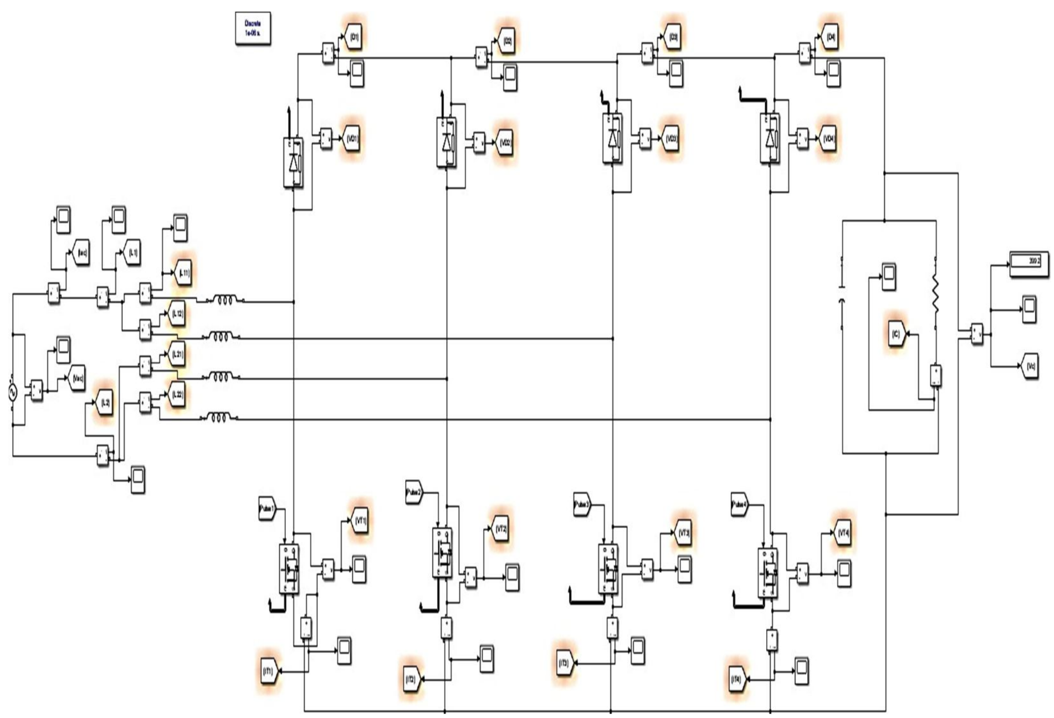

Fig.4 Simulation of Bridgeless Interleaved Boost PFC

The simulation model of the Bridgeless Interleaved Boost Power Factor Correction (PFC) converter represents the front-end AC–DC stage of the onboard charger. Its primary function is to convert the single-phase AC supply into a regulated high-voltage DC output while improving input power quality. The circuit includes an AC source, boost inductors, four MOSFET switches, and output diodes arranged in a bridgeless topology, which eliminates the conventional diode bridge and reduces conduction losses. Two interleaved boost channels operate 180° out of phase to share input current, minimize ripple, and reduce thermal stress on the switches. A DC-link capacitor maintains a stable boosted voltage for the next conversion stage. Closed-loop PWM control regulates the DC-link voltage under varying load conditions. The PFC control strategy ensures that the input current follows the supply voltage waveform, achieving near-unity power factor and low harmonic distortion.

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B. AC To DC Stage Parameters (BIBPFC)

Parameter	Value
Input Voltage	230 V rms
Output Voltage	400V
Switching Frequency	48 kHz
Inductor	400µH
Capacitor	780µF

Table.1 AC to DC Stage Parameters (BIBPFC)

The AC–DC stage of the onboard charger is designed to operate from a standard single-phase supply of 230 Vrms, which corresponds to the commonly available grid voltage in domestic and public charging environments. This input is processed using a bridgeless interleaved boost power factor correction (PFC) converter to generate a regulated DC output of approximately 400 V, forming a stable DC link for the subsequent DC–DC conversion stage. A switching frequency of 48 kHz is selected to maintain a suitable compromise between compact magnetic component size and acceptable switching losses. The boost inductors are designed with a value of 400 µH to ensure operation in continuous conduction mode, which reduces input current ripple and improves overall power factor performance. Additionally, a 780 µF DC-link capacitor is employed to smooth the boosted voltage and minimize output ripple, thereby maintaining stable DC conditions even under varying load requirements.

C. Result

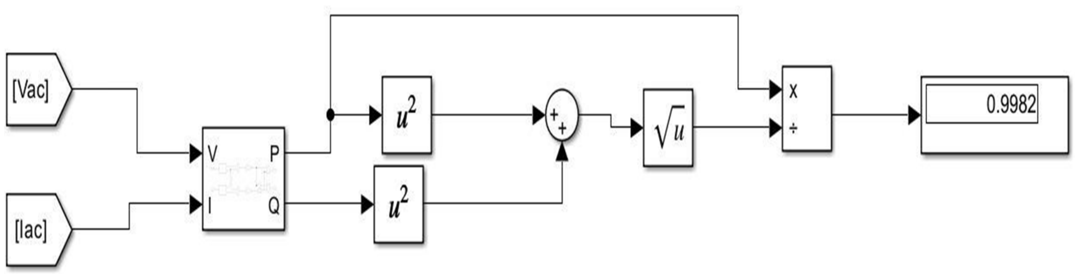

Fig.5 Simulation Result of Power Factor Measurement

This simulation block diagram represents the Power Factor (PF) calculation and verification of the PFC stage. The input voltage (Vac) and input current (Iac) are used to compute the real power (P) and reactive power (Q). These values are squared and summed, and the square root operation is applied to obtain the apparent power (S). The real power is then divided by the apparent power (P/S) to calculate the power factor. The output value of 0.9982 indicates that the input current is almost perfectly in phase with the input voltage, confirming near-unity power factor operation and effective performance of the PFC converter in the simulation

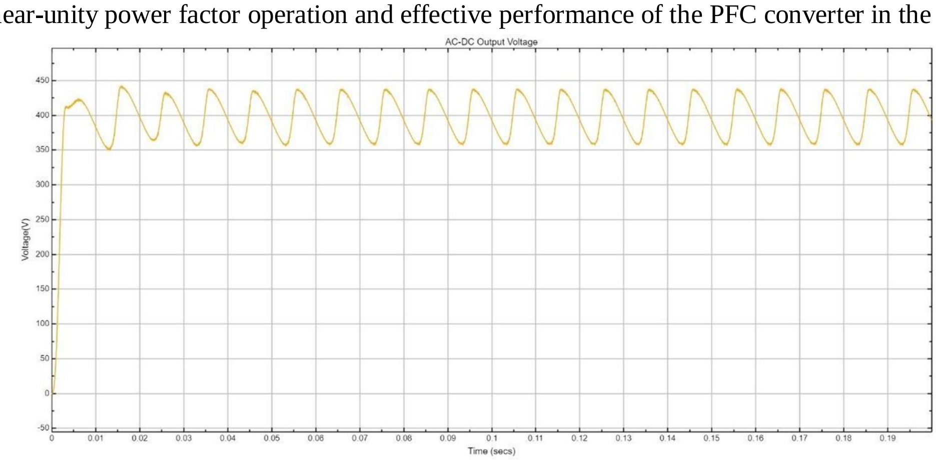

Fig.6 Output of Bridgeless Interleaved Boost PFC

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Fig. 6 shows the output voltage waveform of the Bridgeless Interleaved Boost PFC converter. The DC link voltage is obtained at 400 V under rated operating conditions. The waveform exhibits minimal ripple, indicating effective voltage control and stable operation of the PFC stage. The DC output confirms proper duty cycle control and successful AC–DC conversion.

D. Simulation Circuit of Phase-Shifted Full-Bridge (PSFB) Converter

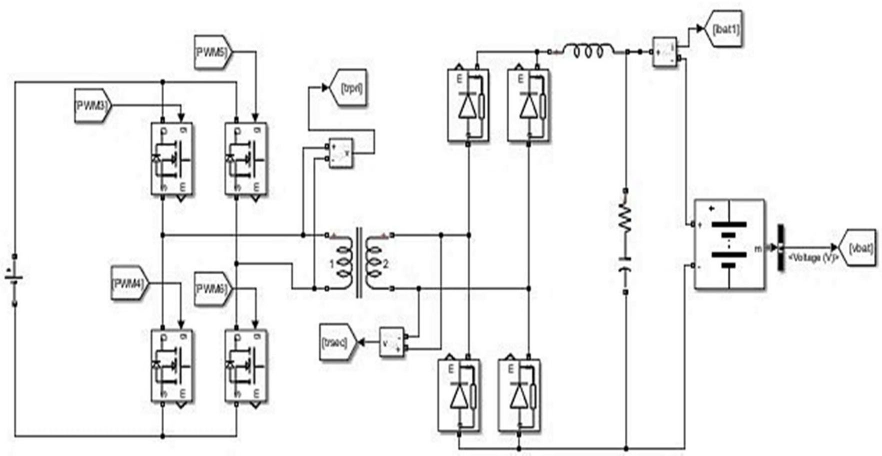

Fig.7 Simulation of Phase Shifted Full Bridge Converter

The Phase-Shifted Full-Bridge (PSFB) converter constitutes the isolated DC–DC conversion stage of the proposed onboard charger and plays a crucial role in regulating and delivering controlled power to the battery system. In the developed simulation model, four MOSFET switches are arranged in a full-bridge configuration on the primary side of a high-frequency transformer, and the regulated 400 V DC output obtained from the PFC stage is applied across this bridge network. Through controlled switching of the bridge devices, the DC input is converted into high-frequency alternating voltage. The output power is regulated by introducing a precise phase shift between the switching signals of the two bridge legs, which effectively controls the duration of energy transfer to the transformer. This phase-shift modulation technique enables smooth power control while facilitating Zero Voltage Switching (ZVS), thereby significantly reducing switching losses, lowering device stress, and improving overall converter efficiency. The high-frequency transformer provides galvanic isolation between the input and output sides while stepping down the voltage to the required battery charging level. On the secondary side, fast-recovery or Schottky diodes perform rectification, and an LC filter network minimizes ripple to produce a stable DC output. The simulation results confirm that the PSFB stage ensures efficient, isolated, and well-regulated DC power suitable for reliable and safe battery charging applications.

E. DC To DC Stage Parameters (PSFB)

Parameter	Value
Input Voltage	400V
Output Voltage	52V
Inductor	16µH
Capacitor	107µF
Turns ratio	70 : 400

Table.2 DC to DC Stage Parameters (PSFB)

The DC–DC conversion stage operates with an input voltage of approximately 400 V, which is derived from the regulated output of the AC–DC bridgeless interleaved PFC stage. This high-voltage DC link serves as the primary energy source for the Phase-Shifted Full-Bridge (PSFB) converter, where further voltage regulation and isolation are performed. The PSFB topology is selected to ensure efficient power transfer while maintaining electrical separation between the input and output sides.

The converter is designed to deliver a regulated output of around 52 V DC, which is appropriate for charging low-voltage electric vehicle battery packs used in small and medium EV applications. Voltage reduction is achieved using a high-frequency transformer with an approximate turn's ratio of 70:400, enabling effective step-down operation while also providing galvanic isolation for safety. The use of high-frequency operation allows the transformer size to be reduced compared to conventional low-frequency designs. This stage ensures controlled power delivery, improved efficiency, and stable DC output suitable for reliable battery charging.

F. Result

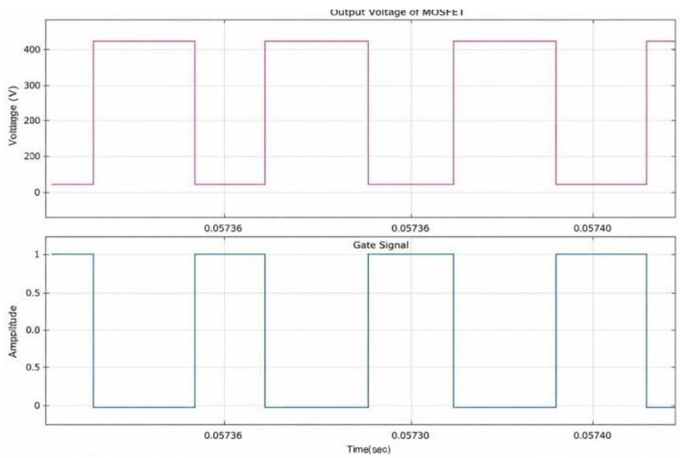

Fig.8 Simulation Result of Output Waveform Of ZVS

Fig.8 The waveform shows the MOSFET drain-to-source voltage (Vds) and gate signal (Vgs), where the drain voltage is observed to fall to nearly zero before the gate pulse turns ON, confirming that the device operates under Zero Voltage Switching (ZVS) conditions. This soft-switching behaviour significantly reduces turn-on switching losses, minimizes voltage stress on the device, and improves electromagnetic compatibility. As a result, overall switching losses are reduced, thermal stress on the MOSFET is lowered, and the converter achieves higher efficiency and improved reliability in high-frequency operation.

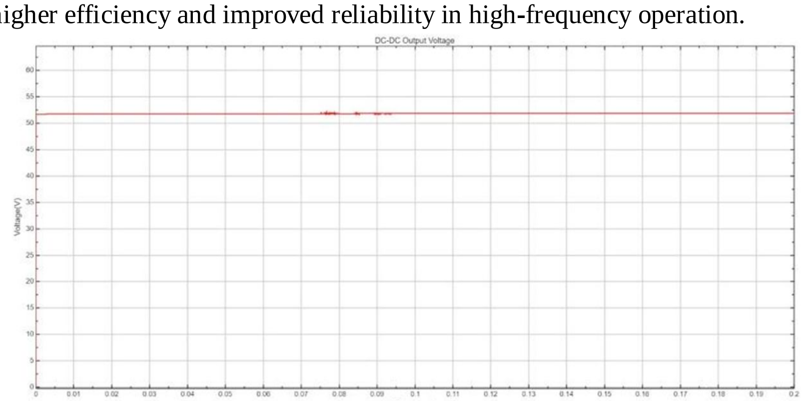

Fig.9 Output of DC-To-DC Output Voltage

Fig. 9 shows the simulated output voltage waveform obtained from the Phase-Shifted Full-Bridge (PSFB) converter. From the waveform, it can be observed that the converter successfully reduces the high-voltage DC link to nearly 52 V, which matches the required battery charging level. After the initial transient period, the output settles quickly and maintains a nearly constant value.
The voltage ripple is minimal, indicating that the rectifier and LC filter at the secondary side are properly designed. The smooth and regulated output also confirms that the phase-shift control strategy is effectively managing power transfer within the converter. The steady and stable waveform demonstrates that the DC–DC stage operates reliably under the given operating conditions and is suitable for controlled battery charging applications

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In the first stage of the onboard charger, the MOSFETs of the bridgeless interleaved boost converter are driven using the TLP250 opto-isolated gate driver. This driver receives PWM control signals from the Arduino UNO and provides the required gate drive voltage for proper switching of the IRF540N MOSFETs. The TLP250 offers electrical isolation between the low-power control circuit and the high-power converter stage, thereby protecting the microcontroller from voltage spikes and switching noise. It is capable of supplying sufficient gate current to ensure fast and efficient switching operation. Since the boost converter operates with respect to ground and does not require high-side floating drive, the TLP250 serves as a simple and reliable solution for the first stage of the system.

V. HARDWARE

A. Hardware Implementation

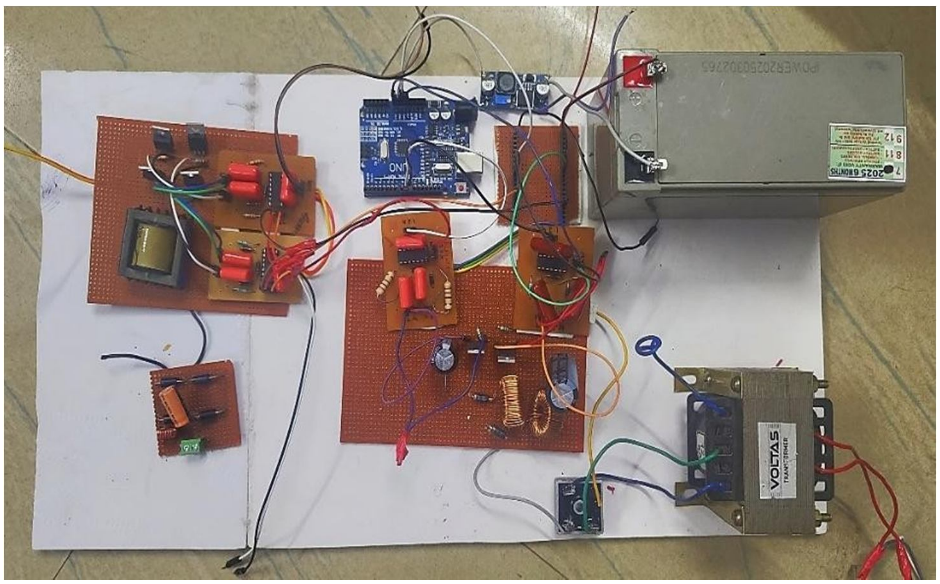

Fig.10 Hardware Setup

The hardware realization of the proposed onboard charger starts with a 230 V single-phase AC supply. Since the prototype is intended for laboratory-scale validation, the input voltage is deliberately reduced using a 230 V/6 V isolation transformer to ensure user safety and to minimize electrical stress on the power components. This reduced AC voltage is then converted into DC using a KBPC3510 bridge rectifier, and a 470 µF electrolytic capacitor is employed to smooth the rectified output and obtain a stable low-level DC supply for further processing. The obtained DC voltage is fed into a bridgeless interleaved boost converter comprising 1 mH ferrite-core inductors, IRF540N MOSFETs, and boost diodes, where the voltage is increased to a controlled level maintained below 48 V in the prototype. The switching of the boost MOSFETs is controlled using an IR2110 high-side and low-side gate driver IC. PWM signals generated by the Arduino UNO are supplied to the IR2110, which in turn delivers adequate gate voltage (approximately 10–12 V) and drive current for efficient switching. The driver’s bootstrap capability enables proper high-side operation, ensuring stable and reliable converter performance. The boosted DC is stored across 470 µF, 100 V DC-link capacitors, with a 0.1 µF film capacitor for high-frequency noise suppression and a 220 kΩ, 2 W bleeder resistor for safe capacitor discharge.
In the second stage, the boosted DC is applied to a Phase-Shifted Full-Bridge (PSFB) converter constructed using IRF540N MOSFETs. The same IR2110 driver is utilized to control the four bridge switches, as the topology requires independent high-side and low-side gate driving. The Arduino generates phase-shifted PWM pulses, which are amplified by the driver to enable high-frequency switching around 50 kHz. This switching action produces high-frequency AC at the transformer primary, where an ETD34 ferrite-core transformer with an approximate 3:1 turns ratio provides electrical isolation and voltage step-down. The secondary output is rectified using Schottky diodes and filtered through an LC network to produce a smooth DC output. The final regulated output voltage is obtained in the range of 13–14 V, confirming proper voltage step-down, stable regulation, and suitability for low-voltage battery charging under laboratory conditions.

B. Result

1) PWM Pulse

The observed waveform represents the Pulse Width Modulation (PWM) control signal generated by the controller for driving the power switching devices of the converter. The uniform high-frequency square pulses with controlled duty cycle indicate stable switching operation, where the pulse width directly regulates the effective voltage and power transferred through the converter stage. The presence of synchronized PWM signals reflects coordinated gate control required for proper converter operation, ensuring balanced switching, reduced device stress, and improved energy transfer. The clean rising and falling edges demonstrate low signal distortion and reliable gate drive performance, which is essential for minimizing switching losses and maintaining high system efficiency. Overall, the stable amplitude and consistent switching frequency confirm accurate PWM generation, enabling precise output regulation and dependable operation of the power conversion system.

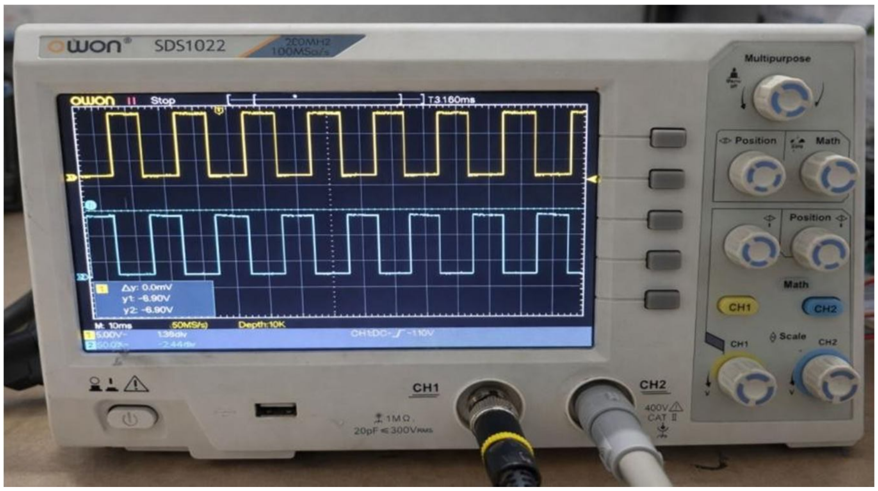

Fig.11 PWM Gate Driving Signals of MOSFET

2) Output DC Waveform

The final output voltage of the developed onboard charger was experimentally verified using a digital storage oscilloscope (DSO). The oscilloscope settings were adjusted to a vertical sensitivity of 10 V per division on Channel 1 and a time base of 100 µs per division, as indicated on the display. The captured waveform appears as a nearly straight horizontal trace, confirming that the output is a steady DC voltage rather than a fluctuating or ripple-dominant signal. From the vertical displacement of the waveform on the screen, the trace is positioned approximately 1.3 to 1.4 divisions above the reference level. Based on the selected scale (10 V/div), this corresponds to an output voltage of approximately 13–14 V DC. The absence of noticeable oscillations or switching ripple indicates that the rectification and filtering stages are functioning effectively, providing stable voltage regulation. The measured result confirms that the system successfully delivers a smooth and regulated low-voltage DC output in the intended 13–14 V range, making it suitable for low-voltage battery charging and laboratory-scale validation of the converter design.

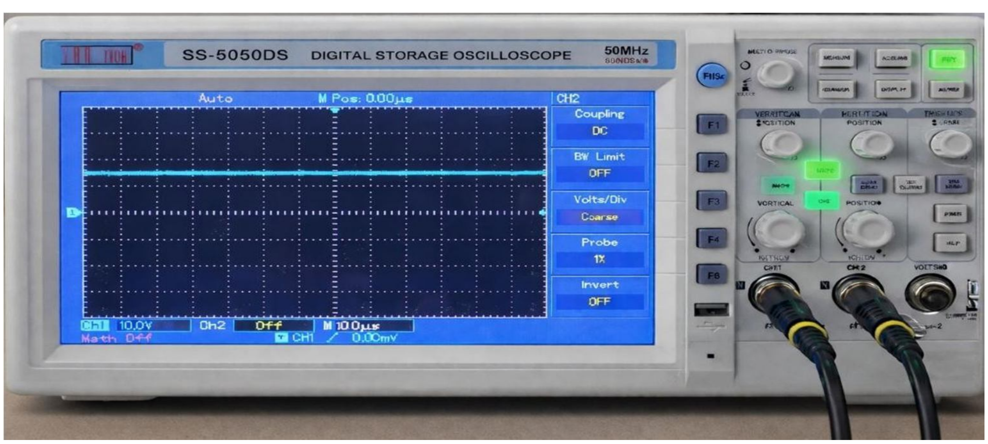

Fig.12 Output DC Waveform

The final output voltage of the developed onboard charger was experimentally verified using a digital storage oscilloscope (DSO). The oscilloscope settings were adjusted to a vertical sensitivity of 10 V per division on Channel 1 and a time base of 100 µs per division, as indicated on the display. The captured waveform appears as a nearly straight horizontal trace, confirming that the output is a steady DC voltage rather than a fluctuating or ripple-dominant signal. From the vertical displacement of the waveform on the screen, the trace is positioned approximately 1.3 to 1.4 divisions above the reference level. Based on the selected scale (10 V/div), this corresponds to an output voltage of approximately 13–14 V DC. The absence of noticeable oscillations or switching ripple indicates that the rectification and filtering stages are functioning effectively, providing stable voltage regulation. The measured result confirms that the system successfully delivers a smooth and regulated low-voltage DC output in the intended 13–14 V range, making it suitable for low-voltage battery charging and laboratory-scale validation of the converter design.

IV. CONCLUSION

The project focused on the design and simulation of a high-efficiency onboard charger intended for plug-in electric vehicle applications. The developed system combines a Bridgeless Interleaved Boost Power Factor Correction (PFC) stage with a Phase-Shifted Full-Bridge (PSFB) DC–DC converter to achieve improved input power quality, stable voltage regulation, and enhanced conversion efficiency. The AC–DC stage effectively improved the input power factor and reduced harmonic distortion, ensuring better interaction with the utility supply. The PSFB stage provided galvanic isolation and controlled voltage step-down using phase-shift modulation and Zero Voltage Switching (ZVS), which reduced switching losses and improved overall reliability. Both simulation and prototype evaluations demonstrated stable DC output, minimal ripple, and consistent battery charging behavior. The results indicate that advanced power converter topologies can be successfully implemented in compact onboard charging systems. With further refinement and scaling, the proposed design has strong potential for practical deployment in small and medium electric vehicles, supporting efficient and sustainable charging solutions.

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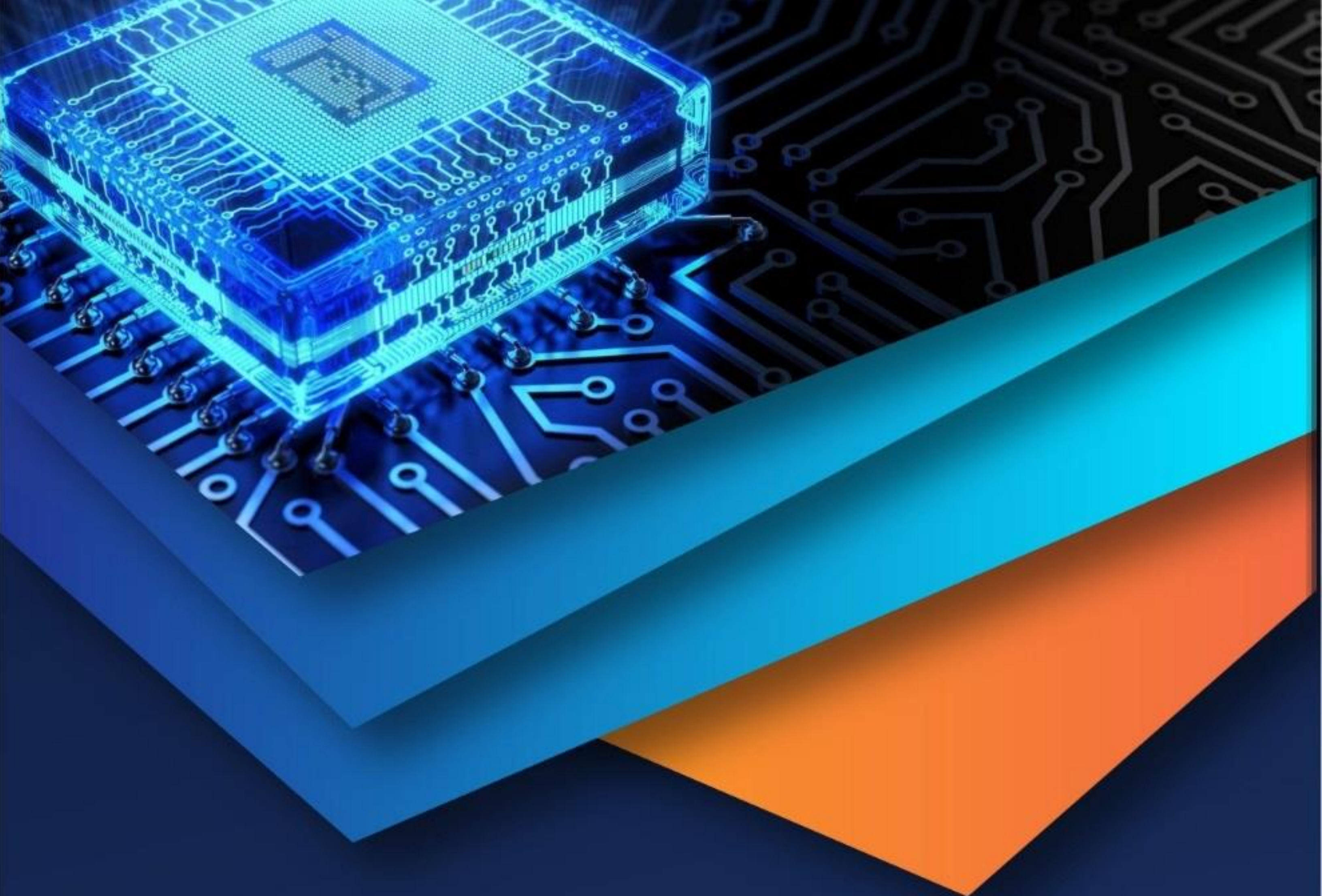

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