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Optimized Logic Gate Design using QCA

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Abstract: ***Quantum-dot cellular automaton (QCA) represents a burgeoning and auspicious nanoelectronic computational framework for the forthcoming generation, where binary data is encoded through the electronic charge arrangement within a cell. This architec- ture, rooted in digital logic, leverages individual electrons within arrays of quantum dots to execute binary operations. At the core of QCA circuits lies the QCA cell, serving as a fundamental unit for constructing basic gates and logic devices within QCA architectures. An assessment of diverse QCA-based XOR gate implementations is conducted in this study, alongside the proposition of novel layouts exhibiting enhanced performance metrics. The paper delves into various methodologies for designing QCA circuits, specifically focus- ing on the XOR gate. These layouts demonstrate a reduced number of crossovers and a diminished cell count in comparison to the conventional structures documented in existing literature. Notably, these design configurations hold significance for communication- centric circuit applications, particularly in activities such as phase detection within digital circuits, arithmetic computations, and error identification and rectification processes. A comparative analysis of different circuit designs is also provided, illustrating the potential of the proposed layouts in realizing more intricate circuits. The simulations in this study are executed utilizing the QCADesigner tool.***

I. INTRODUCTION

The scaling of technology to accommodate a greater number of devices has led to various constraints in the reduction of CMOS (Y. Taur, 2002; Shekhar Borkar, 1999). To address these issues, the emerging Nano device QCA was introduced by Lent (P. Douglas Tougaw & Craig S. Lent, 1994). QCA, with its Nano size, offers simplicity in implementation and shows promise as a technology for computing at the Nano scale. Despite the fact that all digital circuits currently utilize CMOS technology, QCA presents numerous advantages over CMOS and may potentially supplant it in the foreseeable future. QCA exhibits lower power dissipation due to the absence of current flow between cells, unlike CMOS where power dissipation occurs as current transfers between transistors. The reduction in cell size in CMOS leads to increased complexity in internal routing, yet the size of CMOS cannot be decreased due to various factors impacting its structural design. Conversely, in QCA, the size is straightforward, and routing can be achieved through wire propagation methods such as coplanar and multilayer crossovers. In contrast to CMOS, QCA integrates the transmission media and logic elements within the same block. While CMOS operates with only two clocking stages (high to low and low to high), QCA has developed a four-phase clocking system to eliminate coherence issues. CMOS draws power solely from an external supply, whereas QCA draws power from the clock signal itself. This study presents an optimized design of XOR and compares it with existing designs.

Various applications of XOR, such as Half Adder, Full Adder, Parity Generator, and Parity Checker, have been developed with reduced cell count, area, and delay compared to current designs. Quantum-dot Cellular Automata, commonly referred to as Quantum Cellular Automata (QCA), is implemented utilizing quadratic cells, hence known as QCA cells (K.Kim, K.Wu, R. Karri, 2005). Within QCA, the fundamental logic primitive gates are the majority gate and inverter, with the majority gate consisting of five QCA cells depicted in Figure 1 to generate an output of logic ’1’ based on a majority of logic ’1’ inputs, otherwise producing a logic ’0’.

The inverter, or NOT gate, can be designed in two distinct manners, illustrated in Figure 2. The AND and OR gates were developed by inducing polarization in one of the inputs within the majority gate, resulting in logic ’0’ and logic ’1’ respectively (Prameela Kumari N, K.S.Gurumurthy, 2014). The Quantum-dot Cellular Automata (QCA) system consists of four distinct phases during the clocking process (Rumi Zhang, KonradWalus, WeiWang, & Graham A. Jullien, 2004). These phases are switch, hold, release, and relax. During the switch phase, tunneling barriers begin to increase. Subsequently, in the hold phase, the tunneling reaches a high level to inhibit electron tunneling. In the release phase, the tunneling barriers gradually decrease, while in the relax phase, electrons resume tunneling activity.

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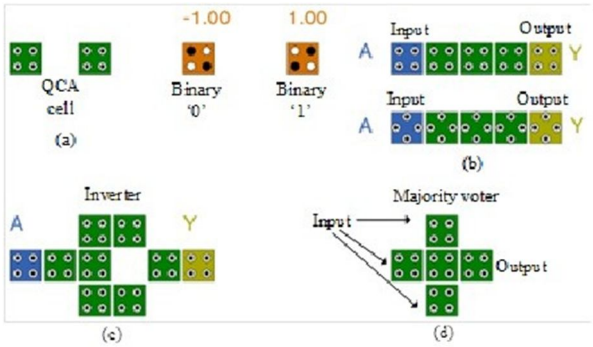

Fig. 1 QCA Basics (a) Cell (b) wire (c) Inverter (d) Majority gate

During the previous decade, multiple combinational circuits have been proposed and developed utilizing Quantum-dot Cel- lular Automata (QCA) as indicated by [2]. The principal component within combinational gates is the Exclusive OR (XOR) gate, which finds extensive utility in arithmetic circuits and digital communication systems. The XOR gate produces an output of logic '1' if the quantity of inputs is odd; otherwise, it yields a logic '0'. This fundamental operation of the XOR gate proves beneficial in numerous applications like Half Adders, Full Adders, Parity Generators, and Checkers[3][4][5][6]. While essential gates including AND, OR, NOT, along with universal gates such as NAND and NOR can be realized through a majority gate, the additional valuable gates XOR and XNOR cannot be directly derived, given their intricate fabrication process. Their im- plementation necessitates a combination of basic gates. Specifically, the XOR gate is constructed using the fundamental gates AND, OR, and an inverter. The prevailing design of the XOR gate adheres to traditional conventions. The initial implementation of XOR gate is based on a traditional design using [3]. The traditional designs of XOR gate initially employed numerous cells, areas, and crossovers. The XOR layout can be derived by applying various logic functions of fundamental gates and universal gates. The alternative methods for illustrating the fundamental logic function of XOR gate are provided below. The traditional configuration of the XOR gate, as outlined in [4], is constructed by employing majority gates. The XOR configuration exhibits a latency of 1 $^{1}_{4}$ clock cycle, occupies an area of 0.08μm^2, and consists of 51 cells. Subsequent Half Adder and Full Adder configurations utilize the aforementioned established design.

II. OPTIMIZED XOR GATE DESIGN

The XOR gate serves as the fundamental component in numerous digital circuits, including arithmetic circuits and parity bit generator circuits. Various XOR configurations have been introduced in the field of QCA technology with the objective of reducing the utilization of majority gates or inverters through the restructuring of the XOR equation. Some of these designs were developed based on the inherent capabilities of QCA. A traditional example of XOR architectures in QCA is depicted in Figure b, whereas the proposed XOR layout is shown in a separate figure. Here it is verified from the waveform that Y output is functioning properly for the given inputs A and B. Here the delay is 0.25 clock. Here from the above table it is verified that, total area is 0.02 μm^2 and it has 09 numbers of cells which is more optimized compared to above table.

III. CONCLUSION

The XOR gate serves as the fundamental component in numerous digital circuits, including arithmetic circuits and parity bit generator circuits. Within this manuscript, a novel single-layer Exclusive-OR gate design is put forth leveraging QCA technology. This innovative design showcases a 50% enhancement in speed and a 35% decrease in required cell count compared to the most

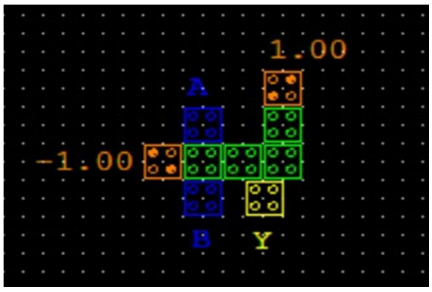

Fig. 2 XOR gate QCA layout

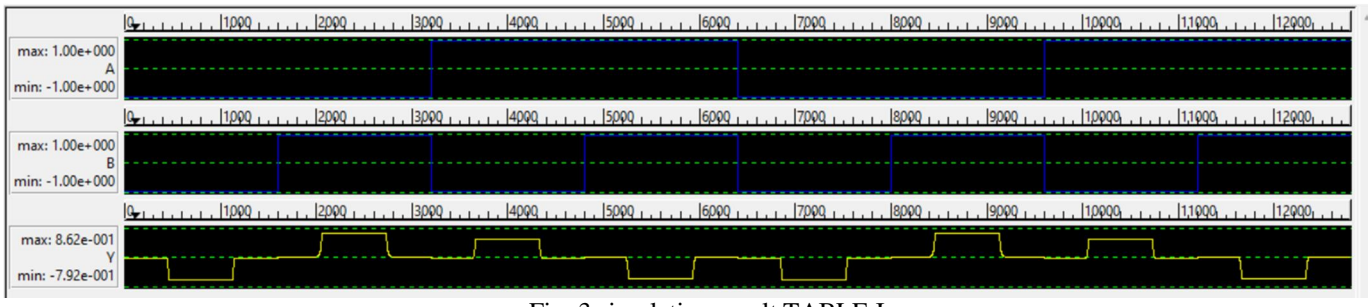

Fig. 3 simulation result TABLE I

COMPARISON WITH EXISTING DESIGNS

XOR	Area(μm2)	No. of Cells	Latency
[2]	0.22	121	1
[3]	0.07	64	1
[4]	0.06	49	1
[5]	0.09	60	1.5
[6]	0.08	54	1.5
[7]	0.03	29	0.75
[8]	0.02	28	0.75
[9]	0.02	14	0.5
Proposed	0.02	09	0.25

Optimal XOR configuration reported previously. The aforementioned gate is leveraged for the creation of more advanced half and full adders, resulting in a notable decrease in both circuit layout area and cell count.

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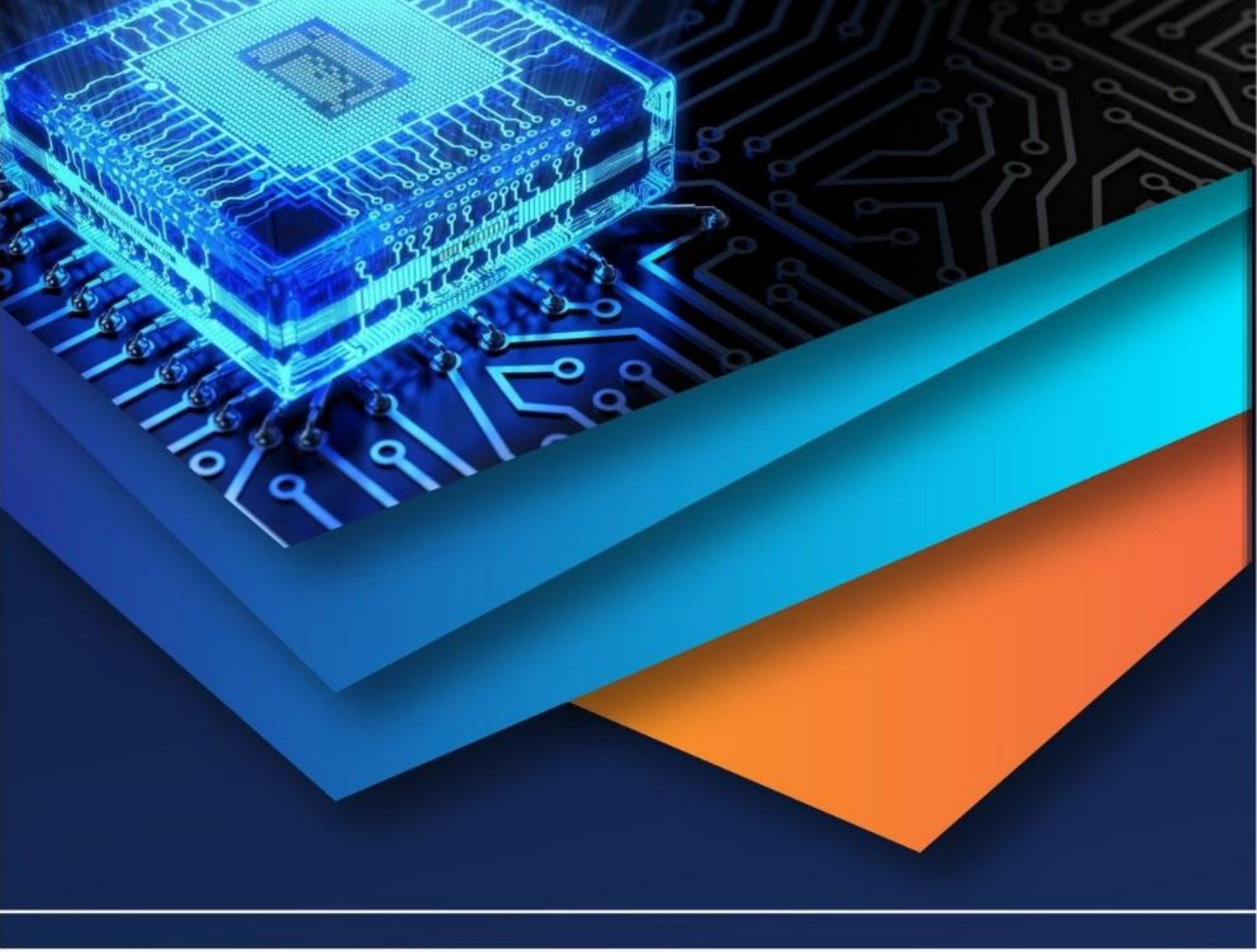

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