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Performance Analysis of Deep Sub Micron Two Quadrant Analog Divider Circuits

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Abstract: ***Current mode Analog Dividers are widely used in various circuits such as fuzzy logic controllers, neural networks, adaptive filters and variable gain amplifiers. When these current analog divider circuits implemented in DSM technology, many of the second order effects starts deteriorating its performance. Most of the available literatures on analog dividers are reporting performance of these circuits implemented using long channel MOSFETs. Hence it is a peak time to compare the performance variation between various proposed analog circuits implemented in lower technological nodes. This is for identifying most reliable circuit which safely works in this node. .In this work a comparative performance analysis of two quadrant CMOS analog divider against two quadrant CMOS approximation divider using 45nm technological node has been carried out. The obtained result indicates that Approximation Divider is reliabie than two quadrant CMOS analog divider. The entire work is carried out using Tanner software.***

Keywords: DSM Technology, Short channel effects, Analog Divider circuits, Two quadrant CMOS analog divider. Two quadrant CMOS approximation divider.

I. INTRODUCTION

Analog signal processing find applications in portable equipments, wireless nano sensors or medical implantation devices because of their compact implemented structure due to low power consumption and speed [2]. Analog Dividers are widely used in current mode analog circuits such as fuzzy logic controllers , neural networks, adaptive filters and variable gain amplifiers [3]. Most of the available analog divider circuits implemented using long channel MOSFETs [4-6]. When current divider circuits uses DSM technology ,many of the second order effects deteriorating performance. The reduction of the channel length of the transistor is the most common features of the modern CMOS technology. With the introduction of DSM CMOS technologies (minimal channel length below 100nm) designers of analog circuits are facing new challenges at different stages of the design [1]. The common second order effects are body effect, channel length modulation and subthreshold conduction [7]. This work aim to fill that literature gap. In this work a comparative analysis of two quadrant CMOS analog divider [4] against two quadrant CMOS approximation divider [6] has been carried out. This is for identifying most reliable circuit which safely works in DSM node. This work aim to explore the functionality and performance variations of settling time and resolution.

Section II compares basic working difference of two analog divider circuits such as two quadrant CMOS analog divider against two quadrant CMOS approximation divider and it also gives an overview of various second order effects arises in DSM circuits.. , Statement of problem and solution methodology are discussed in section III. Section IV consolidates the various results obtained and the conclusion remarks and future scope of this work is narrated in Section V.

II. REVIEW OF LITERATURE

This work mainly focuses on two types of analog dividers. The first circuit under study is a two quadrant CMOS analog divider, where , the numerator and denominator input data are provided to the circuit as equivalent currents where as the output quotient is a voltage. In this circuit which some transistors operate in the triode region. The second structure two quadrant CMOS approximation divider the numerator and denominator data are currents and output also derived in current This circuit developed by using two variable second-order Taylor series approximation. The main three second order effects which play prominent role in DSM circuits are body happens if the bulk effect, channel length modulation and subthreshold conduction. Body effect voltage of an NFET drops below the source voltage ie $V_b<0$ more holes attracted to the substrate connection leaving a large negative charge behind. It results in the widening of depletion region.

As a function of that threshold voltage increases. As in the case of channel-length modulation , actual length of the inverted channel gradually decreases as the potential difference between the gate and drain increases. This is the channel-length modulation. Even for gate source voltage less than threshold voltage the drain current is finite, but it exhibits an exponential dependence on gate source voltage called subthreshold voltage.

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III. PROBLEM STATEMENT AND SYSTEM METHODOLGY

Most of the literatures on analog dividers are discussing there performance when they are implemented in long channel MOSFETs. Hence there is lack of information about the performance and reliability of these circuits when they are implemented using lower technological node such as 45nm. This work aim to fill that literature gap. A comparative performance analysis of two prominent analog divider circuits are carried out in work.The aim of this work is to simulate and study the comparative performance variation of two quadrant Analog dividers in 45nm technological node. Spice tool from TANNER is used for this purpose.

IV. RESULT ANALYSIS

A. *Two Quadrant Analog Divider Circuit*

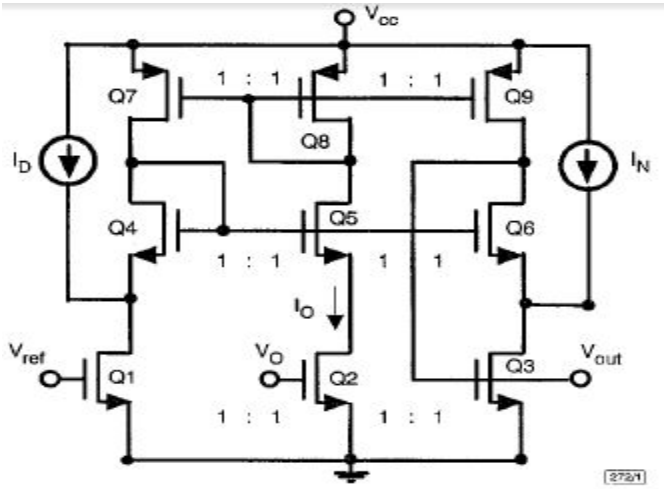


Fig.1 Two Quadrant CMOS Analog divider

In the simplified schematic drawing of the divider shown in Fig 1 , the numerator and denominator are two currents called I_N and I_D respectively. The output is derived from the gate voltage of transistor Q3. The circuit comprises three layers of transistors. The lowest one performs the actual division operation. All transistors are connected in common source mode. Transistors Q_1- Q_3have the same size and are operates in the triode region. The middle layer consists of two source followers Q_5 and Q_6 controlled by the diode connected transistor Q_4, which replicates the drain voltage V_{ds} of Q_1 at the drains of Q_2 and Q_3. Finally, the upper layer is a current mirror mirroring the drain current of the centre transistor Q2 into the drains of Q1 and Q3. The principle of the divider is , considering transistors Q1 and Q2 first. The drain current of Q1 will be equal to the sum of I_D and the mirrored drain current of Q2, we have

$$I_D + I_o = \beta\left((V_{ref} - V_T)V_{ds} - \frac{n}{2}V_{ds}^2\right) \quad (1)$$

where

$$I_o = \beta\left((V_o - V_T)V_{ds} - \frac{n}{2}V_{ds}^2\right) \quad (2)$$

Hence

$$I_D = \beta(V_{ref} - V_o)V_{ds} \quad (3)$$

Now consider the transistor Q3 its drain current is equal to the sum of I_N and Io its gate voltage Vout must adjust itself to satisfy the expression

$$I_N + I_o = \beta\left((V_{out} - V_T)V_{ds} - \frac{n}{2}V_{ds}^2\right) \quad (4)$$

Hence, similarly to eqn. 3,

$$I_N = \beta(V_{out} - V_o)V_{ds} \quad (5)$$

and thus

$$V_{out} - V_o = (V_{ref} - V_o)\frac{I_N}{I_D} \quad (6)$$

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Thus if V_{out} is referred to Vo a two quadrant divider is obtained . The transistor Q3 is being connected to high impedance node ,the loop gain controlling the output voltage can be very large while the output impedance is very large

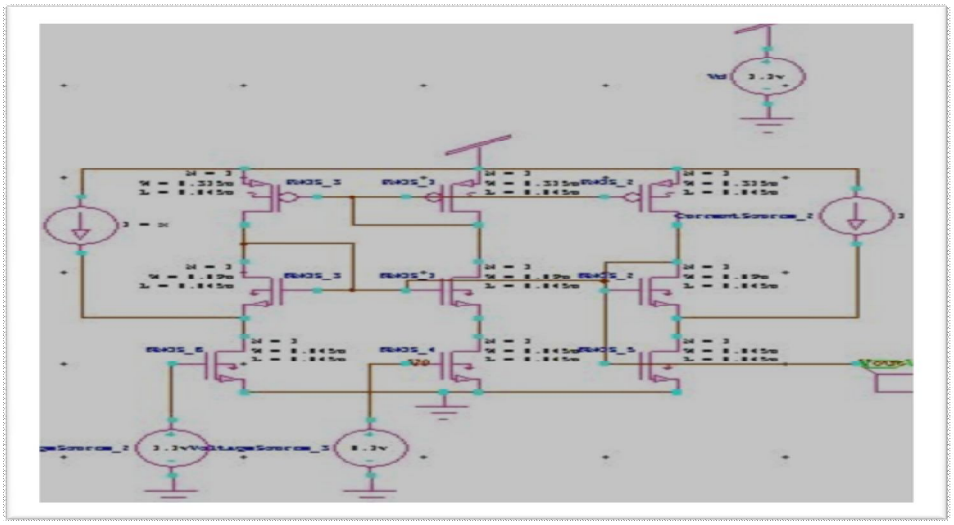
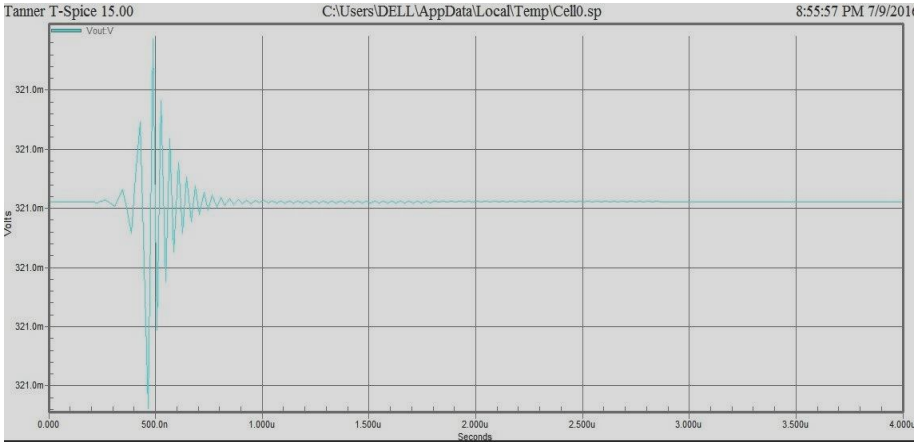


Fig.2 Current-input/Voltage-output Two quadrant divider (simulation set-up)

1) Settling time

It is the time required for the output to reach and stay within a tolerance band. In this circuit upto 2.85uS the output shows ringing and after it goes on to steady



2) DC response of the circuit

Fig.4 shows the measured dc response of two quadrant the analog divider it shows a relative error which is more than approximation divider.

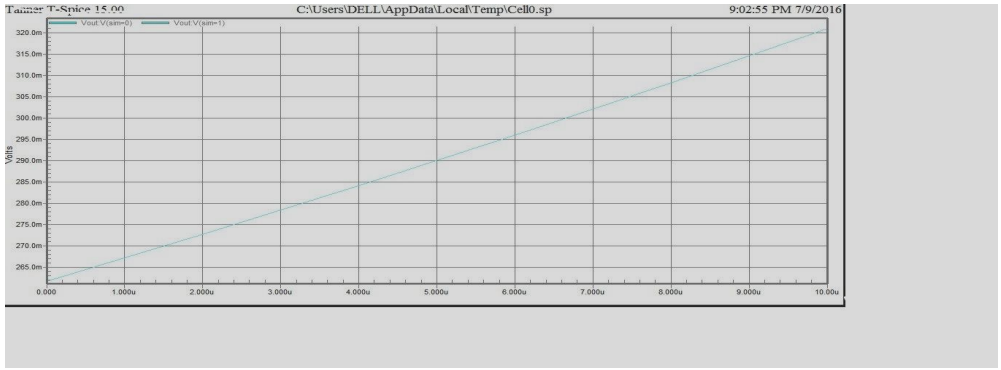


Fig:4 DC Response of the Divider (Vout against I_D from 0-10uA in 1uA steps with I_N 10uA)

3) Resolution

It is the minimum input to produce a perceptible output. This minimum necessary increment is called resolution.

B. Two-Quadrant CMOS approximation Divider

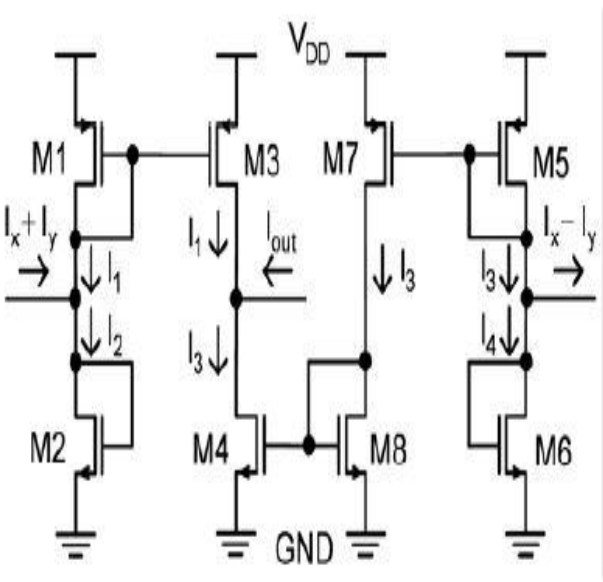


Fig.5 Two Quadrant CMOS Approximation Divider

In Fig.5 the left cell constructed by M1, M2 and current input $I_x + I_y$, produces I_2 and I_1 where

$$I_1 = KV_0^2\left(1 - \frac{I_x + I_y}{4KV_0^2}\right)^2$$

The core cell constructed by M5, M6 and current input $Ix - Iy$,produces I_3 and I_4 Where

$$I_3 = KV_0^2\left(1 + \frac{I_x - I_y}{4KV_0^2}\right)^2$$

In these two =equations

$$V_0 = (V_{DD} - |V_{Tp}| - V_{Tn})/2$$

$$K = K_n = \frac{1}{2}\mu_n C_{ox} W/L = K_p = \frac{1}{2}\mu_p C_{ox} W/L$$

The output current Iout = I_3- I_1

Then

$$I_{out} = I_x - \frac{I_x I_y}{4KV_0^2}$$

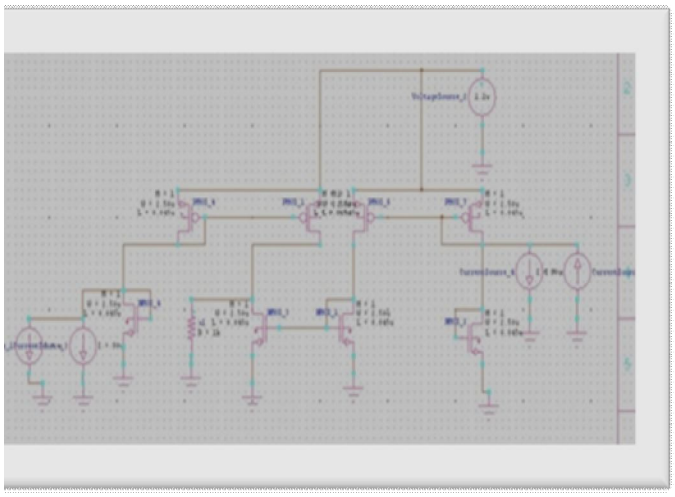


Fig.6 Two Quadrant CMOS Approximation Divider (simulation set-up)

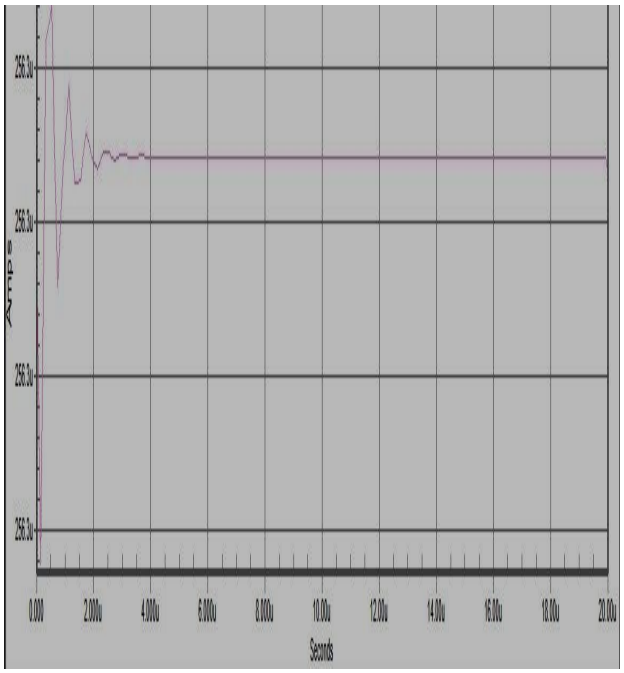


Fig.7 Settling time

This circuit settled out after 3.85uS

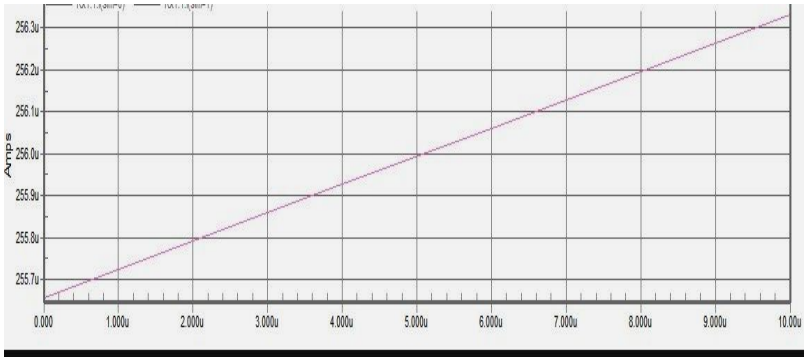


Fig.8 DC response of the divider (Iout against I_x from 0 to 10uA in 1uA steps with I_y ,.10uA

DC response is better than Analog divider in approximation divider

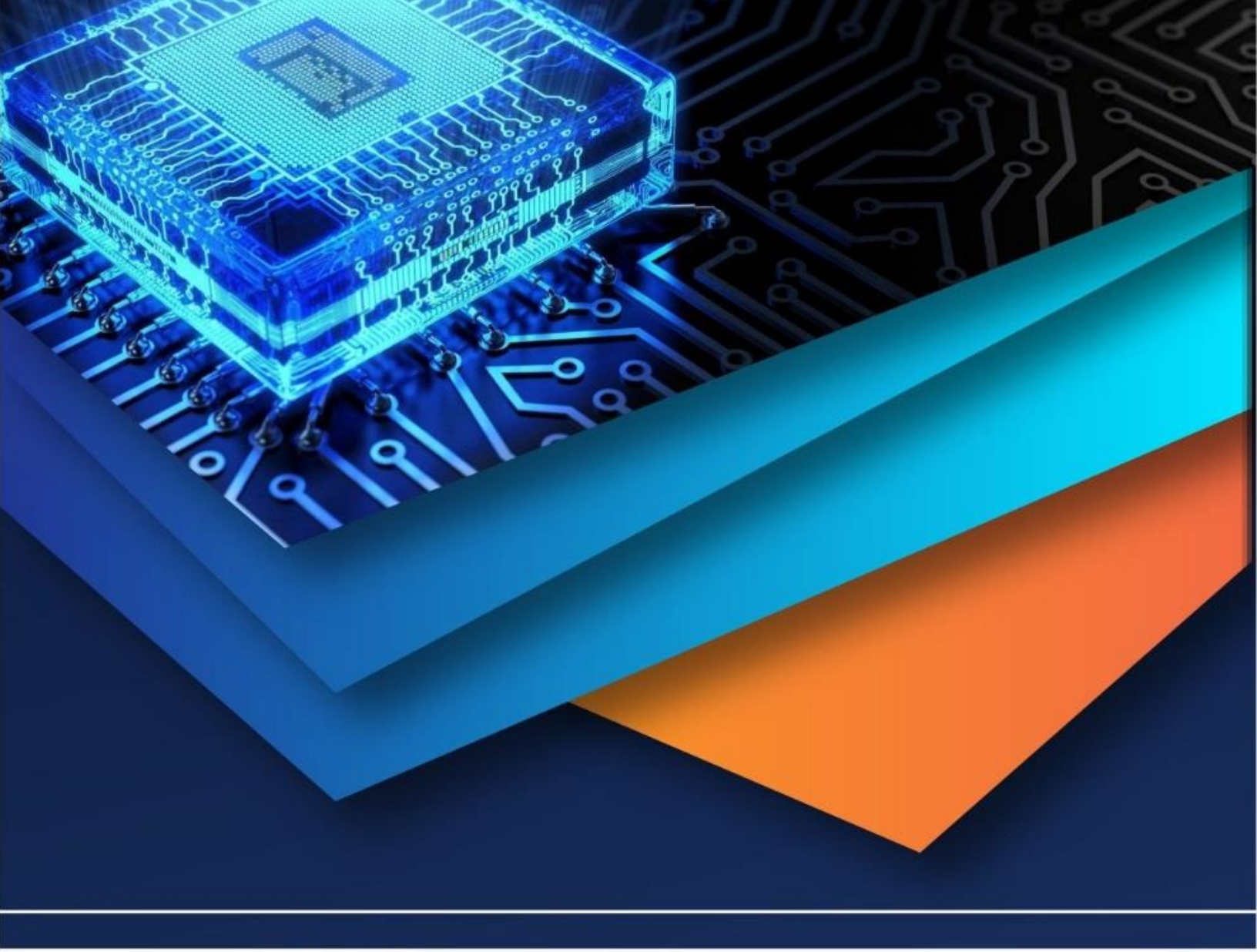
V. CONCLUSION

Parameter	Analog divider-1	Analog divider-2
Settling time	2.85uS	3.85uS
Resolution	0.2mV	.02mV
Relative error	more	less

In this paper , the performance of two analog dividers namely CMOS analog divider and approximation divider are compared according to settling time, resolution and relative error and it is verified that the Analog divider is more reliable than Approximation divider. In this paper process variability is not considered so proposing Monte carlo analysis for reducing the process variations.

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