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Performance Analysis of Ring Oscillators and Current-Starved VCO in 45-nm CMOS Technology

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***Abstract:** This paper presents a relative study among two Ring oscillators architecture (CMOS, NMOS) and current- starved Voltage-controlled oscillator (CS-VCO) on the basis of different parameters like power dissipation ,phase noise etc. All the design has been done in 45- nm CMOS technology node and 2.3 GHz Centre frequency have been taken for the comparison because of their applications in AV Devices and Radio control. An inherent idea of the given performance parameters has been realize by the comparative study. The comparative data shows that NMOS based Ring oscillator is good option in terms of the phase noise performance. In this study NMOS Ring Oscillator have attain a phase noise -97.94 dBc/Hz at 1 MHz offset frequency from 2.3 GHz center frequency. The related data also shows that CMOS Ring oscillator is the best option in terms of power consumption. In this work CMOS Ring oscillator evacuatea power of 1.73 mW which is quite low.*

***Keywords:** Voltage controlled oscillator (VCO), phase noise, power consumption, Complementary metal-oxide-semiconductor (CMOS), Current Starved Voltage-Controlled Oscillator (CS- VCO), Pull up network (PUN), Pull down network (PDN)*

I. INTRODUCTION

Voltage controlled oscillator (VCO) are basic building blocks of modern communication system. It has also applications in AV Devices and Bluetooth which is one of the important application in Electronic applications. MOSFET based VCOs still remains one of the challenging RF blocks, Mainly, the larger close-in phase noise due to higher 1/f noise in CMOS continues to be a challenge [1-2]. Power dissipation is one of the main problem in all system. Mainly, in RF system where the device runs by battery. So,special care is needed to minimize the power dissipation. Due to the technology advancement in last few decades all the design is shifting towards miniaturization [3]. In a MOS transistor, neither of the gate can change the logic level instantly because of its gate capacitances which should be charged for flowing current between source and drain end. As a result, output of each inverter changes after certain delay time. Inverters connected in ring manner can get more delay and may decline the frequency of oscillation [4- 6]. The conventional three stage ring oscillator architecture is shown in the figure 1. The propagation delay time td of signal transition for the full cycle determinesthe time period of Ring oscillator and is given by the equation 1.

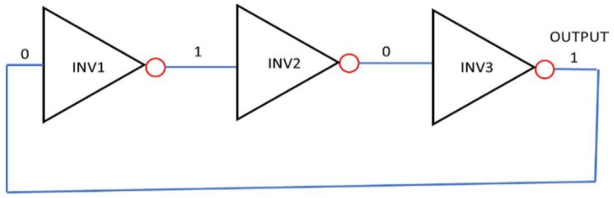


Figure 1: Simple three-stage CMOS Ring Oscillator [10]

Where, N represents the number of inverters connected (delaystages) in a ring oscillator [5]. The equation number (1) showsthe factor two because of two transitions present (low to highand high to low).Thus, the oscillation frequency can be expressed as equation2.

$$T = 2 \times N \times t_d = \frac{1}{2Nt_d} \quad (1)$$

$$f_0 = \frac{1}{T} = \frac{1}{2Nt_d} \quad (2)$$

$$2 \gg t_f + t_r \quad (3)$$

Where, (and t_f) are the rise and fall time period

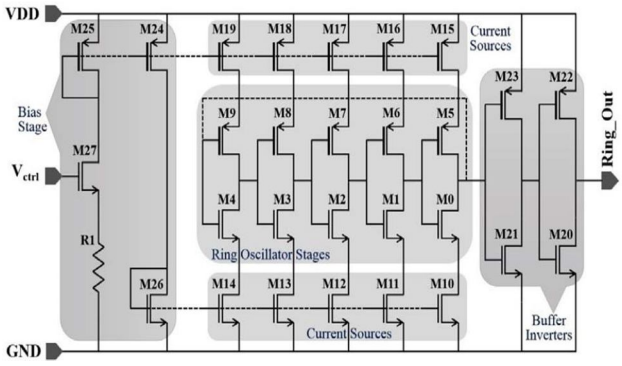


Figure 2: Typical CS-VCO architecture [5]

The paper is organized as follows: the circuit design is presented in section II and the discussion of the simulated result is carried on section III.

II. CIRCUIT DESIGN

A. CMOS based Ring Oscillator

CMOS Ring oscillator is the most popular oscillator topology in recent days due to its CMOS technology in which odd number of not gates are connected in ring manner that's why it is also known as ring oscillator. In this architecture the last inverter's output is connected to the first inverter's input through a feedback path. Schematic diagram of three stage CMOS Ring oscillator is depicted in below figure 3.

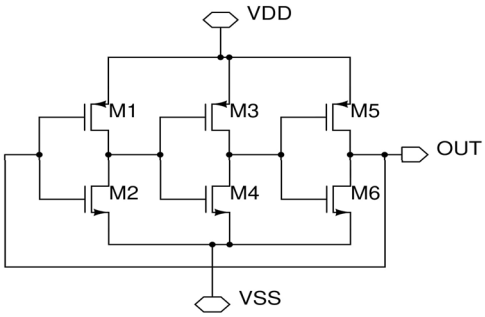


Figure 3: Schematic diagram of CMOS Ring Oscillator

B. Current-Starved Voltage-Controlled Oscillator

In CS-VCO the main advantage is that it provide great balance between minimum area and broad tuning range.In designing CS-VCO architecture three inverters have been connected in a cascaded manner along with PUN and PDN. The PUN network is consisting of PMOS connected load and the PDN network is made by using NMOS transistor. For controlling the frequency one switch namely V_C has been incorporated through the gate of the NMOS transistor. The controlled voltage V_c is varying from 0.4 to 1.1 V and the corresponding frequency varies from 2.03 GHz to 2.59 GHz.The CS-VCO schematic diagram is shown in below figure 4.

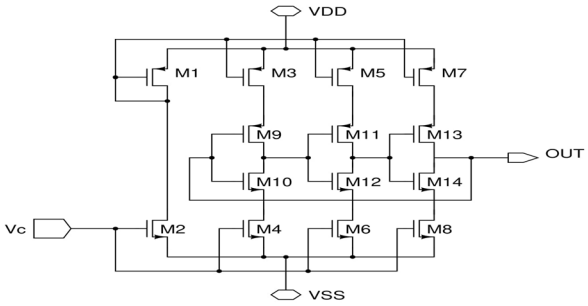


Figure 4: Schematic diagram of CS-VCO

C. NMOS Ring Oscillator

NMOS Ring oscillator is nearly same topology as CMOS Ring oscillator topology. The major difference between architecture is a 122KΩ resistive load is connected in place of PMOS transistor. The output of each drain terminal of NMOS transistor is connected to the gate terminal of the next stage ofNMOS transistor. NMOS Ring oscillator schematic diagramis shown in below figure 5.

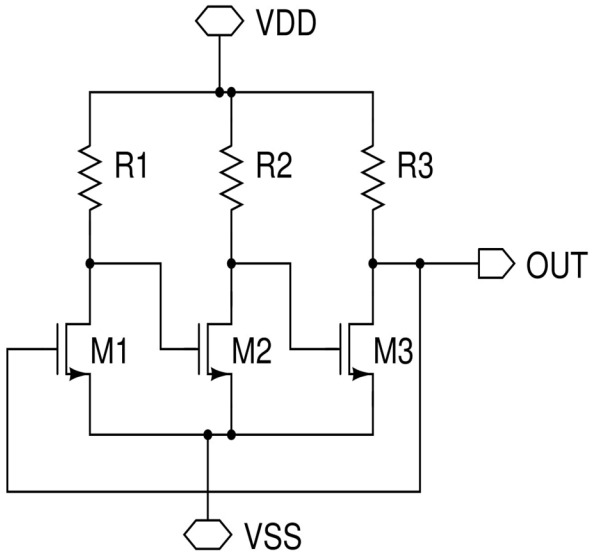


Figure 5: Schematic diagram of NMOS Ring Oscillator

III. SIMULATED RESULTS AND ANALYSIS

In this section we have discussed all three designed oscillator's some of the performance parameters such aspower consumption, phase noise, delay and frequency tuning characteristics. In this work, we have designed CS-VCO circuit which is shown in the previous section in figure 4. Theother two oscillators circuits are depicted in the previous section-II.

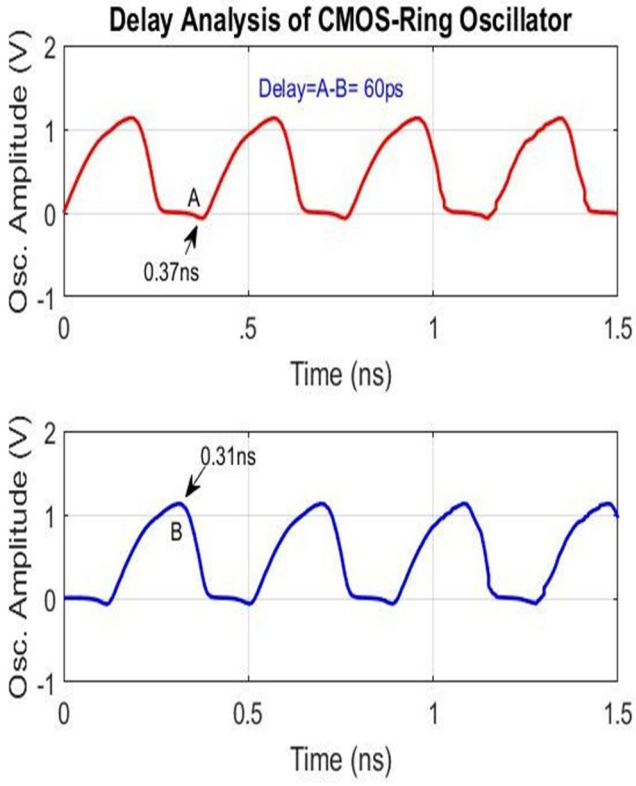


Figure 6: Delay analysis of CMOS Ring Oscillator

To measure the frequency of the CMOS Ring oscillator adelay analysis mechanism has been considered. In the abovefigure 6 trough point is A, which is representing the first inverter's output and crest B point is representing the secondinverter's output. So, delay and frequency can be obtained from the below equations.

$$\text{Delay} = A - B = 60pS \quad (4)$$

$$f_0 = \frac{1}{T} = \frac{1}{2Nt_d} = 2.77\ \text{GHz} \quad (5)$$

As, stated in the last section that control voltage (Vc) tunes the frequency as per the requirement. In the figure 4 we can see that M2, M4, M6 acts as an NMOS current source and M1, M3, M5, M7 acts as an PMOS current source of the circuit. Where Vc is a controlling voltage to change the frequency tuning range by changing the current of the circuit. The designed CS-VCO has achieved a tuning range of 600 MHz with a controlling voltage limit of 0.4 to 1.1V. The maximumfrequency has been obtained is 2.8 GHz at 1.1V control voltage and the minimum frequency has been obtained is 2.05GHz at 0.4 V. The tuning curve is shown in the below figure7.

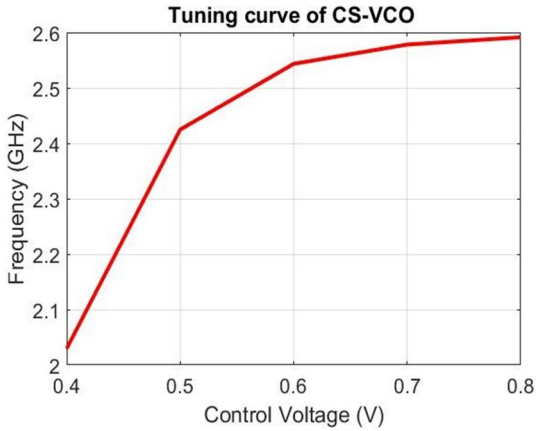


Figure 7: Tuning curve of CS-VCO

We know that the phase noise of the PMOS is less than the phase noise of the NMOS, because PMOS transistor conductsdue to the hole movement as a result it suffers lesser flicker noise than NMOS transistor. But, in this work NMOS Ring oscillator achieves the best phase noise performance of -97.85dBc/Hz at an offset frequency of 1 MHz from the of 2.21 GHz centre frequency. The reason behind for minimum phase noise is due to less number of transistors used in thisarchitecture. Whereas, CMOS Ring oscillator also achieves avery good phase noise performance which is in the range of - 92.3 dBc/ Hz at an offset frequency of 1 MHz from the of 2.21 GHz centre frequency. Whereas, CS-VCO has obtained -88.7 dBc/ Hz which is the worst phase noise performance compare to other topologies. The main cause behind this is to number of transistors used here is more than the other oscillator architecture. The next figure 8 is showing the threedifferent oscillator topologies phase noise performance.

In this work we have compared three different type of oscillator topologies namely CS-VCO, CMOS Ring Oscillator and NMOS Ring Oscillator. The main focus has been given to mainly decrease of the power dissipation because power consumption is an major concern from long time.

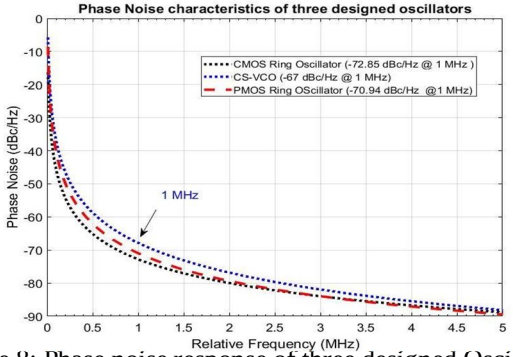


Figure 8: Phase noise response of three designed Oscillators

In this related study we have given main focus on to reduce the power dissipation of the different oscillator topologies. The below figure 9 is showing the three different types of oscillator's power consumption. The easiest way to reduce power consumption is to use lesser number of components used. If we notice NMOS Ring oscillator architecture it has only three transistors used but still power dissipates more due to large resistor have been used as a load. The simulated data shows that CMOS Ring oscillator achieves a best power dissipation response among all other oscillator topologies.

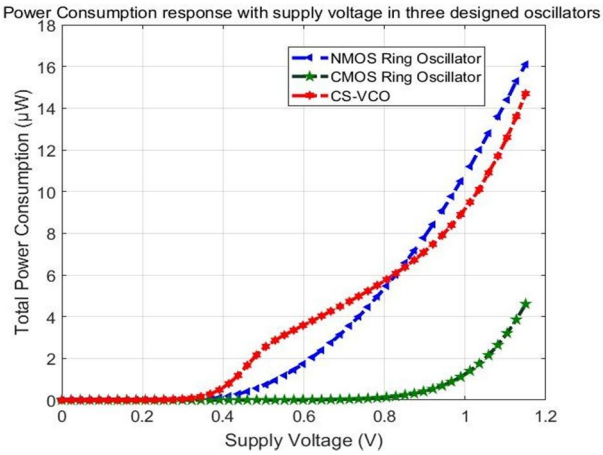


Figure 9: Power consumption response of three designed oscillators

From the figure 9 it can be seen that NMOS Ring oscillator results maximum power dissipation due to its energy loss in terms of heat energy because of register. The CS-VCO has dissipated 12.7 µW which is little-bit higher than CMOS Ring oscillator. The minimum power dissipation has been achieved by CMOS Ring oscillator which is 4.31 µW.
The overall performance analysis based on the comparison of the various performance parameter has been given in the below table-I.

Table I: PERFORMANCE COMPARISON WITH STATE- OF-ART OSCILLATORS

Reference Number & Year		Technology node (nm)	Centre Frequency (GHz)	Frequency Tuning range (%)	Supply Voltage (V)	Phase noise @1 MHz (dBc/Hz)	Total Power Consumption (µW)
[1] & 2011		45	3.125	54	1.8	-91	12600
[3] & 2010		45	5.79	14	1.8	-99.5	-
[4] & 2004		45	5	130	2.5	-82	13500
This Work	CMOS Ring	45	2.21	-	1.1	-92.3	4.31
	CS-VCO	45	2.21	25.08	1.1	-88.7	12.7
	NMOS Ring	45	2.21	-	1.1	-97.85	16.13

IV. CONCLUSION

In this paper we have relate three different topologies oscillator namely Ring oscillator, current starved voltage- controlled oscillator and NMOS Ring oscillator and measure their performance with the existing literature. The design has been done in 45 nm CMOS technology node. Various parameters such as delay, power, phase noise have also been analysed to maximize efficiency. Also, From the simulation results it can be said that higher oscillation frequency can be achieve by increasing control voltage. The three oscillators have been designed in same centre frequency of 2.21 GHz with a 1.1V supply voltage. From the above study of different oscillators, it can be observe that the NMOS Ring Oscillator has obtained the best phase noise performance in comparison to other oscillator topologies where as in terms of power consumption CMOS Ring oscillator is the best choice among the other oscillators. So, finally we cocluded that CMOS Ring oscillator would be the best choice among these three designed oscillators.

V. ACKNOWLEDGMENT

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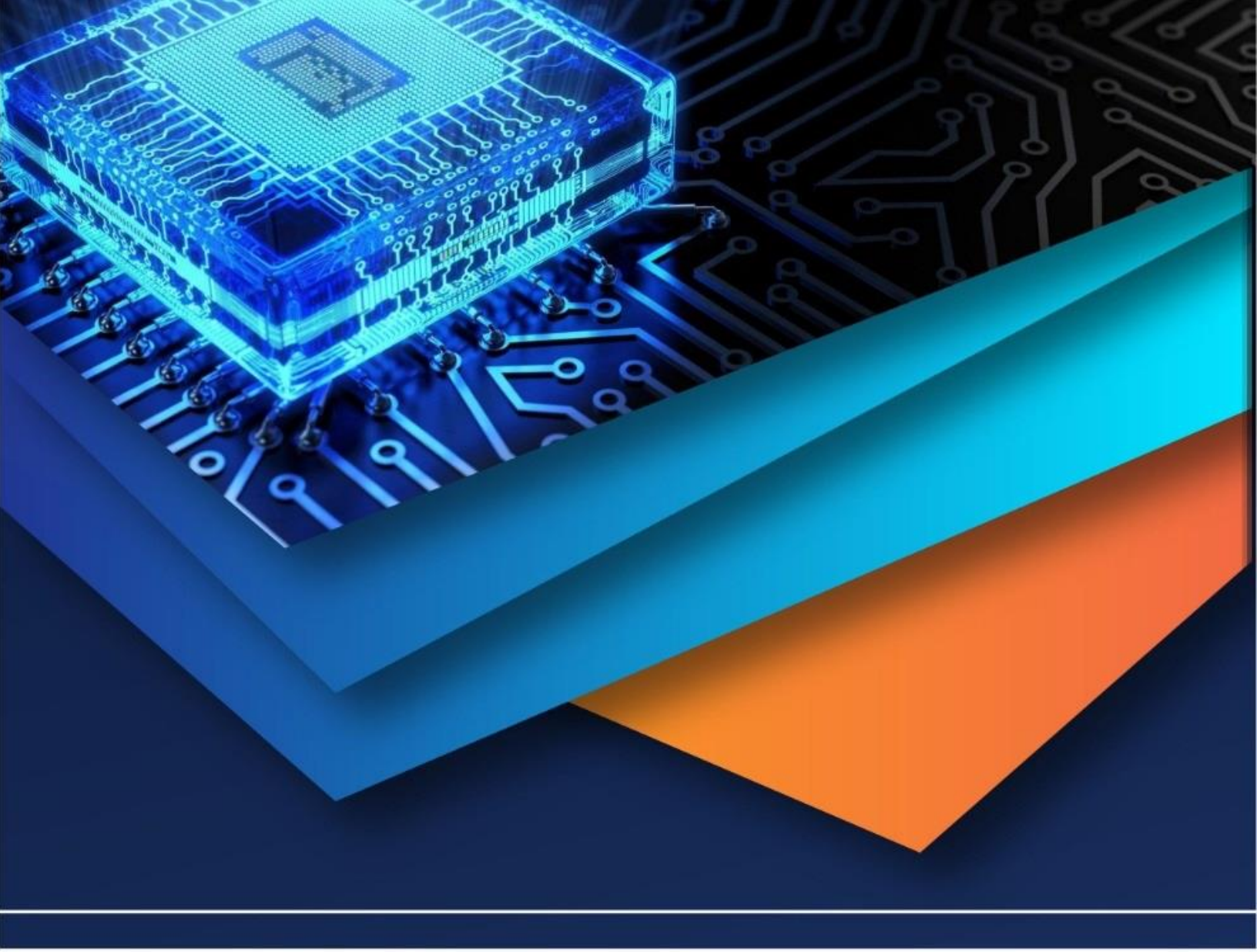
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