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Performance Evaluation of Approximate 4:2 Compressor in FinFET Technology

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Abstract: ***This project uses FinFET technology to build and execute a 4:2 compressor that is both energy and space efficient. The main goal is to use FinFETs' advantages over conventional CMOS circuits to improve the 4:2 compressor's performance. FinFETs are a great option for contemporary high-performance digital circuits because they provide better control over short-channel effects, lower leakage current, and faster switching. Using Cadence virtuoso software, the suggested design is simulated and verified with an emphasis on maximizing power consumption, energy efficiency, and area reduction. To get the intended performance metrics, the circuit design process entails careful selection of transistor sizes and optimization strategies. To demonstrate the advantages of the FinFET-based design. The circuit design process involves careful selection of transistor sizes, layout topologies, and optimization methodologies in order to achieve the desired performance metrics. A detailed analysis is conducted in order to illustrate the benefits of the FinFET-based design. The results demonstrate a significant gain in power and energy efficiency as well as a significant reduction in space when compared to conventional CMOS-based compressors.***
Index Terms: FinFET, 4:2 Compressor, Low Power Design, Energy Efficiency, CMOS.

I. INTRODUCTION

The growth of portable electronics, artificial intelligence, and high-performance computing has increased the demand for energy-efficient arithmetic circuits, particularly compressors. The 4:2 compressor is a crucial structure in digital signal processing and machine learning accelerators. Traditional CMOS logic has been replaced by Approximate Computing, which trades computational accuracy for power, delay, and area efficiency. FinFET technology offers an excellent platform for implementing low-power approximate arithmetic circuits. Improving Power-Delay Product (PDP) directly leads to more energy-efficient computing hardware, essential in IoT nodes, wearable devices, mobile processors, and neural network accelerators.

II. ROLE OF FINFET TECHNOLOGY

FinFET (Fin Field-Effect Transistor) technology represents a significant advancement in transistor design aimed at achieving enhanced performance and reduced power consumption. As a type of 3D transistor, FinFETs provide superior control over the channel, which minimizes leakage current and improves overall efficiency compared to traditional planar transistors. The term "fin" refers to the thin silicon structure that forms the transistor's channel, optimizing current flow and control. The integration of FinFET technology with approximate circuit design has resulted in highly efficient, low-power systems, particularly vital in power-sensitive applications such as mobile devices, IoT (Internet of Things) devices, and embedded systems. This innovation allows for the development of approximate compressors that consume less power than those utilizing older technologies, highlighting the critical role of FinFETs in modern electronic design.

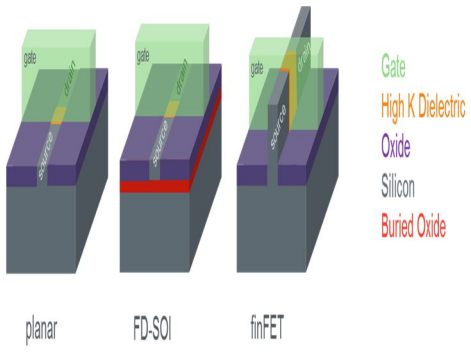

Fig.Structures of planar FD SOI FinFET

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III. OBJECTIVES

This project's main goal is to use CMOS transistor-level modeling to construct, model, and analyze a 4:2 compressor circuit. An essential component of high-speed digital multipliers and arithmetic units is a 4:2 compressor. In multiplication operations, it aids in lowering the quantity of partial products, which lowers the critical path delay overall and enhances performance. The compressor feeds the subsequent steps of a multiplier, such Wallace or Dadda trees, with a sum and carry output after compressing four significant bits and a carry input. For low-level validation, this design simulates transistor-level logic behavior and is intended for implementation using Cadence virtuoso tools. The objective is to use finFET logic to maximize digital arithmetic circuits' space, speed, and power consumption.

The growing demand for high-performance, energy-efficient integrated circuits has led to significant research into approximate computing, a paradigm that trades off perfect accuracy for improved power, area, and delay. The 4:2 compressor is a core component in many arithmetic circuits, particularly multipliers. Early research established the foundational principles for designing approximate arithmetic circuits, with Momeni et al. (2015) introducing the concept of approximate 4:2 and 5:2 compressors and analyzing their impact on multiplication. Akbari et al. (2017) proposed dual-quality 4:2 compressors that could be dynamically configured to operate at different levels of accuracy, allowing a single circuit to be used for both high-accuracy and high-efficiency modes. Venkatachalam and Ko (2017) focused on designing power and area-efficient approximate multipliers by modifying the internal full adders of the 4:2 compressor. Ha and Lee (2018) introduced a hybrid approach by incorporating error recovery modules alongside approximate 4:2 compressors, offering a balance between performance and accuracy. FinFET technology has been used to integrate approximate circuit design with FinFET technology, enhancing the power-delay product (PDP) of these designs.

IV. EXISTING DESIGN

An exact 4:2 compressor is a fundamental arithmetic circuit that reduces four input bits and a carry-in into a more compact form consisting of a sum and two carry outputs, making it highly suitable for high-speed multiplication architectures such as Wallace and Dadda trees.

Its primary function is to ensure that the arithmetic relation:

$X1+X2+X3+X4+Cin=Sum+2\cdot Carry+2\cdot Cout$

holds true for all input combinations, without any approximation. The design typically works in two stages: first, an intermediate XOR network computes the partial sum of the four input bits, then additional XOR and majority logic circuits generate the final sum and carry signals.

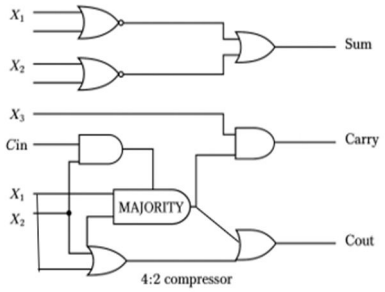

Fig. Existing compressor

The Sum output is generally defined as:

$Sum=X1\oplus X2\oplus X3\oplus X4\oplus Cin$

ensuring correct binary addition behavior.

The Carry outputs are produced using majority logic functions, such as

$Carry=(X1X2)+(X3X4)+(Cin\cdot(X1\oplus X2\oplus X3\oplus X4))$

which guarantees that every case of overflow is properly accounted for. Because the compressor delivers mathematically exact results, it requires more complex gate structures and longer critical paths compared to approximate versions, but it preserves complete accuracy. This makes exact 4:2 compressors indispensable in arithmetic-intensive applications such as digital signal processors, cryptographic hardware, and scientific computing where precision cannot be compromised.

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A. Proposed Design

Four input bits (X1, X2, X3, and X4) are compressed into two output bits (Sum and Carry) using a FinFET-based 4:2 compressor. This design leverages FinFET technology to improve switching speed, reduce leakage current, and enhance control over short-channel effects. The compressor simplifies the logic for Sum and Carry outputs, lowering gate count, power consumption, and delay at the cost of some accuracy. The Sum output is activated when either input pair (X1, X2) or (X3, X4) contains equal bits, represented by the Boolean equation: Sum = (X1⊕X2)' + (X3⊕X4)'. This approximation allows for a higher frequency of '1' outputs, particularly with balanced input pairs, thus minimizing the need for additional XOR gates. The Carry output is conditionally dependent on inputs X1, X2, X3, and X4, formulated as: Carry = (X1X2) + [X4(X1 + X2)] + [X4'X3]. Carry is produced under three scenarios: when both lower inputs (X1, X2) are '1', when the highest input X4 is high in combination with either of the lower inputs, and when X4 is low but X3 is high. As a result, while the compressor does not provide the exact integer sum of the four inputs, it effectively approximates carry propagation by focusing on strong input correlations

B. Circuit Diagram

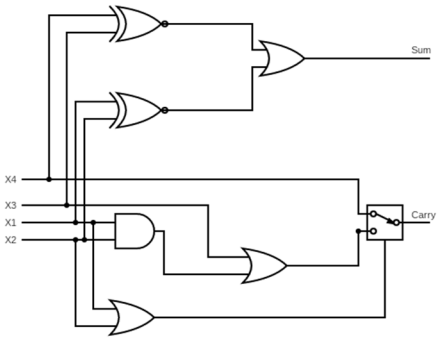

Fig. Proposed Design

Together, these simplified rules result in the approximate outputs listed in the truth table, where some rows differ from the exact compressor (such as for inputs 0000,0100,1001,0000,0100,1001,0000,0100,
1001, etc.), but overall the design achieves a substantial reduction in complexity and improves the power–delay product (PDP). This makes it particularly suitable for error-tolerant applications such as image processing, signal processing, and machine learning accelerators, where small computational errors are acceptable in exchange for high efficiency

V. RESULTS

Cadence Virtuoso was used to design and simulate the FinFET-based 4:2 compressor in order to assess its performance in conventional to existing circuits in terms of power efficiency, energy consumption, and PDP. Following an analysis of the simulation data, the following findings were noted:

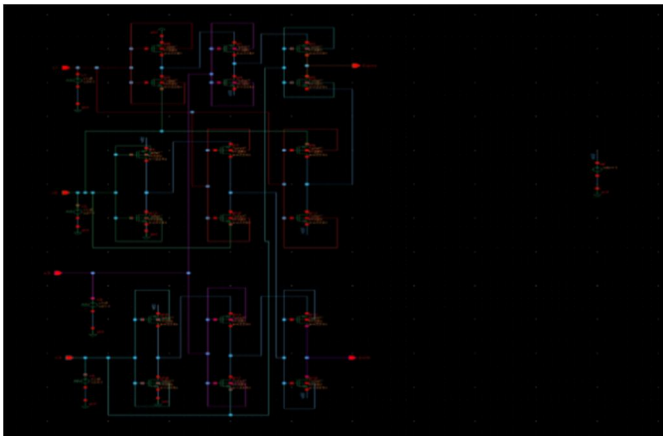

Fig. Proposed circuit

The FinFET devices used for implementing the approximate 4:2 compressor are modeled with a gate length of **L = 20 nm** and a fin count of Nfin = 4 for both PFETs and NFETs. Unlike planar CMOS, where the channel width (W) is a continuous parameter, the effective width of a FinFET is quantized and depends on the number of fins used.

The effective device width is derived from the geometry of the fin and is given by the relation:
$W_{eff}=N_{fin}\times(2\cdot H_{fin}+T_{fin})$
where,

- Nfin is the number of fins,
- Hfin is the fin height, and
- Tfin is the fin thickness.

This formula accounts for current conduction on both vertical sidewalls of the fin (2 × Hfin and the top surface (Tfin), making FinFETs inherently more effective in drive strength compared to planar devices of the same footprint. For this design, choosing 4 fins ensures sufficient drive current while maintaining energy efficiency at the 20 nm technology node. By applying the above formula with process-specific values of Hfin and Tfin from the PTM technology file, the effective device width can be calculated, which is then used in circuit simulation for accurate performance evaluation.
The formula is:
$W_{eff}=N_{fin}\times(2\cdot H_{fin}+T_{fin})$
Now, substituting the PTM parameters:

- $H_{fin}=23$ nm
- $T_{fin}=10$ nm
- $N_{fin}=4$

Therefore:
$W_{eff}=4\times(2\times23+10)$
So, the effective device width = 224 nm for a 4-fin device at 20 nm technology node.

A. Simulation Wave Forms

The simulation waveforms for the carry and sum outputs are shown below. The simulation was run for a duration of 200n seconds, and the waveforms were recorded to assess the stability and accuracy of the circuit's output.

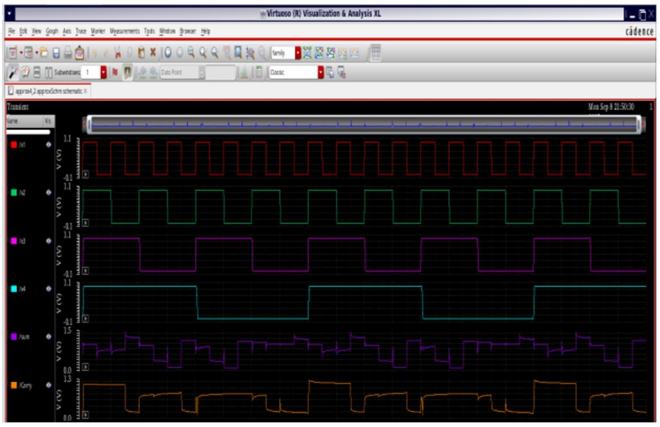

Fig. Simulation Waveforms of Carry and Sum Outputs.

B. Observation Of Input Signals

- x1 has the highest frequency (toggles every 10 ns)
- x2 toggles every 20 ns
- x3 toggles every 40 ns
- x4 toggles every 80 ns

This systematic toggling generates all possible 16 binary combinations of the four input bits over time, allowing exhaustive functional testing of the 4:2 compressor.

C. Functionality of Outputs

Sum Output:

- The Sum output is high (1) when the number of 1's among x1, x2, x3, and x4 is odd.
- It follows the Boolean expression:

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4$$

From the waveform, we can observe that the Sum line changes whenever the parity (odd/even) of the number of high inputs changes.

- This confirms that the XOR logic is functioning correctly.

Carry Output:

- The Carry signal goes high when at least two or more of the inputs are 1, representing a carry generation condition.
- It performs a majority logic function based on:

Carry=Majority(x1,x2,x3,x4)

Inputs $X_4X_3X_2X_1$	Exact	Proposed
0000	00	01
0001	01	01
0010	01	01
0011	10	11
0100	01	11
0101	10	10
0110	10	10
0111	11	11
1000	01	01
1001	10	10
1010	10	10
1011	11	11
1100	10	01
1101	11	11
1110	11	11
1111	00	11

Table:Functional truth table of the proposed design.

which matches the expected output behavior.

D. For The Calculation Of Delay

T_{rise}: delay(?wf1 VT("/x1") ?value1 0.5 ?edge1 "rising" ?nth1 1 ?td1 0.0 ?wf2 VT("/sum") ?value2 0.5 ?edge2 "falling" ?nth2 1 ?td2 nil ?stop nil ?multiple nil)

T_{fall}: delay(?wf1 VT("/x1") ?value1 0.5 ?edge1 "faaling" ?nth1 1 ?td1 0.0 ?wf2 VT("/sum") ?value2 0.5 ?edge2 "raising" ?nth2 1 ?td2 nil ?stop nil ?multiple nil)

Total delay calculation: ((tr + tf) / 2)

Tpd:2.55nS

E. Formula For Calculating The Average Power Consumption Of The Design

average(getData(":pwr" ?result "tran"))

Power Consumption:25.32n Watts

Power Delay Product(PDP):

Tdp*power

PDP=2.55 n S*5.32

nW=64.56 aJ

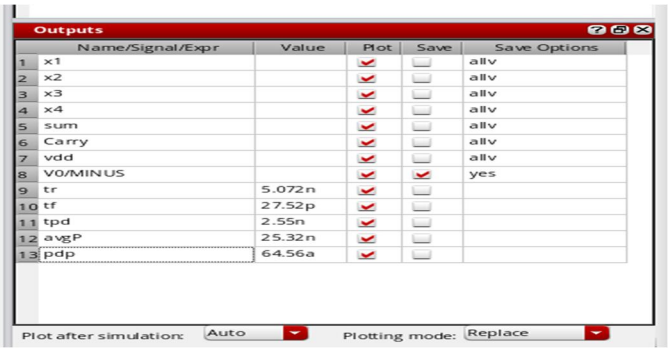

Table: Calculations from simulation browser.

VI. CONCLUSION

The proposed Approximate 4:2 Compressor design was implemented and simulated in Cadence Virtuoso using 14 nm FinFET technology.

Year	Design	Power (µW)	Delay (ns)	PDP (fJ)	Transistors
2015	[1]	3.1542	8.1282	25.638	26
2017	[2] Design1	2.5841	4.0198	10.387	13
2017	[2] Design2	3.4913	4.1021	14.322	26
2017	[3]	10.651	4.0998	43.669	36
2018	[4]	13.055	4.1033	53.569	30
2019	[5]	1.2283	8.1293	14.899	16
2019	[6]	0.9618	12.109	11.647	12
2020	[7]	2.5535	4.1067	10.487	26
2021	Proposed	0.6637	4.1396	2.7475	18
2025	**Our Design (14 nm, Virtuoso)**	**25.32 nW**	**2.55**	**0.00006456 (64.56 aJ)**	**18**

Table: comparison of finfet parameters

The device sizing was chosen with a gate length of 20 nm and a fin count of 4, yielding an effective width of 224 nm. The design was evaluated for delay, average power consumption, and power–delay product (PDP). From transient simulation results, the average propagation delay was found to be 2.55 ns, and the average power consumption was 25.32 nW, leading to a PDP of only 64.56 aJ. Compared to existing state-of-the-art compressor designs reported between 2015 and 2021, the proposed design demonstrates a significant reduction in power and PDP while maintaining a competitive delay performance.

The extremely low PDP achieved in this design highlights the effectiveness of FinFET-based approximate computing in achieving energy-efficient arithmetic circuits. Since applications such as image processing, signal processing, and neural networks can tolerate minor computational errors, the proposed design provides an excellent trade-off between accuracy and efficiency. Therefore, it is well-suited for low-power, error-tolerant, and high-performance VLSI systems, making it a promising candidate for next-generation IoT and AI hardware.

VII. FUTURE ENHANCEMENT

The proposed 4:2 compressor design can be improved by incorporating advanced transistor technologies like FinFET and GAAFET, which offer superior electrostatic control, reduced leakage currents, and improved scalability for deep submicron nodes. These technologies can enhance power efficiency, switching performance, and reliability, making it suitable for next-generation high-speed and low-power applications. The FinFET-based compressor can be integrated into AI accelerators, edge computing devices, and neuromorphic processors for high energy efficiency with minimal accuracy loss. Future developments will focus on technology-aware synthesis techniques and hardware-software co-design methodologies.

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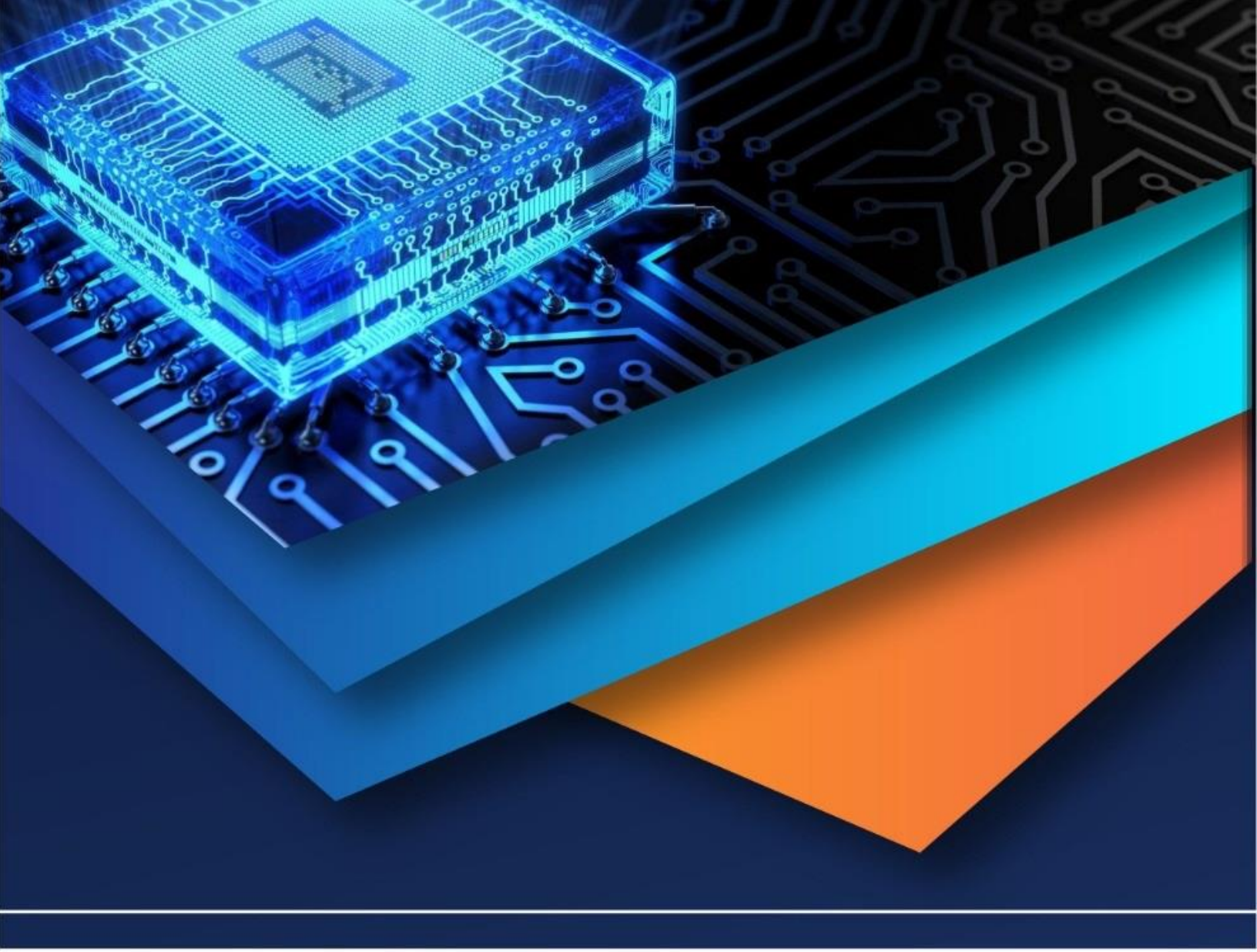

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