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Power Optimization for Enhanced Data Transmission in VLSI Router Buffers

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***Abstract:** One essential component of contemporary communication systems is the planning and execution of effective routing topologies. In this research, a redesigned VLSI-based router architecture optimized for low power consumption and fast data transmission speed is proposed. The suggested architecture and state-of-the-art VLSI design approaches to provide efficient data routing to any of the outputs. Through simulations, the design's performance is assessed. The simulation was run using the VHDL programming language in Xilinx software. The design includes the Arbiter, Cross Bar, and FIFO blocks. A major step toward the creation of high-performance communication systems has been made with this study. In the proposed method by using clock gating the overall power of the design and delay and area will be reduced compared to the existing architecture.*

I. INTRODUCTION

Because it can manage the rising number of cores in System-on-Chip (SOC) designs, the Network-on-Chip (NOC) architecture has gained popularity in the field of communication infrastructures. This architecture was unveiled as a response to the shortcomings of the SOC paradigm and the previously favored communication technologies, which suffered from problems including low core utilization, poor reuse, excessive complexity, and poor scalability A thorough grasp of NOC's design ideas, including topology, control flow, switching techniques, routing strategies, and the components utilized in its implementation, is vital. NOC is defined by its network configuration and data flow. These parts, which are utilized to control the Arbiter, Router, Crossbar, and FIFO Buffer,

A. Fifo Buffer

FIFO stands for "First In/First Out" and is a way for the UART to process data more smoothly. It is a memory device that allows for flow control from the modem to the CPU and vice versa. The UART stores incoming data in the FIFO buffer, and the FIFO buffer holds it until the CPU is ready for it. In the other direction, the CPU can send a bunch of data to the modem, which sits in the FIFO buffer and streams out as the UART is ready to pass it to the modem. There are actually two separate buffers, one for incoming and one for outgoing. FIFO buffers can be adjusted for the number of bytes they can hold at a time. Knocking the FIFO buffers down a notch can help with connection problems and disconnections, because without them, the modems respond more directly to each other. But as the FIFO buffers are turned down, performance will be decreased.

B. Router

A router is a device that connects two or more packet-switched networks or sub networks. It serves two primary functions: managing traffic between these networks by forwarding packets to their intended IP address and allowing multiple devices to use the same Internet connection. There are several types of routers, but most routers pass data between LAN (local area network) and WANs (wide area network) A LAN is a group of connected devices restricted to a specific geographic area. A LAN usually requires a single router. A WAN, by contrast, is a large network spread out over a vast geographic area. Large organizations and companies that operate in multiple locations across the country, for instance, will need separate LANs for each location, which then connect to the other LANs to form a WAN.

Because a WAN is distributed over a large area, it often necessitates multiple routers and switches. An Arbiter is used to provide access of data bus whenever there is more than one requester for the bus, we can say arbiter is like a traffic police constable who grant the access of road to the vehicle drivers according to the traffic rules. Consider the case of a System-on-Chip (SOC). When we say SOC it symbolizes a complete system compromising of different units on single chip. In SOC the data transfer between different units takes place via single bus. So, to remove ambiguity we need to provide bus to a single unit at a particular time. Here we have different units as requesters and bus as our resource.

C. Round Robin Arbiter

A Round Robin Arbiter is a type of hardware or software component used in computer systems, particularly in the field of digital logic and system design. Its primary purpose is to manage access to a shared resource by multiple competing processes, modules, or components. The round robin arbitration technique is a fair, systematic way to allocate resources in a cyclic manner, ensuring that every competing entity gets a chance to access the resource.

D. Crossbar

Crossbar networks allow any processor in the system to connect to any other processor or memory unit so that many processors can communicate simultaneously without contention. A new connection can be established at any time as long as the requested input and output ports are free. Crossbar networks are used in the design of high-performance small-scale multi processors, in the design of routers for direct networks, and as basic components in the design of large-scale indirect networks. A crossbar can be defined as a switching network with N inputs and M outputs, which allows up to min {N, M} one-to-one interconnections without contention. System-on-chip (SOC) designs solve challenging design problems in different application domains by integrating diverse domain expertise. The successful design of such complex single-chip applications requires expertise in several technology areas such as communication, multimedia, encryption, and analog and RF designs. These technologies are increasingly hard to find in a single design house.

Hence, there is a business model where the specialists in the specific domain provide the IP, and the SOC designer focuses on the system integration design aspects. Success will rely on using appropriate design and process technologies and the ability to interconnect existing components reliably in a plug-and-play fashion. SOC design methodologies are hence shifting from computation-centric to communication-centric ones. The design of the SOC interconnect thus demands significant research to ensure optimal communication between the components.

Network topology describes how networks fit together. Routers are the entities that connect networks to each other. A router is any machine that has two or more network interfaces and implements IP forwarding. However, the system cannot function as a router until properly configured, as described in Router. Routers connect two or more networks to form larger internetworks. The routers must be configured to pass packets between two adjacent networks. The routers also should be able to pass packets to networks that lie beyond the adjacent networks.

The following figure shows the basic parts of a network topology. The first illustration shows a simple configuration of two networks that are connected by a single router. The second illustration shows a configuration of three networks, interconnected by two routers. In the first example, Router R joins Network 1 and Network 2 into a larger internetwork. In the second example, Router R1 connects Networks 1 and 2. Router R2 connects Networks 2 and 3. The connections form a network that includes Networks 1, 2, and 3.

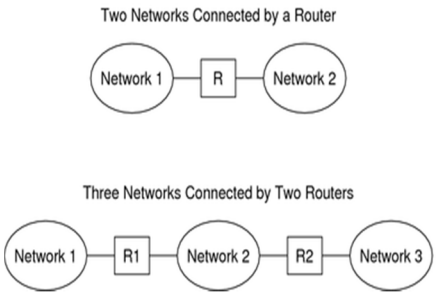

Figure1 Basic parts of a network topology

Flow routing is a network routing technology that takes variations in the flow of data into account to increase routing efficiency. This increased efficiency helps avoid excessive latency and jitter for streaming data. Flow routing uses adaptive routing algorithms that base their decisions on the traffic conditions between a computer and all the other computers it is connected to on the sub network. Based on the traffic within this sub network, flow routing makes the decision about which computer to send a packet to. A flow router evaluates traffic flows in Real Time -- based on an ID, route, time of receipt and rate of flow -- to keep streaming traffic moving as quickly as possible. Rather than routing individual packets, it observes and evaluates flows of multiple packets to gather statistics, including source, destination, amount of traffic "in flight" and stream duration.

E. SOC

A system on a chip, also known as an SOC, is essentially an integrated circuit or an IC that takes a single platform and integrates an entire electronic or computer system onto it. It is, exactly as its name suggests, an entire system on a single chip. The components that an SOC generally looks to incorporate within itself include a central processing unit, input and output ports, internal memory, as well as analog input and output blocks among other things. Depending on the kind of system that has been reduced to the size of a chip.

II. LITERATURE SURVEY

1) *Balharith, Taghreed, and Fahd Alhaidari. "Round robin scheduling algorithm in CPU and cloud computing: a review." 2019 2nd International Conference on Computer Applications & Information Security (ICCAIS). IEEE, 2019*

The Round Robin algorithm is considered as one of the most common scheduling algorithms due to its simplicity and fairness. It is applied in many fields to improve system performance. In this paper, we conducted a review on how the researchers applied the RR algorithm in the CPU scheduling as well as in the cloud computing environment. Many researchers proposed various techniques in order to improve the RR algorithm and selecting the optimal time quantum which plays a vital role to enhance this algorithm. This paper presents a review and new classification on these techniques. Studies have been classified into two categories: RR based on static quantum, and RR based on dynamic quantum. Furthermore, the second category was divided into dynamic quantum for each round and dynamic quantum for each process. Moreover, an analytical comparison has been provided. This review can be a strong starting point for researchers who seek to enhance or optimize RR algorithm or either apply it in other fields.

Summary: The Round Robin algorithm is considered as one of the most common scheduling algorithms due to its simplicity and fairness.

2) *S. Madhavan and H. P. V, "Design and Verification of 1X5 ROUTER," 2022 IEEE 2nd Mysore Sub Section International Conference (MysuruCon), Mysuru, India, 2022, pp. 1-6, doi: 10.1109/MysuruCon55714.2022.9972633.*

A router is a device that forwards the data packets along with the networks, commonly two LANs or WANs. It is an Open Systems Interconnection (OSI) layer 3 routing device. Depending on the address content in the incoming packets, this router routes a packet to an output channel. The packet has 3 parts, namely Header, payload and parity. In this project, a router of packet width 8 bits, payload length ranging from 1 byte to 31 bytes is implemented. This design is implemented in Verilog, verification is done using Universal Verification Methodology (UVM) and QuestaSim is used for functional coverage. This router consists of 4 submodules, namely First in First Out (FIFO), registers, Synchronizer and Finite State Machine (FSM). Five FIFOs are employed here and the final top module design is simulated and synthesized. The advantage of this router design is that it can receive only one packet at a time but five packets can be read out simultaneously.

Summary: A router is a device that forwards the data packets along with the networks, commonly two LANs or WANs

III. EXISTING METHOD

The circuit was implemented using structural modelling. Initially smaller blocks are simulated and finally complete router circuit is implemented. The smaller blocks are as follows

1) Working of FIFO is based on Write pointer, read pointer, Read enable and write enable. So, based on that the input data given is 10100101. When the write enable is high and write pointer points towards the empty space in the FIFO, the data is read inside the FIFO.
2) When read enable is high, it is observed that the data is read from the FIFO which is w_rd_data.
3) Based on req signal in the figure, the data is being read from each FIFO at particular intervals of time. Initially when the reset signal is high, the request signal is always 000 that means it is not taking data from any of the available FIFO's.
4) Crossbar is a combinational circuit where multiple MUX and DEMUX are connected together to transfer a data. The sel is the main signal here, using that we can easily analyses the working of the crossbar. When sel line is 00, the data from SC is transferred to CNI, and data from SN is transferred to NWI Similarly, it works based on the truth table for each value of select signal from 00 to 11 {00, 01, 10,11).
5) Old Router Architecture is implemented in Xilinx software. As mentioned earlier the old design consists of IFO, Arbiter, Crossbar, where each block has its own task and the total combination works as router. After designing all these blocks individually, using structural modelling, all these blocks are combined and simulated. Using X Power analyse, the power consumption rating is obtained for this router design.

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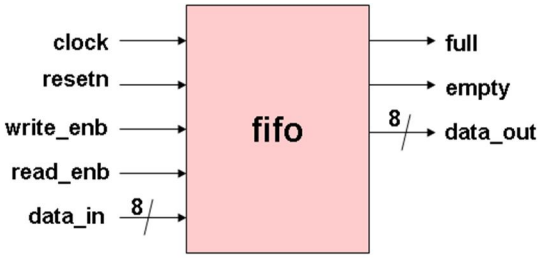


Figure 2 The circuit was implemented
using structural modelling

When write _enb is high then wr_ptr points to the write positions in the memory, automatically wr_ptr keeps on incrementing when data is being written into the write address in the memory. When reedmen is high, then data is being read from the fifo, then automatically rd_ptr keeps on incrementing when data is being read out from the fifo then rd_ptr keeps on decrementing, Detain of fifo is exactly 8 bits and output of fifo is 8 bit output. The drawback in existing method is the data is routed only from center to center, north to north, south to south. The circuit was implemented using structural modelling. Initially smaller blocks are simulated and finally complete router circuit is implemented.

IV. PROPOSED METHOD

working of FIFO is based on Write pointer, read pointer, Read enable and write enable. So, based on that if the input data given is 10100101. When the write enable is high and write pointer points towards the empty space in the FIFO, the data is read inside the FIFO. When read enable is high, it is observed that the data is read from the FIFO which is w_rd_data. the output of Arbiter block which works based on the principle of Round Robin Scheduling Algorithm. Based on req signal in the figure, the data is being read from each FIFO at particular intervals of time. Initially when the reset signal is high, the request signal is always 000 that means it is not taking data from any of the available FIFO's.

Crossbar is a combinational circuit where multiple MUX and DEMUX are connected together to transfer a data. The sel is the main signal here, using that we can easily analyses the working of the crossbar. When sel line is 01100 the data from SC is transferred to the west likewise by using the selection line the data is routed to any of the outputs. After designing all these blocks individually, using structural modelling, all these blocks are combined and simulated. Using X Power analyses, the power consumption rating is obtained for the router design.

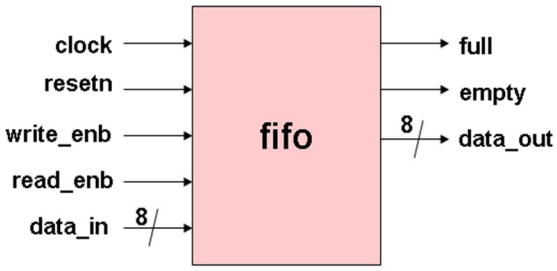


Figure 3 working of FIFO is based
on Write pointer

When write _enb is high then wr_ptr points to the write positions in the memory, automatically wr_ptr keeps on incrementing when data is being written into the write address in the memory. When read_enb is high, then data is being read from the fifo, then automatically rd_ptr keeps on incrementing when data is being read out from the fifo then rd_ptr keeps on decrementing, detain of fifo is exactly 8 bits and output of fifo is 8-bit output. For the efficient routing of the data the crossbar is modified with the 4 cross 1 and 8 cross 1 multiplexers.

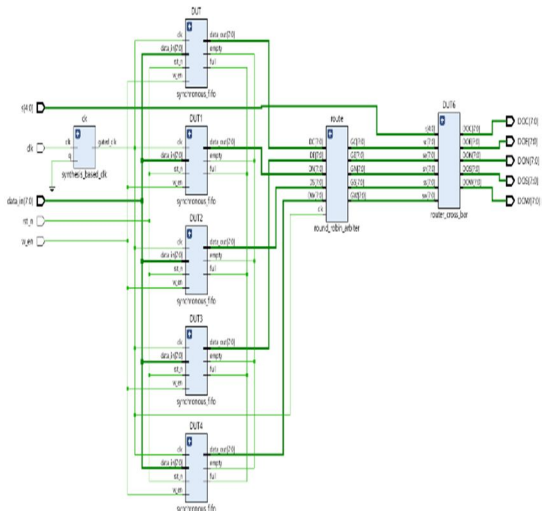


Figure 4 Schematic of new router design

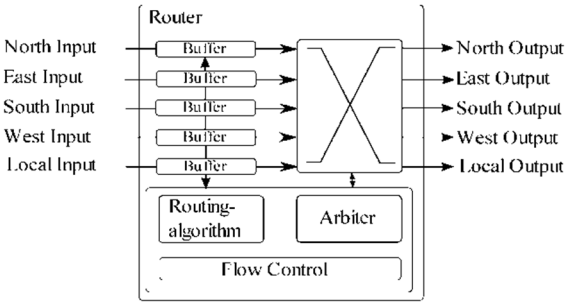


Figure 5 New router design

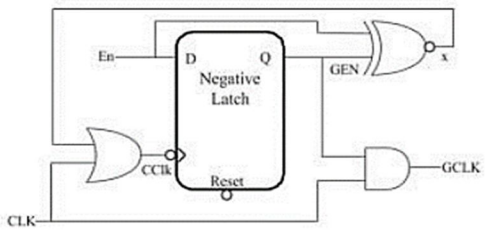


Figure 6 Synthesis based clock gating technique using negative latch

The design is modified with extra buffers at the output ports. The same is implemented in Xilinx and above figure represents the block diagram of new design. In the schematic, at the output ports the buffers can be observed. In computer architecture, clock gating is a popular power management technique used in many synchronous circuits for reducing dynamic power dissipation, by removing the clock signal when the circuit, or a subpart of it, is not in use or ignores clock signal. Clock gating saves power by pruning the clock tree, at the cost of adding more logic to a circuit. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not switch state, as switching the state consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. In the proposed method of VLSI Router for the Faster Data Transmission Using Buffer the overall power of the design will be reduced and the delay and area of the design also reduces slightly.

A. Clock Gating

Reduction in power dissipation is an essential design issue in VLSI circuit. Few decades back designers mostly focus on area, delay and testability to optimize.

While technology scaling down, we can see more power leakage and dissipation in chip. In order to reduce power dissipation and leakage power while scaling, we need to adopt the optimize techniques like clock gating. If operations are more and more complex then power dissipation is more. The clock network is a major source of power dissipation so we can reduce significant amount of power if we can gate the clock whenever it isn't required. In proposed work, we mainly focused on dynamic power dissipation and it reduced by making less signal activities in proposed design. The clock network is a major source of power dissipation so we can reduce significant amount of power if we can gate the clock whenever it isn't required.

B. Synthesis based clock gating technique

In this technique, gated clock can be generated by using either a positive or a negative latch with combination of AND or OR or EXOR or EXNOR logic gates shown in fig. Synthesis based clock gating technique using negative latch in synthesis-based clock gating using negative latch, we can observe when enable signal constant then x signal can be one and due to this controlled clock can be high so negative latch won't work and it gives previous value as output.

When enable signal changes then X value goes to zero value and controlled clock operated the negative latch circuit and it provides different value at the output side. Gated clock signal can be generated with AND gate of clock signal and output signal of negative latch

V. RESULTS

A. Simulation Results

1) Proposed VLSI Router using Buffer

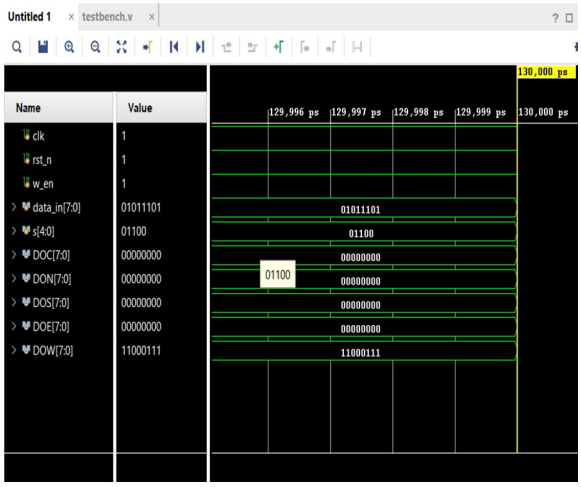
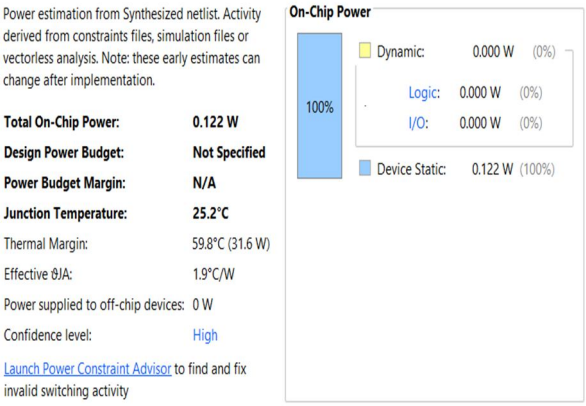


Figure 7 Simulation results for proposed VLSI Router buffer

This is the simulation results for the proposed VLSI Router.Based on the 5 input selection line the inputs are routed to the outputs.The inputs are SC,SN,SS,SE,SW and the outputs are DOC,DON,DOS,DOE,DOW.As it is a 5 input selection line if the selection line is 00100 the input SC is routed to DON.

2) Power Report



3) Area Report

Name	Bonded IOB (400)
TOP	40

4) Comparison table

	Power	**Area**
Existing	0.457	53
proposed	0.122	40

VI. CONCLUSION

The work focuses on optimizing the performance of VLSI based router architecture. From comparison table we can infer the comparison of the existing router model and the proposed router model. The proposed model increases the efficiency of data transmission by compared to the existing model. This is achieved by adding multiplexers in the crossbar at the output port and negative edge D latch. In proposed method of VLSI Router for the Faster Date Transmission using Buffer the power of the design was reduced by 0.122w and area, delay was also getting reduced.

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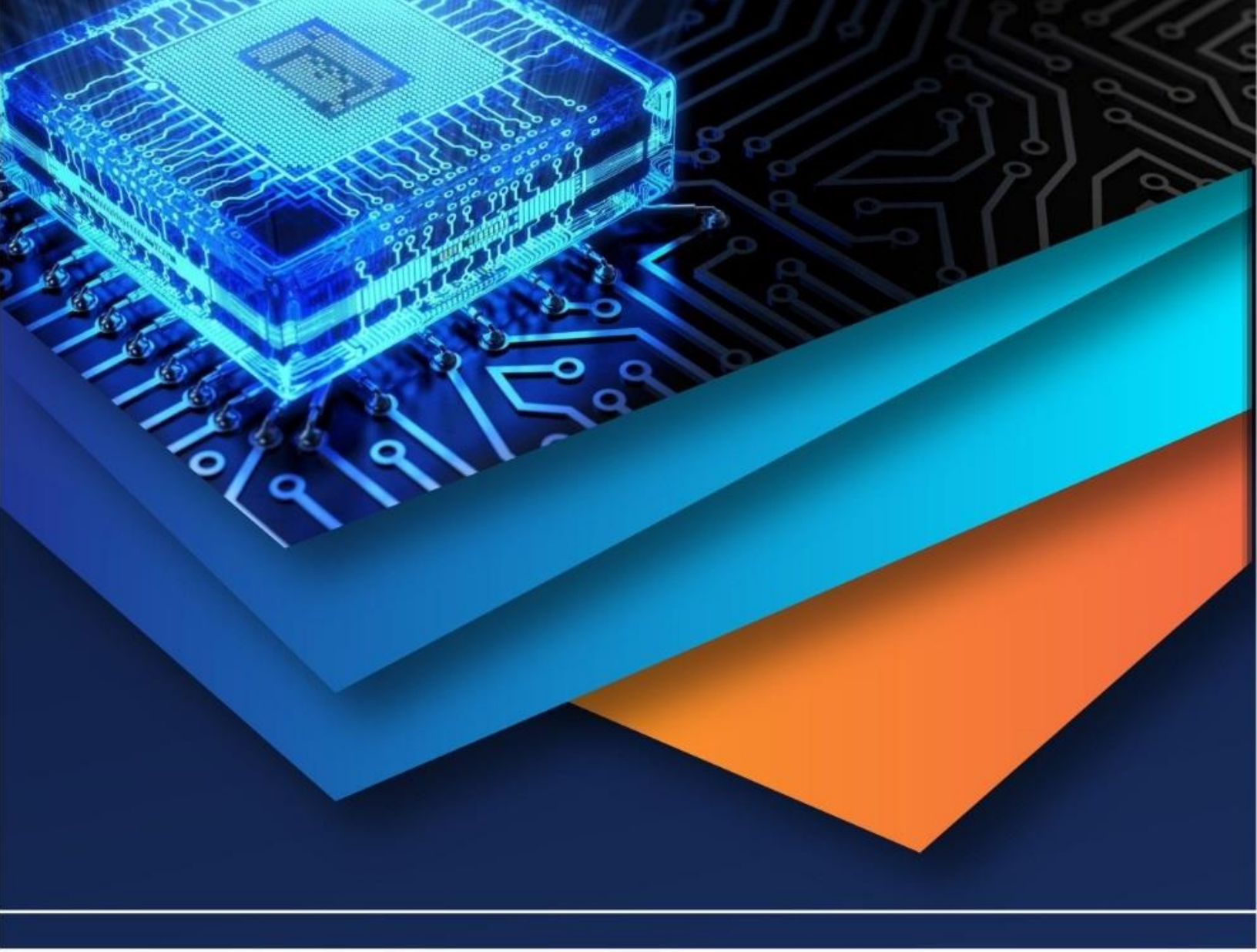

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