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Reduced Switches Count of Five Level H-bridge Inverter with Integrated Boost Converter in Solar PV System

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Abstract: ***PV systems are becoming more popular now a days, due to increase in the energy demand and it also reduces the environment pollution around the world. This paper proposes a reduced switches count of five-level H-bridge inverter with integrated boost converter in solar PV system. The proposed 5-level reduced switches count H-bridge MLI configuration requires less no.of power semiconductor devices compared to that of conventional MLI topology. In this paper INC MPPT control technique is used, which provides a duty ratio for controlling dc-dc boost converter and allowing the PV cells to operate more efficiently and extract maximum solar energy. The phase shifted sinusoidal pulse width modulation (PSCPWM) control technique is used for controlling the gating pulse of 5-level reduced switches H-bridge inverter. To improve the quality of PV based 5-level reduced switches h-bridge inverter output parameters mainly contribute switching losses and total harmonic distortion. The proposed model is modeled and simulated in MATLAB/SIMULINK software.***

Keywords: PV array, H-bridge multilevel inverter, boost converter, phase shifted PWM, maximum power point tracking (MPPT), incremental conductance, total harmonic distortion (THD).

I. INTRODUCTION

Now a day, photovoltaic energy is increasingly used because of its important benefits. In fact, this type energy ensures an electricity production without greenhouse gases emission. Besides, PV energy is totally flexible and can meet a wide range of needs [1-2].solar cells convert sunlight directly into electricity. They are made of semiconducting materials. A PV cell converts the solar energy into the electrical energy by the photovoltaic effect. When sunlight is absorbed by these materials, the solar energy knocks electrons loose from their atoms, allowing the electrons to flow through the material to produce electricity [3]. This process of converting light (photons) to electricity (voltage) is called PV effect. The size of a solar PV array, cells are stacked in a series–parallel configuration for required energy. PV array output voltage varies with change in irradiance and ambient conditions. Therefore, tracking the solar radiation is an important issue to increase efficiency of PV .An MPPT technique is used to extract maximum power available from the PV array under any operating conditions. Therefore, the maximum voltage from a PV array is produced using an MPPT control technique with a boost converter. Most important and famous MPPT methods are discussed by many researchers. Perturbations and observations (P&O) and incremental conductance [4].In solar PV power stations, a PV panel converts solar energy to DC electric power. This DC power is converted to the AC power by using inverter.

Multilevel inverters have gained much attention in recent years as power converters in many applications, such as utility and large motor drives. They are advantageous over the conventional two-level inverters because of their capability to reduce lower order harmonic contents by increasing the number of levels [5], [6], [7]. However, having high number of levels lead to complex control algorithm and introduces voltage imbalance problems.

Generalized structure of the multilevel inverters has been studied before [6]

The most attractive features of multilevel inverters are as follows:

1) They can generate output voltages with extremely low distortion.
2) They can operate with a lower switching frequency
3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings [5], [8].

Multilevel topologies are divided into three types, they are diode clamped, flying capacitor and cascaded H- bridge multilevel inverter.

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Among all these MLI cascaded H- bridge inverter requires less no.of power switching components and has a higher efficiency and has simple circuit layout. So, CHB MLI is suitable for PV panels but it requires more no.of PV panels in series or parallel connection when no.of levels increases. Therefore no.of switches increases when the level of inverter increases. The no.of switches in MLI defines cost, the size of the circuit, reliability and complexity. So the key element in designing MLI is the no.of switches required against the required voltage. To obtain the same output as in a 5-level CHB MLI, a new circuit design has been developed with reduced no.of switches without increasing the no.of H-bridges. The new 5-level CHB MLI is to contributes less numbers of power switching components and less switching and conduction losses and increases the inverter efficiency.

In this proposed model, we are employing a dc-dc boost converter which is regulating SPV array voltage and power according to INC (Incremental Conductance) MPPT (Maximum Power Point Tracking Algorithm) .The output power is fed to a 5-level reduced switch count h-bridge inverter, which is controlled using a phase shifted sinusoidal pulse width modulation (PSCPWM) control mechanism.

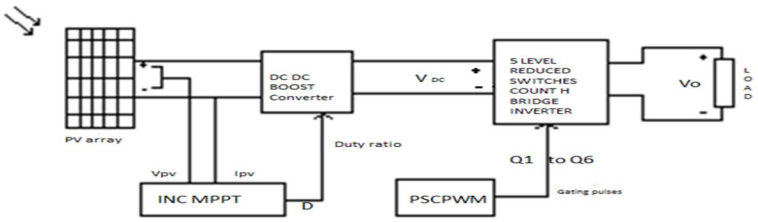


Fig.1. Proposed SPV fed 5-level RSMLI

II. PROPOSED SYSTEM CONFIGURATION AND DESIGN

The proposed reduced switch count five level H-bridge inverter with integrated boost converter in the solar PV system is shown in Fig.1. The PV array converts solar energy to electrical power and is regulated by a boost converter. The boost converter is controlled based on the *INC* MPPT algorithm. It generates a duty cycle (D). The boost converter is followed by a reduced switch count, 5-level H-bridge inverter. The phase shifted sinusoidal pulse width modulation (PSCPWM) control technique is used for controlling the gating pulse of the 5-level reduced switch h-bridge inverter.

A. PV array Design

PV modules are an extremely suitable DC source for the cascaded H-bridge MLI units. The single diode model of a solar cell is shown in fig. 2.The equations that represent PV model are well known as given in [9]. P-V and I-V characteristics of PV system as shown in fig.3

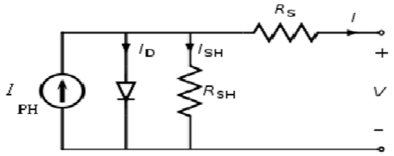


Fig.2. Single Diode Model of a Solar cell

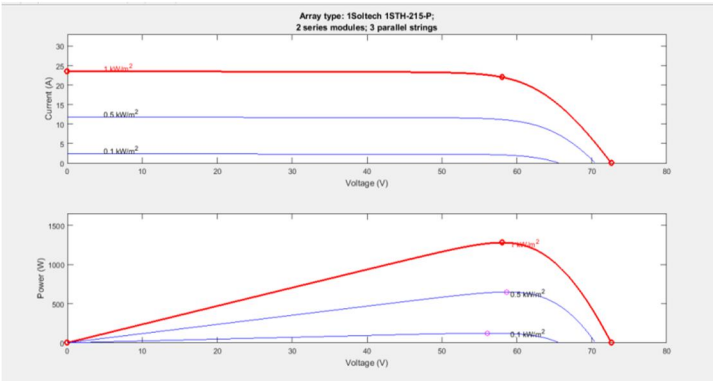


Fig.3. PV and IV Characteristics

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For designing SPV array systems, the 1SOLTECH 1STH-215-P PV module is employed. The SPV array module has two series modules and three parallel strings, resulting in a 72.6V open-circuit voltage (V_{oc}) and 23.52A short-circuit current (I_{sc}). At 80% V_{oc} and 93% I_{sc}, this SPV system reaches its maximum power point. Table.1 summarises the SPV module's specifications as shown in below.

Table.1. PV Module Design Parameters

	Single Module SPV Array	Complete SPV Array Module
Power at MPP(Pmp)	213.15W	1278.9W
Voltage at MPP(Vmp)	29V	58V
Current at MPP(Imp)	7.35A	22.05A
Open Circuit Voltage(Voc)	36.3V	72.6V
Short Circuit Current(Isc)	7.84A	23.52A
No.of Series Module(Ns)	2	
No.of Parallel Module(Np)	3	

B. Boost Converter Design

In PV applications, the DC-DC converter plays an important role. PV-generated DC voltage is insufficient to meet the load requirements. In these circumstances, a boost converter is employed to step up the voltage generated by the PV system. In this paper, a step up converter uses the INC MPPT algorithm to increase the voltage generated by a PV system, which is then applied to the input of a 5 level H-bridge inverter with reduced switches count. Circuit diagram of boost converter as shown in fig.4

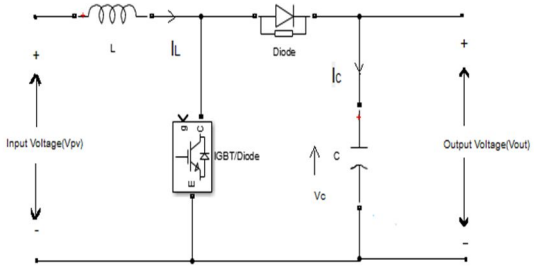


Fig.4. Boost Converter

This circuit has two modes of operation, which are determined by the duty cycle D of the switch ON and OFF times.

$$\text{Where, } D = \frac{Ton}{T}$$

$$T = Ton + Toff$$

The values of capacitor(C) and inductor (L) to be chosen by [10]

$$D = \frac{(v_0 - v_{mp})}{v_0}$$

$$L = \frac{v_{in} * D}{(\Delta_{i_L}) * f_s}$$

$$C = \frac{I_o * D}{\Delta v_0 * f_s}$$

Table.2. gives different parameter values of boost converter in RS 5-level h-bridge inverter configuration.

Table.2. Boost Converter Parameters

Parameters	Values
Switching frequency	6KHZ
Duty cycle	0.5

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C. Reduced Switches count 5-level H- Bridge Inverter

The reduced switches count 5-level h- bridge inverter circuit as shown in fig.5. The circuit consists of six switches (Q1, Q2, Q3, Q4, Q5, Q6) and two diodes (D1,D2). The circuit contains two conversion stages. The first stage produces two-level voltage with devices Q1, Q2 and diodes D1, D2, and the second stage produces three-level voltage with devicesQ1, Q2, Q3 and Q4 in an h-bridge model. The primary switching devices (IGBTs) may be switched on or off to provide five -level voltage at the inverter's output. The Inverter output voltage (Vo) is defined by the difference between V3 and V4. Table.3.gives the switching states and voltage levels of the five-level H-bridge inverter reduced switch count.

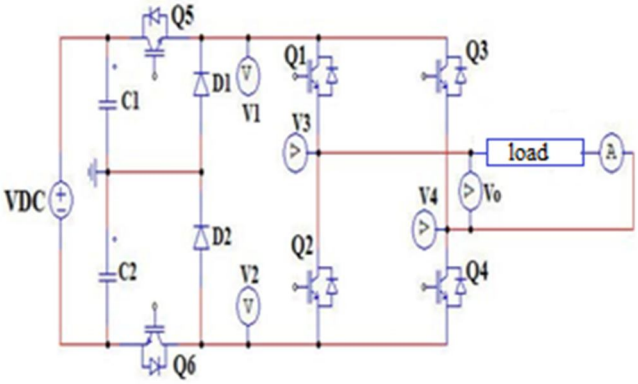


Fig.5. Reduced Switches Count 5-Level H-bridge Inverter

Table.3. Switching States And Voltage Levels

M	Main switching devices						Voltage levels				
	Q1	Q2	Q3	Q4	Q5	Q6	V1	V2	V3	V4	Vo
1	on	off	off	on	on	on	Vdc/2	-Vdc/2	Vdc/2	-Vdc/2	Vdc
2	off	on	on	off	on	on	Vdc/2	-Vdc/2	-Vdc/2	Vdc/2	-Vdc
3	on	off	on	off	*	*	0	0	0	0	0
4	off	on	off	on	*	*	0	0	0	0	0
5	on	off	off	on	on	off	Vdc/2	0	Vdc/2	0	Vdc/2
6	on	off	off	on	off	on	0	-Vdc/2	0	-Vdc/2	Vdc/2
7	off	on	on	off	on	off	Vdc/2	0	0	Vdc/2	-Vdc/2
8	off	on	on	off	off	on	0	-Vdc/2	-Vdc/2	0	-Vdc/2

M= modes and * indicates on or off

For table 3, the mode of operations is eight. There are, In mode 1, the switching devices Q1, Q4, Q5, and Q6 are in an on state. The output voltage Vo = Vdc is generated. In mode 2, the switching devices Q2, Q3, Q5 and Q6 are in an on state, the output voltage Vo = -Vdc is generated, In modes 3 & 4, only two switches i.e., Q1 and Q3 or Q2 and Q4 are in on state. The output voltage, Vo =0, In modes 5 & 6, only 3 switches i.e., Q1, Q4, Q5 or Q2, Q3, Q6 are in an on state, the output voltage Vo=Vdc/2 is generated. In modes 7 and 8, only 3 switches, i.e., Q2, Q3, Q5 or Q1, Q4, Q6 are in an on state. The output voltage Vo = -Vdc/2 is generated [11].

III. CONTROL TECHNIQUES FOR PROPOSED SYSTEM

The control techniques of the proposed system consist of two stages. They are the mppt stage and the modulation stage. For the first stage, the INC MPPT control technique is used, which provides a duty ratio for controlling the DC-DC boost converter and allows the PV cells to operate more efficiently and extract maximum solar energy. In the second stage, the phase-shifted sinusoidal pulse width modulation (PSCPWM) control technique is used to control the gating pulse of the 5-level reduced switch h-bridge inverter.

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A. Incremental conductance MPPT control method:

To determine the maximum power point, many methods were developed. They are different in their characteristics. Such as, sensors, cost, correct tracking, speed, accuracy. In this paper, the INC MPPT control technique is used and it provides better dynamic performance.in fig.3.,seems to be a bell-shaped curve, indicating that the slope of the curve is positive in the left hand, negative in the right hand, and maximum power is zero (dp/dv=0). The output power differs depending on the climate, but the voltage should stay constant throughout the operation. The flow chart of incremental conductance MPPT algorithm is shown in fig.6.

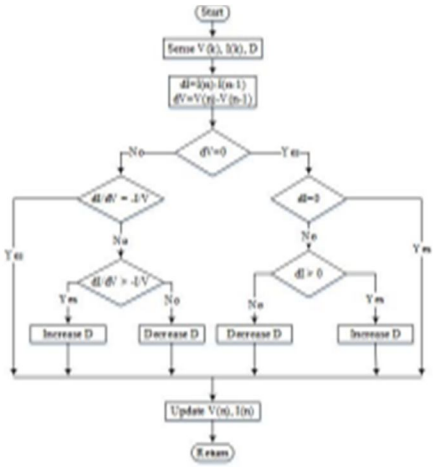


Fig.6.FlowChart of Incremental Conductance MPPT Algorithm

B. Phase Shifted Carrier pulse width Modulation (PSCPWM)

Different modulation techniques have to be suggested to control multilevel inverters. Basically there are classified into two types they are low switching frequency and high switching frequency pulse width modulation. Again high switching frequency pulse width modulation is classified into two types: space vector pwm and sinusoidal pwm. The sinusoidal pulse width modulation technique is broadly classified into: phase shifted modulation and level shift modulation.

In this paper, a phase shifted carrier pulse width modulation (PSCPWM) technique is used. PSCPWM has two types of signals: one is sinusoidal and other is a triangular signal. For the PSCPWM technique, a sinusoidal wave is the reference signal and a triangular wave is the carrier signal. The reference signal is identical and the carrier signals are slightly phase shifted. The usage of PSCPWM is a capability to improve the control performance. All carriers have the same frequency and same peak-peak amplitude and different phase angles. The results are merged into a single logical diagram. A MLI with 'L' voltage levels requires (L-1) triangular carriers. The proposed L=5 levels h-bridge MLI requires (L-1)= 4 carrier signals. The modulation index (M), given by

$$M = \frac{A_r}{A_C}$$

The phase shift between any two adjacent carrier signals, given by

$$\theta = \frac{360^0}{L-1}$$

Based on table 3, the gating patterns for the switches were generated by considering four cases. In four cases, Vcarrier1, Vcarrier2, Vcarrier3 and Vcarrier4 are denoted by Vc1, Vc2, Vc3 and Vc4 respectively [11].

First case: Gating pattern generation for first case is shown in below fig.7

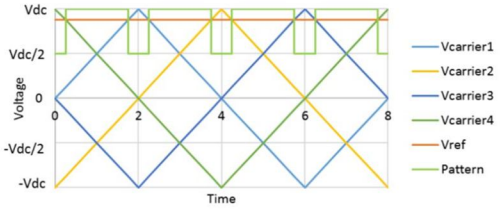


Fig.7. Gating Pattern Generation for First case

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For mode 1, gating logics are

$$y_1 = (Vdc/2 \leq Vref \leq Vdc) \wedge ((Vref \geq Vc1) \wedge (Vref \geq Vc2) \wedge (Vref \geq Vc3) \wedge (Vref \geq Vc4))$$

Mode 5 and 6 has two distinct states; gating logic in state (a) is as follows

$$y_{5a} = (Vdc/2 \leq Vref \leq Vdc) \wedge ((Vref < Vc1) \vee (Vref < Vc3))$$

$$y_{6a} = (Vdc/2 \leq Vref \leq Vdc) \wedge ((Vref < Vc2) \vee (Vref < Vc4))$$

Second case: Gating pattern generation for second case is shown in below fig.8.

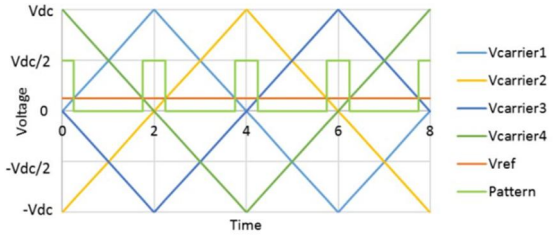


Fig.8. Gating Pattern Generation for Second case

For mode 5 and 6 has two distinct states, gating logic in state (b) as follows

$$y_{5b} = (0 \leq Vref < Vdc/2) \wedge ((Vref \geq Vc1) \wedge (Vref \geq Vc3))$$

$$y_{6b} = (0 \leq Vref < Vdc/2) \wedge ((Vref \geq Vc2) \wedge (Vref \geq Vc4))$$

For mode 3and 4 has two distinct states; gating logic in state (a) as follows

$$y_{3or4a} = (0 \leq Vref < Vdc/2) \wedge (((Vref < Vc1) \vee (Vref < Vc3)) \wedge ((Vref < Vc2) \vee (Vref < Vc4)))$$

Third case: Gating pattern generation for third case is shown in below fig.9.

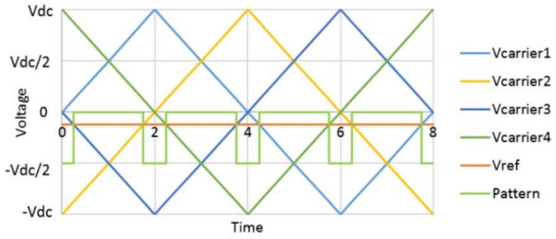


Fig.9. Gating Pattern Generation for Third case

For mode 3and 4 has two distinct states; gating logic in state (b) as follows

$$y_{3or4b} = (-Vdc/2 < Vref \leq 0) \wedge (((Vref > Vc1) \vee (Vref > Vc3)) \wedge ((Vref > Vc2) \vee (Vref > Vc4)))$$

For mode 7and 8 has two distinct states; gating logic in state (a) as follows

$$y_{7a} = (-Vdc/2 < Vref \leq 0) \wedge ((Vref \leq Vc1) \wedge (Vref \leq Vc3))$$

$$y_{8a} = (-Vdc/2 < Vref \leq 0) \wedge ((Vref \leq Vc2) \wedge (Vref \leq Vc4))$$

Fourth case: Gating pattern generation for third case is shown in below fig.10

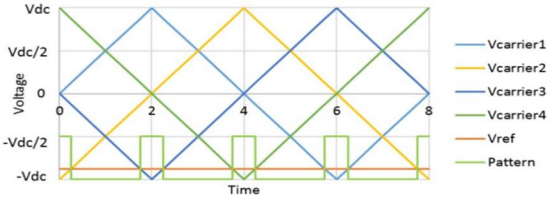


Fig.10. Gating Pattern Generation for fourth case

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For mode 7and 8 has two distinct states, gating logic in state (b) as follows

$$y_{7b} = (-Vdc \leq Vref \leq -Vdc/2) \wedge ((Vref > Vc1) \vee (Vref > Vc3))$$

$$y_{8b} = (-Vdc \leq Vref \leq Vdc/2) \wedge ((Vref > Vc2) \vee (Vref > Vc4))$$

For mode 2, gating logics are

$$y_2 = (-Vdc \leq Vref \leq -Vdc/2) \wedge ((Vref \leq Vc1) \wedge (Vref \leq Vc2) \wedge (Vref \leq Vc3) \wedge (Vref \leq Vc4))$$

Based on table 3, Logic circuits for each switch can be given as follows [11]

$$Q1 = y_1 \vee y_{3a} \vee y_{3b} \vee y_{5a} \vee y_{5b} \vee y_{6a} \vee y_{6b}$$
$$Q2 = \neg Q1$$
$$Q3 = y_2 \vee y_{3a} \vee y_{3b} \vee y_{7a} \vee y_{7b} \vee y_{8a} \vee y_{8b}$$
$$Q4 = \neg Q3$$
$$Q5 = y_1 \vee y_2 \vee y_{5a} \vee y_{5b} \vee y_{7a} \vee y_{7b}$$
$$Q6 = y_1 \vee y_2 \vee y_{6a} \vee y_{6b} \vee y_{8a} \vee y_{8b}$$

IV. SIMULATION RESULTS AND DISCUSSIONS FOR PROPOSED SYSTEM

The proposed reduced switch count five level H-bridge inverter with integrated boost converter in the solar PV system has been modelled and simulated in MATLAB/SIMULINK environment using simpower system toolbox. The multi carrier phase shifted pulse width modulation technique with sinusoidal reference is used to trigger the switches in reduced switches count five level H-bridge inverter. The circuit was simulated with load. Parameters of solar panel and boost converter are shown in table.1and 2.The proposed system is implemented in 1000w/m2 irradiance and 25degrees C temperature. Parameters of reduced switch count five-level H- bridge inverter as shown in below table.4.

Table.4. Simulation Parameters

PARAMETERS	VALUES
Switching frequency	6KHz
Output frequency	50Hz
Capacitor C1=C2	2200µF
Load	10Ω

PV array power, voltage, boost voltage and inverter output voltage values for different irradiations as shown in below table.

Table.5. Output Values for Different Irradiations

Irradiation	1000w/m^2	900w/m^2	800w/m^2	700w/m^2
PV power	950W	920W	898W	858W
PV voltage	64V	64V	63.9V	63.8V
Boost voltage	100V	100V	100V	100V
Inverter voltage(V_{peak})	100V	100V	100V	100V

The dc output voltage of PV module and DC-DC boost converter and ac output voltage and current of proposed model are given in fig.11, fig.12, fig.13, fig.14, fig.15 and fig.16 respectively. The total harmonic distortions for the output voltage with load are given in fig.17.

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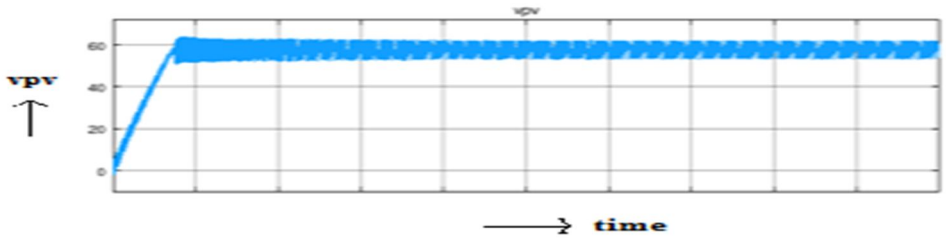


Fig.11. PV Array Output Voltage

In fig. 11 shows the output voltage of PV with irradiance 1000W/m2 and 25degrees temperature.

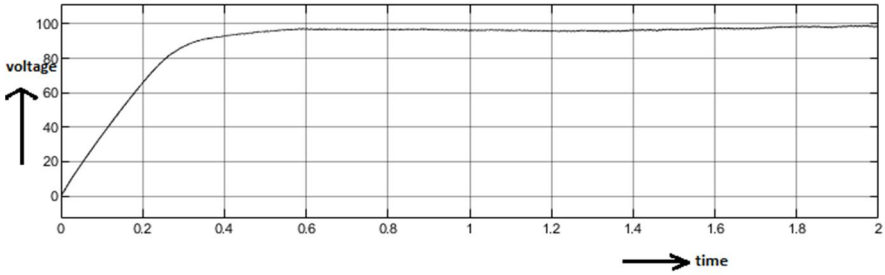


Fig.12. Boost Converter Output Voltage

In fig.12 shows the output voltage of DC-DC boost converter.

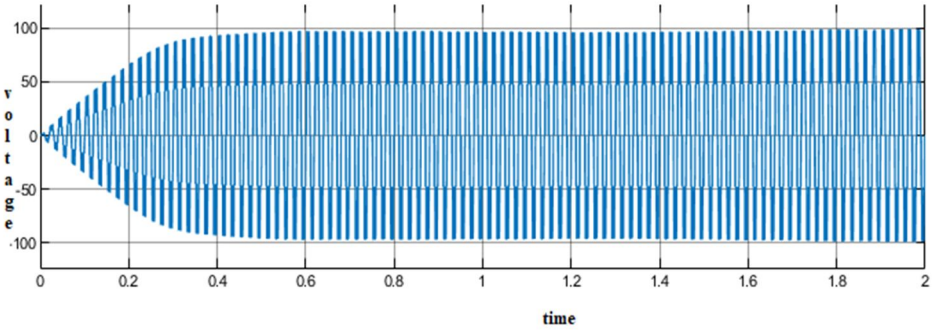


Fig.13. Output Voltage of Inverter

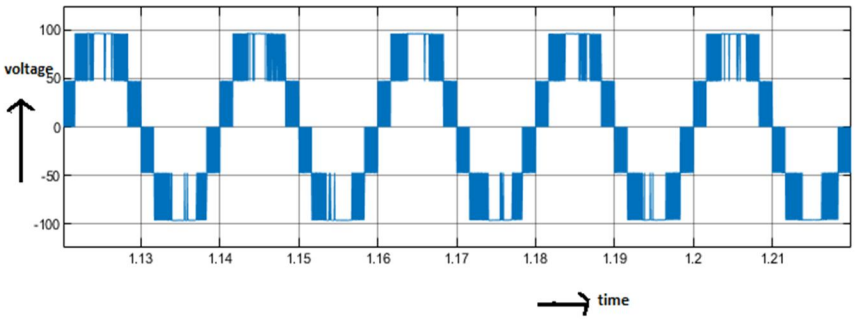


Fig.14. Magnified view of Output Voltage of Inverter

In fig.13 shows the output voltage waveform of a proposed system. The output voltage waveform has 5-levels for one cycle of 50HZ frequency can be observed. Which are -100,-50, 0, 50 and100.

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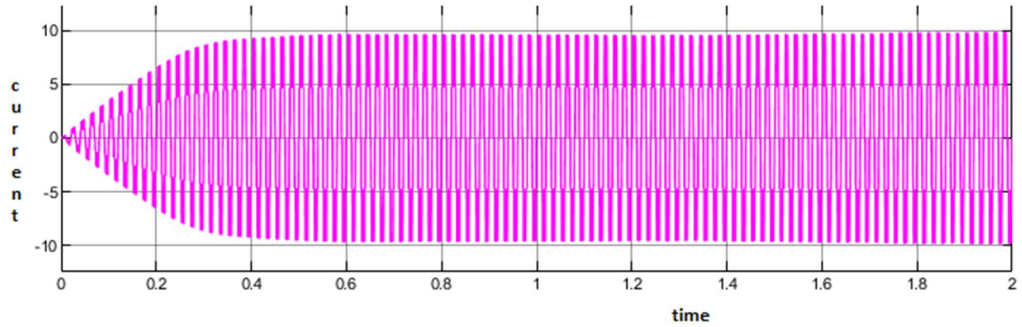


Fig.15. Output Current of Inverter

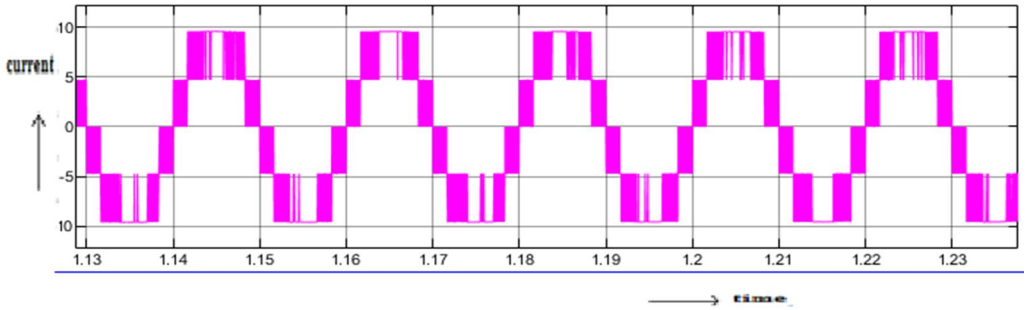


Fig.16. magnified view of Output Current of Inverter

In fig.15 shows the output current waveform of a proposed system. The output current waveform with peak amplitude of 9.98A

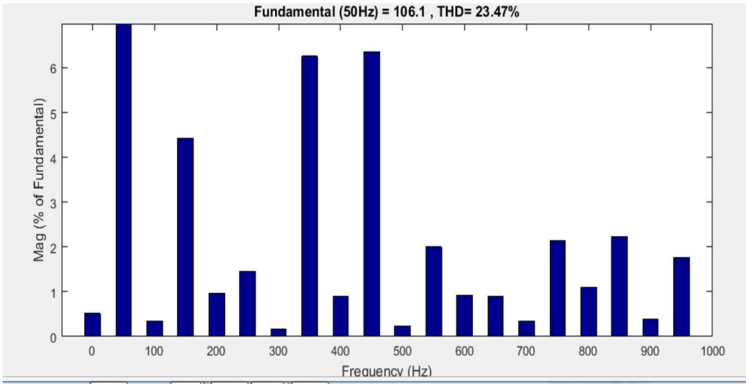


Fig.17. FFT analysis of output voltage

In fig.17 shows the total harmonic distortion (THD) for the output voltage of proposed model with load. To determine the THD present in a waveform, the line spectrum of the output voltage waveform is considered.
From the results the proposed system gives reduced THD. As the no.of power switches are reduced power losses and conduction and switching losses will also be reduced.

V. CONCLUSION

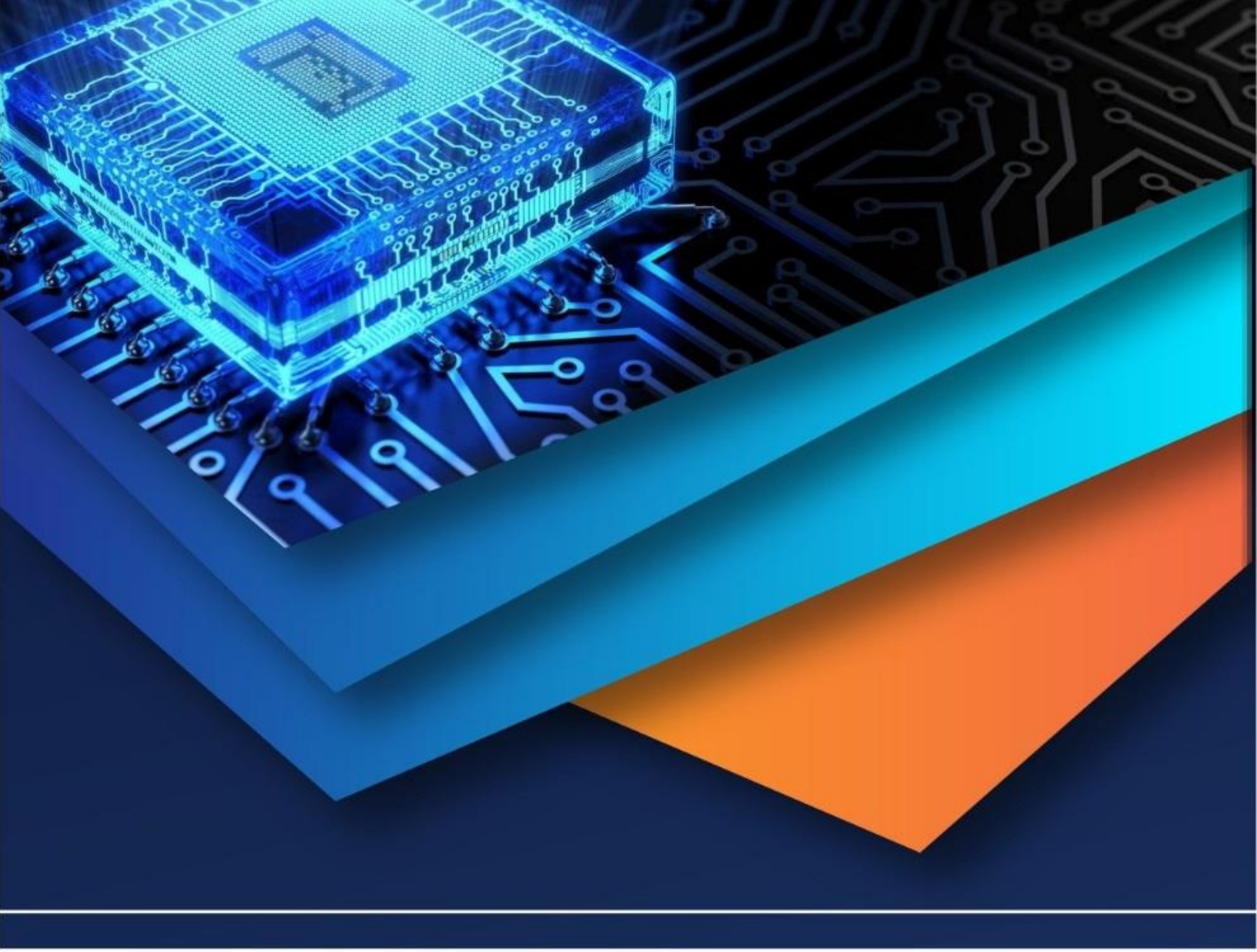
In this paper, the proposed reduced switch count five level H-bridge inverter with integrated boost converter in the solar PV system has been modelled and simulated in MATLAB/SIMULINK software. The reduced switches count 5-level H-bridge inverter is connected from one independent solar panel with INC MPPT algorithm instead of Dc source through boost converter. The most important features of proposed system is increasing the no.of output levels with reduced no.of switches and thereby, decreasing the size, complexity, cost, switching and conduction losses and power losses. The proposed model shown to be the one of the best in terms of efficiency and lesser percentage of voltage THD, Simulation results allow us to conclude that the proposed model offers better performance. Hence the proposed system is suitable for PV applications.

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[4] Vol. 5, Issue 3, March 2016 Copyright to IJAREEIE DOI:10.15662/IJAREEIE.2015.0503112 1694 Analysis of Different MPPT Techniques Athira B1 ,. Greeshma V2 . Jeena Johnson3 Assistant Professor, Dept. of EEE, Sree Buddha College of Engineering for Women, Pathanamthitta, Kerala, India1 U.G Student, Dept. of EEE, Sree Buddha College of Engineering for Women, Pathanamthitta, Kerala, India2 U.G Student, Dept. of EEE, Sree Buddha College of Engineering for Women, Pathanamthitta, Kerala, India
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[18] International Journal of Advance Engineering and Research Development Volume 4, Issue 4, April -2017 @IJAERD-2017, All rights Reserved 943 Scientific Journal of Impact Factor (SJIF): 4.72 e-ISSN (O): 2348-4470 p-ISSN (P): 2348-6406 Analysis and Comparison of PD, POD, APOD PWM Techniques For Symmetrical Multilevel Inverter Bhavana Radadiya1, Meeta Mantani2, Tapankumar Trivedi3 1, 2, 3Marwadi Education Foundation's Group of Institutions, Rajkot, India.
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