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Signoff-Driven Floorplanning Under Foundry and Technology Constraints for Multi-Voltage-Domain SoC Designs

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Abstract: ***Advanced system-on-chip (SoC) designs increasingly rely on multi-voltage domains, aggressive power-performance-area-cost (PPAC) targets, and stringent foundry signoff requirements. At advanced technology nodes, late-stage design rule check (DRC), layout versus schematic (LVS), IR-drop, and electromigration (EM) violations frequently trigger expensive engineering change orders (ECOs), impacting time-to-market. Traditional physical design flows treat signoff as a post-routing activity, leading to poor convergence and closure. This paper presents a signoff-driven physical design methodology that integrates foundry and technology constraints directly into floorplanning, placement, clock tree synthesis (CTS), and routing for multi-voltage-domain SoC designs. Mathematical cost models, early power distribution network (PDN) estimation, voltage-island-aware placement, and ECO-aware routing strategies are introduced. The proposed methodology significantly reduces late signoff iterations and improves first-pass silicon success.***

Index Terms: ***ASIC physical design, signoff-driven design, floorplanning, voltage islands, IR-drop, DRC/LVS, CTS.***

I. INTRODUCTION

Technology scaling has enabled highly integrated SoCs containing CPUs, GPUs, AI accelerators, memories, and high-speed interfaces on a single die. To meet aggressive power budgets, modern SoCs employ multiple voltage domains, power gating, and fine-grained clock control. While these techniques reduce power consumption, they dramatically increase physical design complexity.

At advanced nodes, foundry signoff decks include thousands of design rules related to spacing, density, antenna effects, EM, and reliability. When these constraints are addressed only after routing, designers often face late-stage signoff failures, triggering ECO explosions. This paper argues that signoff awareness must begin at the floorplanning stage and propagate throughout placement, CTS, and routing.

This work contributes:

1) A signoff-driven floorplanning cost model incorporating timing, IR-drop, congestion, DRC density, and voltage-island constraints.
2) Unified methodology for voltage-island-aware placement and level-shifter planning.
3) Early PDN and IR-drop estimation tightly coupled with placement decisions.
4) A routing and CTS strategy designed to minimize late-stage signoff ECOs.

II. BACKGROUND AND RELATED WORK

A. Traditional Floorplanning and Placement

Classical floorplanning research focused on minimizing area and wirelength using slicing and non-slicing floorplans. Placement algorithms further optimized standard-cell locations to reduce timing and congestion. These methods assumed relatively relaxed design rules and homogeneous power domains.

B. Voltage Island Floorplanning

Voltage-island-driven floorplanning has been studied to minimize level-shifter overhead and inter-domain communication. Graph partitioning techniques are commonly used to cluster blocks operating at similar voltages. However, most prior work does not explicitly integrate foundry signoff constraints.

C. Power Integrity and PDN Modeling

IR-drop and EM analysis traditionally occurs after routing using detailed extraction. Early PDN estimation methods have been proposed, but are often disconnected from placement optimization.

D. Signoff Verification EvolutionModern signoff tools

Support incremental DRC/LVS, warm-start analysis, and limited machine-learning acceleration. Despite these improvements, late-stage signoff failures remain a major bottleneck.

Gap: Existing approaches address individual challenges but lack a unified, signoff-driven physical design methodology.

III. TECHNOLOGY AND FOUNDRY CONSTRAINTS AT ADVANCED MANUFACTURING PROCESSES

At advanced processes, physical design is no longer an exercise in optimizing wirelength and timing alone. Instead, it is constrained by:

A. Geometric Design Rules

Advanced nodes exhibit:

1) Restricted routing directions
2) Tight pitch quantization
3) Limited via configurations
4) Minimum pattern density requirements

These rules are driven by advanced lithography and patterning techniques.

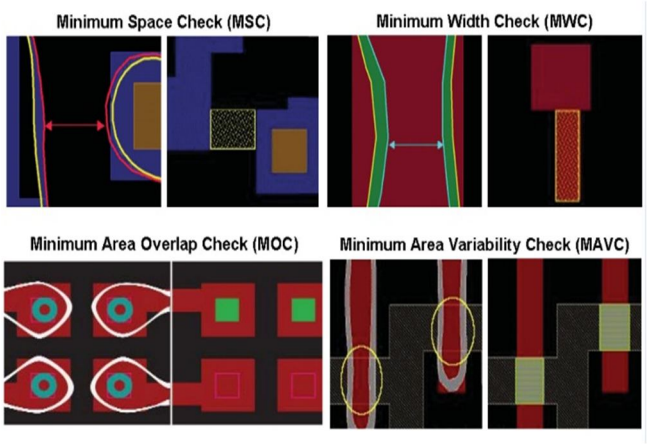

Fig. 1 Manufacturing Constraints

B. Patterning and Lithography Constraints

Multiple patterning introduces:

1) Color-aware routing
2) Decomposition constraints
3) Forbidden pitch combinations

Physical design tools must enforce color-safe placement and routing to ensure manufacturability.

C. Device-Level Constraints

Transistor architectures impose:

1) Fixed fin or channel quantization
2) Discrete gate widths
3) Restricted transistor orientations

Cell architectures are therefore highly constrained, reducing placement flexibility.

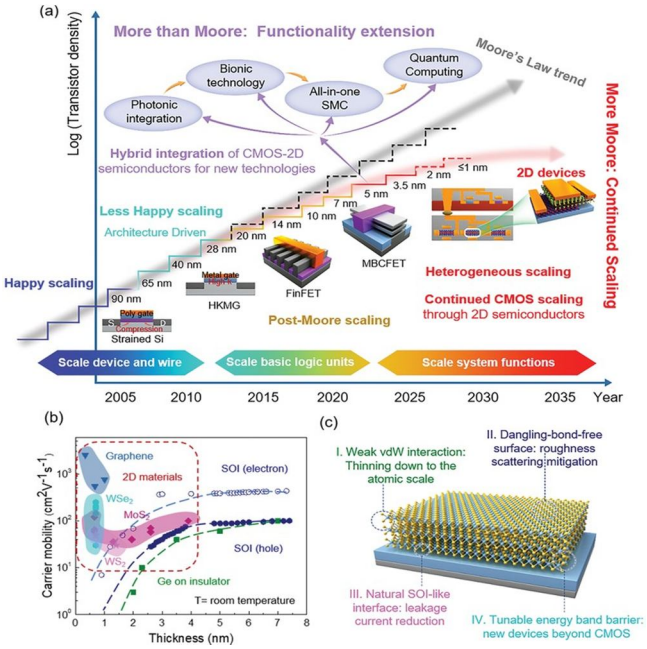

Fig. 2 Scaling Challenges

IV. MULTI-VOLTAGE-DOMAIN SOC DESIGN FUNDAMENTALS

A power domain is a logical and physical partition of the design supplied by a dedicated power net (VDD) and ground (VSS). Each domain may operate at a distinct nominal voltage and may support multiple operating modes, such as active, idle, retention, and power-off. A voltage island refers to the physical realization of such a domain on silicon, often bounded by power grid segmentation and well isolation.

Power domains are typically classified as:

1) *Always-on domains:* Control logic, wake-up controllers, and state retention logic.
2) *Switchable domains:* Performance or accelerator blocks that can be fully powered down.
3) *Retention domains:* Blocks that preserve architectural state at reduced voltage during sleep modes.

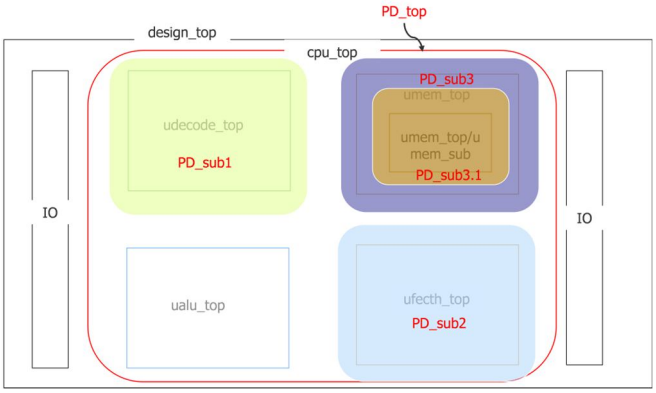

Fig. 3 Power Domain Partitioning

Careful partitioning is required to minimize inter-domain crossings, as these introduce additional cells, routing congestion, and verification complexity.

Signal integrity and functional correctness across voltage domains are ensured through specialized interface cells:

- *Level shifters (LS):* Translate signal voltage levels between higher and lower voltage domains.
- *Isolation cells (ISO):* Prevent unknown (X) propagation from powered-down domains.
- *Retention registers (RET):* Preserve state during low-power or power-off modes.

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V. FLOORPLANNING STRATEGIES FOR MULTI-VOLTAGE DOMAINS

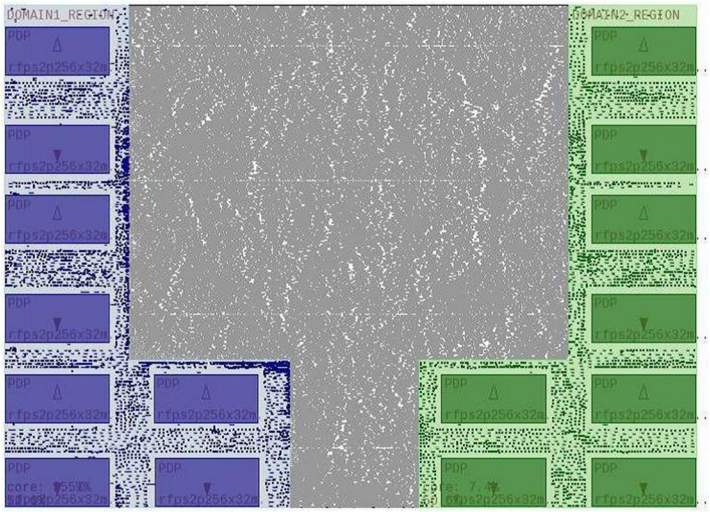

Fig. 4 MSV Floorplan

A. *Power-Grid-Centric Floorplanning*

1) *Early Power Grid Definition:* Power-grid topology is defined during floorplanning, including mesh pitch, strap width, and via strategy. Domain-specific grids are tailored to current demand and noise sensitivity.
2) *Voltage Domain Isolation:* Physical separation and controlled inter-domain connections reduce noise coupling and improve reliability.

B. *Voltage-Island-Aware Macro Placement*

Macros are clustered based on voltage domain, switching activity, and current demand. High-current macros are positioned near package power entry points, while noise-sensitive blocks are isolated from aggressive switching regions.

C. *Level Shifter and Isolation-Aware Floorplanning*

Level shifters (LS) are mandatory for signals crossing voltage domains. Best Practices are placing LS close to receiving domain, Cluster LS in dedicated boundary regions and avoid dispersing LS within standard-cell rows

D. *Isolation Cell Planning*

Isolation cells must: Be placed in always-on regions, be reachable by isolation control signals, Remain powered during domain shutdown. Failure to plan isolation placement early often results in late-stage ECOs.

VI. SIGNOFF STRATEGIES FOR FLOORPLANNING

A. *IR-Drop Budgets*

Each voltage domain is assigned a maximum allowable voltage drop:

$$\Delta V_{max} = V_{nominal} \times \alpha$$

where α\alphaα is typically much smaller for low-voltage or timing-critical domains.

Implications:
High-performance domains require denser power grids
Low-power domains have tighter absolute voltage margins
Shared grids across domains are often prohibited.

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B. Electromigration (EM) Constraints

Technology scaling significantly increases current density, making EM a first-order constraint.

Foundries specify

Maximum DC and RMS current density
Via redundancy requirements
Temperature-dependent derating factors

In multi-voltage-domain SoCs

High-voltage or high-activity domains dominate EM stress
Power switches and level shifters become EM hotspots
Floorplans must minimize long, high-current power paths.

C. Manufacturability and Yield Constraints

1) *Density and CMP Requirements:* Foundries enforce metal and cell density constraints to ensure uniform planarization. Multi-voltage-domain designs complicate this due to: Uneven logic density across domains, Large always-on or retention regions & Power-grid density variations. This requires domain-aware filler and decap planning at floorplan time.
2) *Pattern Matching and Regularity: Advanced manufacturing favors highly regular layouts. Irregular voltage island shapes increase:*
3) Pattern-matching violations, Yield loss, Mask complexity
4) *As a result, voltage domains should be:* Rectangular or smoothly contoured, aligned to routing grids Avoid excessive fragmentation.

VII. MACRO PLACEMENT CONSTRAINTS UNDER FOUNDRY RULES

A. High-Current Macro Localization

Foundry EM rules restrict Maximum current per metal segment and Maximum distance between straps
Therefore, High-current macros must be clustered,
Long power routes across domains are prohibited, Macros cannot be arbitrarily placed for timing alone.
This transforms macro placement into a power-integrity-constrained optimization.

B. Macro-to-Domain Compatibility

Macros are often characterized for Specific voltage ranges, Specific power-grid assumptions.
Placing a macro across or near incompatible domains can violate Reliability rules, DRC spacing constraints, Power-switch insertion rules.
Thus, macro-domain compatibility becomes a hard floorplanning constraint.

VIII.ROUTING CONSTRAINTS THAT SHAPE FLOORPLANNING

A. Routing Resource Reduction

Technology scaling reduces effective routing capacity due to: Wider power straps, increased spacing rules, more routing layers dedicated to power.
In multi-voltage designs, duplicated power grids further consume routing resources, forcing floorplanning to reserve routing channels explicitly.

B. Channel Width and Inter-Block Spacing Constraints

Routing channels are the lifelines of a floorplan.
Channel width must account for Estimated net count, Metal layer availability and Power strap interference.
Underestimated channel widths are a primary cause of Global routing overflow, Track starvation, Detoured critical nets.
Preferred routing directions impose Horizontal congestion in some regions & Vertical congestion in others. So, floorplans must orient blocks and channels to align with routing directionality, rather than against it.

C. Routing Constraints from Clock Networks

Clock routing is often the single largest consumer of routing resources. Clock Trunk require wide, low-resistance routes, Symmetric topology, and Minimal interference from signal routing. Floorplanning must pre-reserve central routing corridors and symmetric block placement.

Multiple clock domains create Clock crossing logic, Additional routing demand, and Placement restrictions. Poor floorplanning leads to clock congestion that cannot be resolved later.

D. Global Routing–Aware Floorplanning

Modern flows incorporate early global routing during floorplanning. Early Congestion Estimation provides congestion heatmaps, overflow prediction and channel adequacy assessment.

Iterative Floorplan Refinement based on routing feedback can be macros are shifted, channels are widened and domain boundaries are reshaped. This loop continues until routing feasibility is proven.

IX. ECO-AWARE FLOORPLANNING

1) Buffer Insertion Capacity: Setup ECOs require Space for buffers, clean routing paths, and Low coupling environment.
2) Hold-Fix Explosion Mitigation: Hold fixes multiply rapidly at advanced nodes. Floorplanning should avoid over-short paths, prevent over-clustering of fast logic, and provide routing slack for detours.
3) Cross-Domain ECO Restrictions: Cannot freely add logic across domains, level shifter availability becomes critical and Isolation logic complicates fixes.

X. CONCLUSION

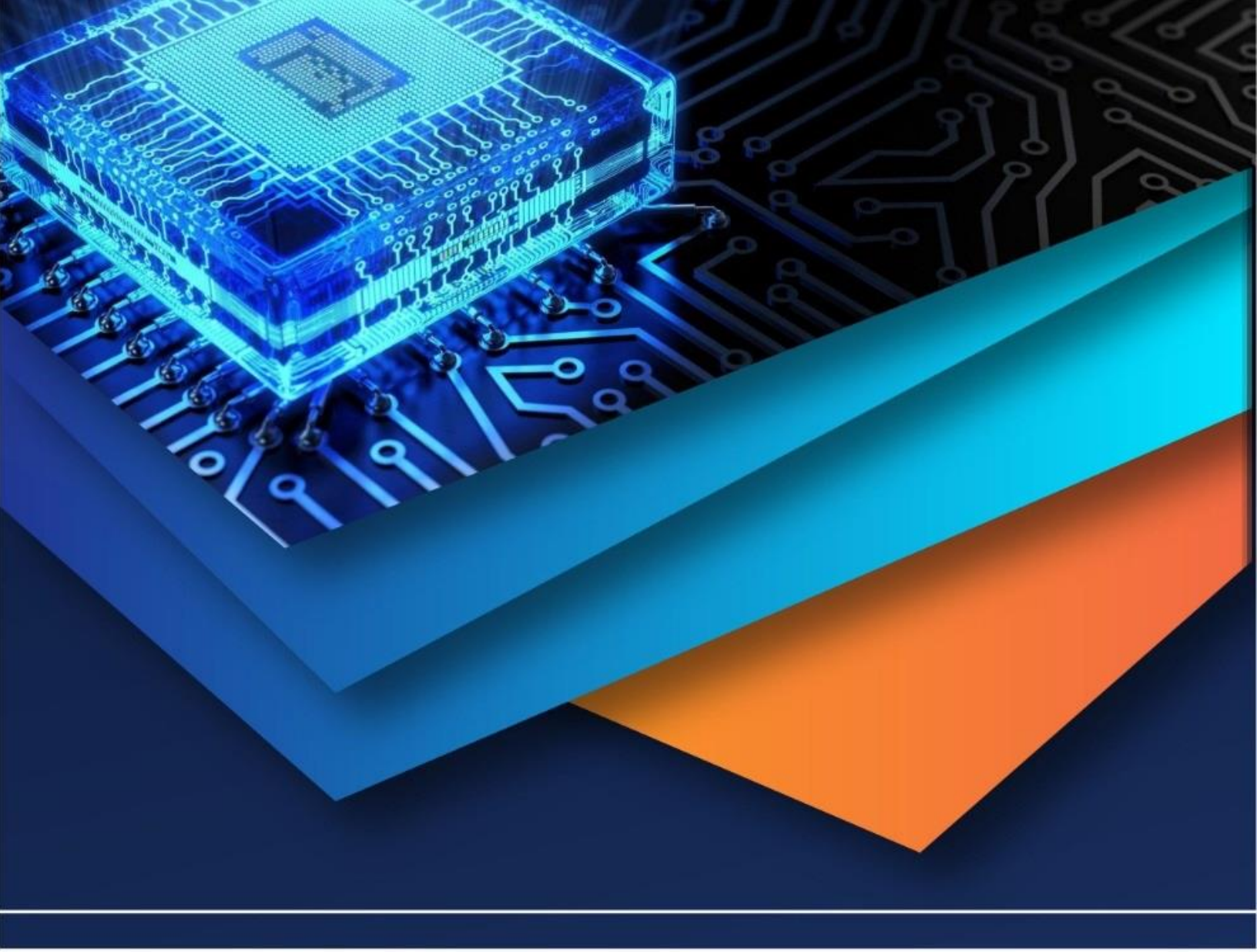
This paper presented a signoff-driven floorplanning methodology for multi-voltage-domain (MVD) SoC designs under stringent foundry and advanced technology constraints. As semiconductor technologies scale into deeply advanced nodes, the interaction between physical layout decisions, manufacturing rules, and signoff requirements has become increasingly complex. Conventional floorplanning approaches, which primarily optimize for area and performance, are insufficient to address the compounded challenges of timing closure, power integrity, routability, and manufacturability in MVD designs.

The analysis further demonstrates that floorplanning serves as the primary control point for downstream placement, CTS, and routing quality, especially in MVD SoCs where cross-domain interactions dominate physical design complexity. Early awareness of routing congestion, EM/IR margins, and timing criticality enables more balanced trade-offs between performance, power, and area while maintaining compliance with foundry signoff requirements. As a result, signoff-driven floorplanning improves implementation predictability, enhances first-pass silicon success, and shortens overall design cycles.

In conclusion, signoff-driven floorplanning is no longer optional but a fundamental requirement for successful MVD SoC implementation at advanced technology nodes. Integrating foundry and technology constraints at the floorplanning stage establishes a robust foundation for downstream physical design stages and mitigates the risk of costly late-stage fixes. Future research directions include the integration of AI-assisted prediction models, adaptive floorplan refinement loops, and cross-domain optimization frameworks to further improve signoff robustness and scalability for next-generation SoC designs.

REFERENCES

[1] J. Cong, M. Xie, and Y. Zhang, “Thermal-aware floorplanning for multi-core SoC designs,” IEEE Trans. Computer-Aided Design Integr. Circuits Syst., vol. 31, no. 10, pp. 1525–1538, Oct. 2012.
[2] D. Sylvester, K. Keutzer, and C. Hu, “IR drop in advanced VLSI design,” IEEE Design & Test of Computers, vol. 21, no. 6, pp. 418–425, Nov.–Dec. 2004
[3] S. R. Nassif, “Power grid analysis benchmarks,” in Proc. IEEE Int. Symp. Quality Electronic Design (ISQED), 2008, pp. 376–381.
[4] A. B. Kahng, S. Kang, R. Kumar, and J. Sartori, “Designing a physical design flow for advanced technology nodes,” IEEE Trans. Computer-Aided Design Integr. Circuits Syst., vol. 36, no. 8, pp. 1259–1272, Aug. 2017.
[5] P. Saxena et al., “multi-voltage and power-gated SoC physical design challenges,” in Proc. IEEE Custom Integrated Circuits Conf. (CICC), 2015, pp. 1–8.
[6] M. Cho, D. Z. Pan, and R. Puri, “Power-aware physical design for multi-voltage designs,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 5, pp. 845–858, May 2012.
[7] A. B. Kahng and Q. Wang, “Challenges and opportunities in DFM-aware physical design,” IEEE Design & Test, vol. 34, no. 4, pp. 6–15, Aug. 2017.
[8] C. Visweswariah et al., “Signoff closure challenges at advanced nodes,” in Proc. IEEE Design Automation Conf. (DAC), 2018, pp. 1–6.
[9] S. Hu et al., “Routing congestion prediction and mitigation in advanced technology nodes,” IEEE Trans. Computer-Aided Design Integr. Circuits Syst., vol. 39, no. 11, pp. 3958–3970, Nov. 2020.
[10] K. Bernstein et al., “High-performance CMOS variability in the 65-nm regime and beyond,” IBM J. Res. Develop., vol. 50, no. 4–5, pp. 433–449, Jul.–Sep. 2006.



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