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Simulation of Asymmetrical Seven Level Multi Level Inverter using MATLAB Simulink

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Abstract: ***Multi-Level Inverter (MLI) has gained significant significance in medium power and medium voltage AC drive applications. Various topologies have been developed in the design of MLIs. Hybrid topologies are emerging to minimize component requirements and reduce switching losses. This paper introduces a comprehensive analysis and functioning of the asymmetrical seven level multi-level inverter topology. The modeling process is executed using the MATLAB Simulink environment.***

I. INTRODUCTION

Due to their drawbacks such as the need for more switching elements, additional switching losses, bulky driver circuit requirements and high dv/dt problems, conventional two-level inverters are becoming outdated in industrial drive applications[1]. To address these challenges, multi-level inverters have emerged with different topologies. The traditional topologies include diode clamped, flying capacitor, and cascaded H-bridge configurations [2-5].

Among these, diode clamped and cascaded H-bridge topologies have gained prominence in various applications [6-8]. The diode clamped topology requires only one DC source, enabling different voltage levels by connecting capacitors in series. However, this approach presents a voltage balancing problem. In contrast, the cascaded topology requires several DC sources, reducing design complexity [9-10]. The flying capacitortopology faces drawbacks related to voltage balancing and control circuit complexity. Consequently, researchers have explored various combinations of these basic topologies, leading to the emergence of cascaded H-Bridge topologies as a potential solution [11-14].

The symmetrical seven level multi-level inverter requires three voltage sources of equal magnitude and 12 switching devices per phase. In case of asymmetrical seven level MLI requires only two voltage sources of different values and requires 8 switches. Hence the efficiency of asymmetrical MLI is more than symmetrical MLI.

II. STRUCTURE OF ASYMMETRICAL SEVEN LEVEL CASCADED MLI

Asymmetrical topologies are the latest structures, where the cascaded series inverters have distinct internal dc voltage sources, uses less switching devices. The significant feature of the proposed multilevel inverter topology is the reduction of switches and consequently minimizing the switching losses.

The three phase circuit structure is represented in the figure 1. The circuit in figure 2 is the standard single phase asymmetrical seven level MLI representation. The neutral point is taken from the bottom inverter. There are seven switch combinations to produce seven-level voltages across the load.

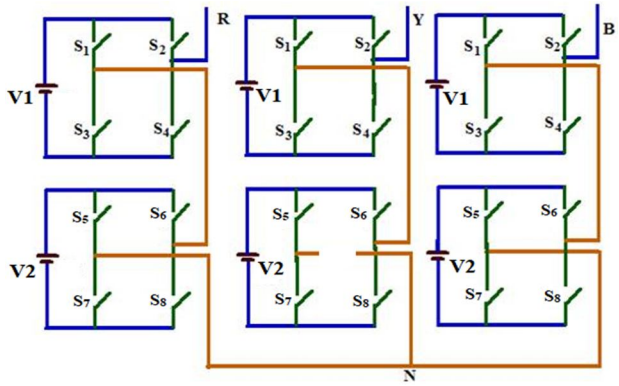


Fig.1 Three phase circuit structure of asymmetrical seven levelmli

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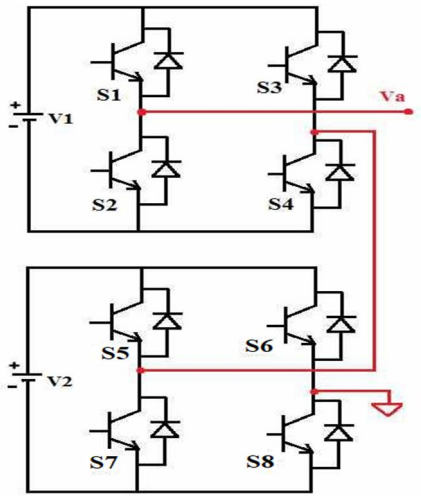


Fig.2 Single phase circuit of asymmetrical seven level MLI

The clear demonstration of the sequence of switch operations to achieve varying voltage levels is depicted from figure 3 to figure 9. Here the V1 is equal to V and The clear demonstration of the sequence of switch operations to achieve seven voltage levels isdepicted from figure 3 to figure 9. Here the V1 is equal to V and V2 is equal to 2V. The seven voltagelevels are 3V, 2V, V, 0, -V, -2V, -3V. For different voltage levels different switches will be operated to get the desired output voltageFor the voltage level 3V the switches S1, S4, S5&S8 will be in ON state and remaining switches will bein OFF state. Both voltage sources V1, V2 will be in ON state it can be clearly observed from thefigure 3.

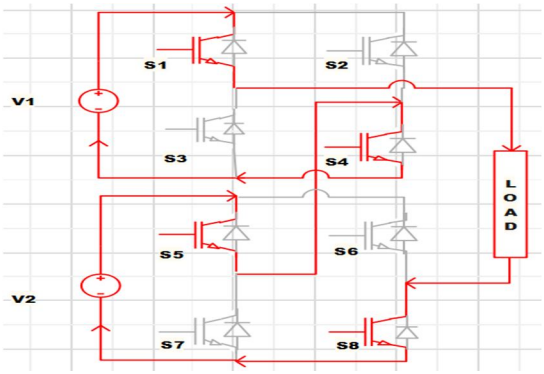


Fig.3 operation of the circuit to generate the output voltageas 3V

To get output voltage of 2V,then the switches S3, S4, S5 & S8 will be ON and remaining will be in OFF state and voltage source is V2 is connected to the load and the voltage source V1 is disconnected from the circuit, which can be observed from the figure 4.

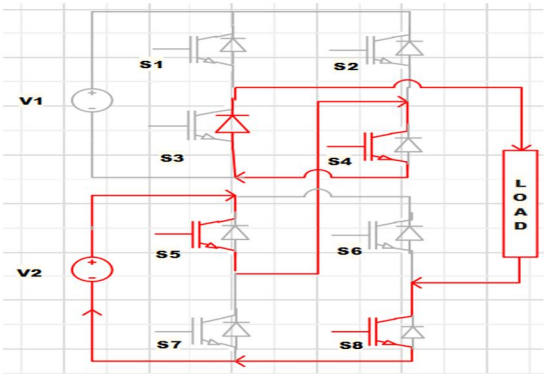


Fig.4 operation of the circuit to generate the output voltage as 2V

To get the output voltage as V, the switches S1, S4, S7& S8 are in the ON state and remaining all will be OFF state and the voltage sourceV1 is connected to the load and V2 is disconnected for this state, which can be clearly observed form the figure.5.

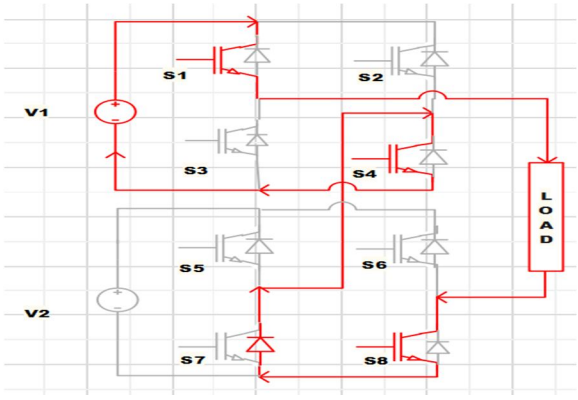


Fig.5 operation of the circuit to generate the output voltage as V

To get the voltage output as 0V, for his state the switches S3, S4, S7 & S8 are in operation and remaining will be in OFF state, In this state both voltage sources are disconnected from the load. In this state it provides the short circuit path, which can be observed from the figure 6.

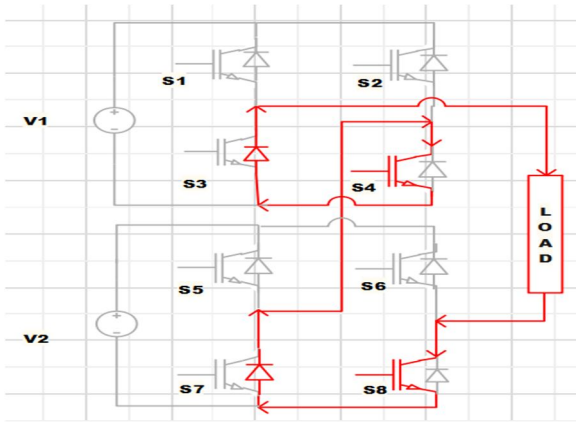


Fig.6 operation of the circuit to generate the output voltage as 0V

For to get the output voltage as -V, the switches S2, S3, S7 & S8 are in ON state and remaining will be in OFF state and the voltage source V1 is will be connected to the load in opposite direction to the previous one so it is denoted with the negative symbol which can be observed from the figure 7.

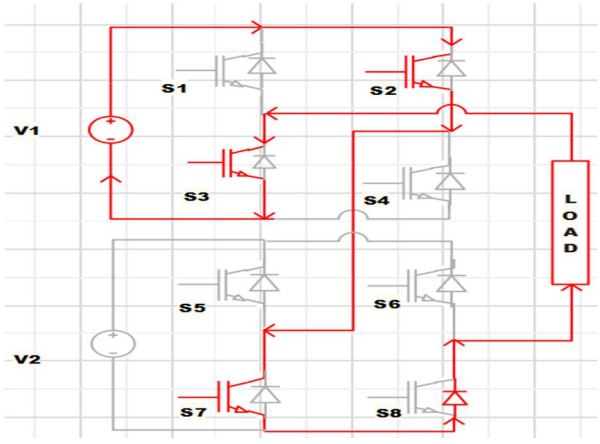


Fig 7 operation of the circuit to generate the output voltage as –V

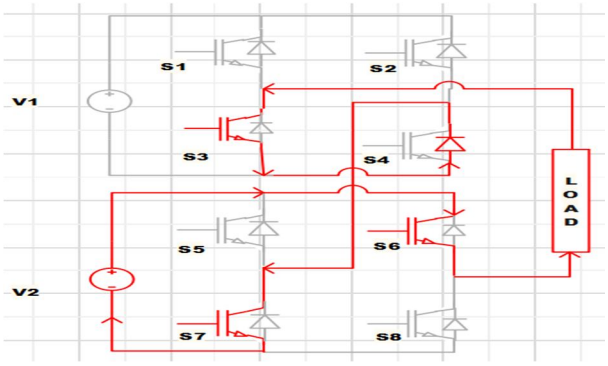


Fig 8 operation of the circuit to generate the output voltage as -2V

To get the output voltage as -2V the switches S3, S4, S6 & S7 will be in ON state and remaining will be in OFF state and the V2 will be connected to the circuit it can be observed from the figure 8.

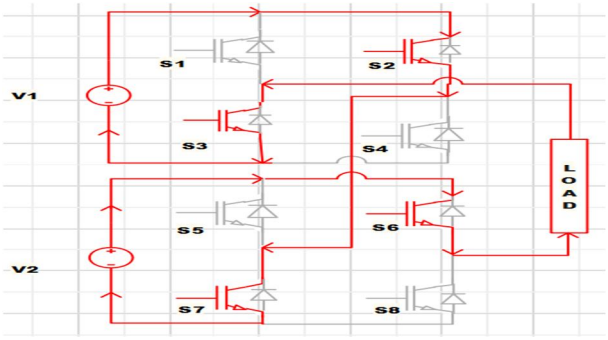


Fig 9operation of the circuit to generate the output voltage -3V

To get the output voltage as -3V the switches S2, S3, S6 & S7 are in ON state and reaming will be in OFF state,which can be observed from the figure 9.

The table provides a summary of the required switching states for the operation of the asymmetrical cascaded seven-level inverter, from the table it can be observed that for each state four switches are operating.

Table 1: Asymmetrical inverter switching state

	3V	2V	V	0V	-V	-2V	-3V
S1	1	0	1	0	0	0	0
S2	0	0	0	0	1	0	1
S3	0	1	0	1	1	1	1
S4	1	1	1	1	0	1	0
S5	1	1	0	0	0	0	0
S6	0	0	0	0	0	1	1
S7	0	0	1	1	1	1	1
S8	1	1	1	1	1	0	0

III. SIMULATION OF ASYMMETRICAL SEVEN LEVEL INVERTER MLI

The figure 10 shows the simulink mode of asymmetrical seven level mli connected to an induction motor.

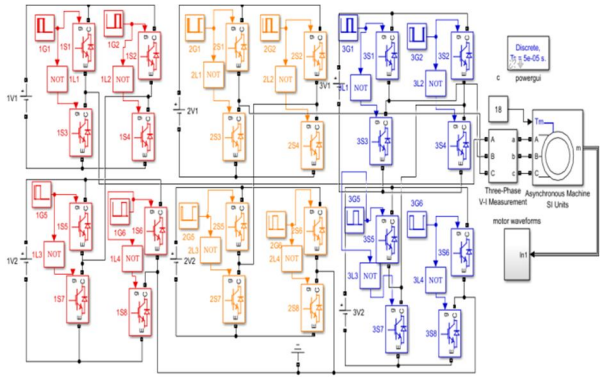


Fig 10 Simulink model for asymmetrical seven level MLI

The control signals for the driver circuit are shown in figure 11. The switches S1 & S3, S2 & S4, S5 & S7, S6 & S8 are complement to each other.

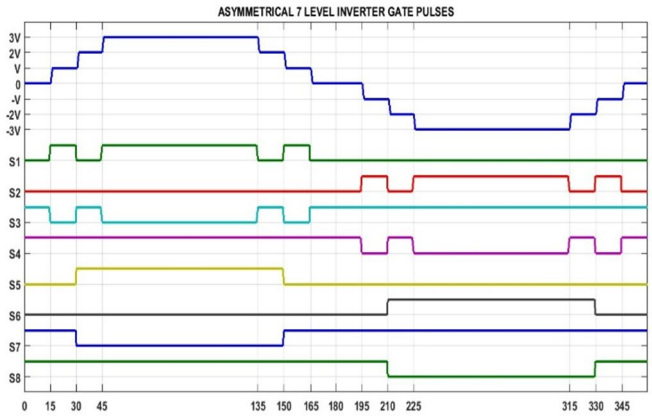


Fig 11 switch control circuit for asymmetrical seven level MLI

IV. RESULTS AND CONCLUSION

The phase and line voltages and corresponding Total Harmonic Distortion (THD) are shown from figure 12 to 15**.**

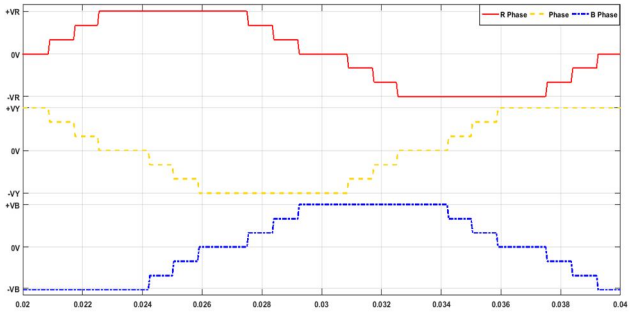


Fig 12 output phase voltages

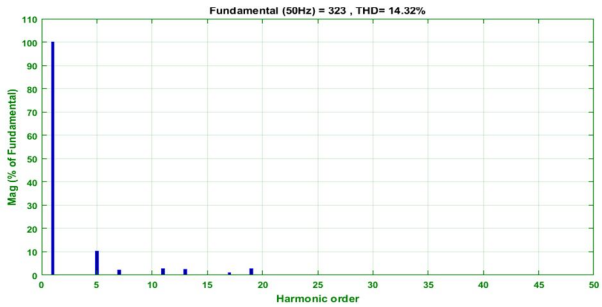


Fig 13 frequency spectrum of phase voltage

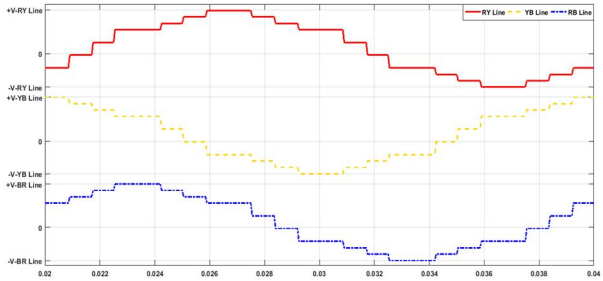


Fig 14 output line voltage

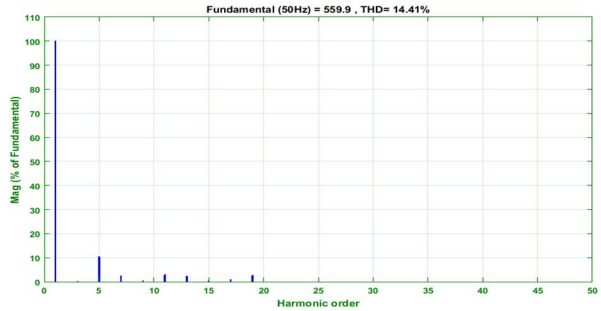


Fig 15 frequency spectrum of line voltage

Based on the results, it can be concluded that the asymmetrical cascaded MLI necessitates a reduced number of elements per phase for generating a seven-level voltage output. Moreover, the scope of this study can be extended to explore various pulse width modulation techniques aimed at mitigating the impact of dominant harmonics.

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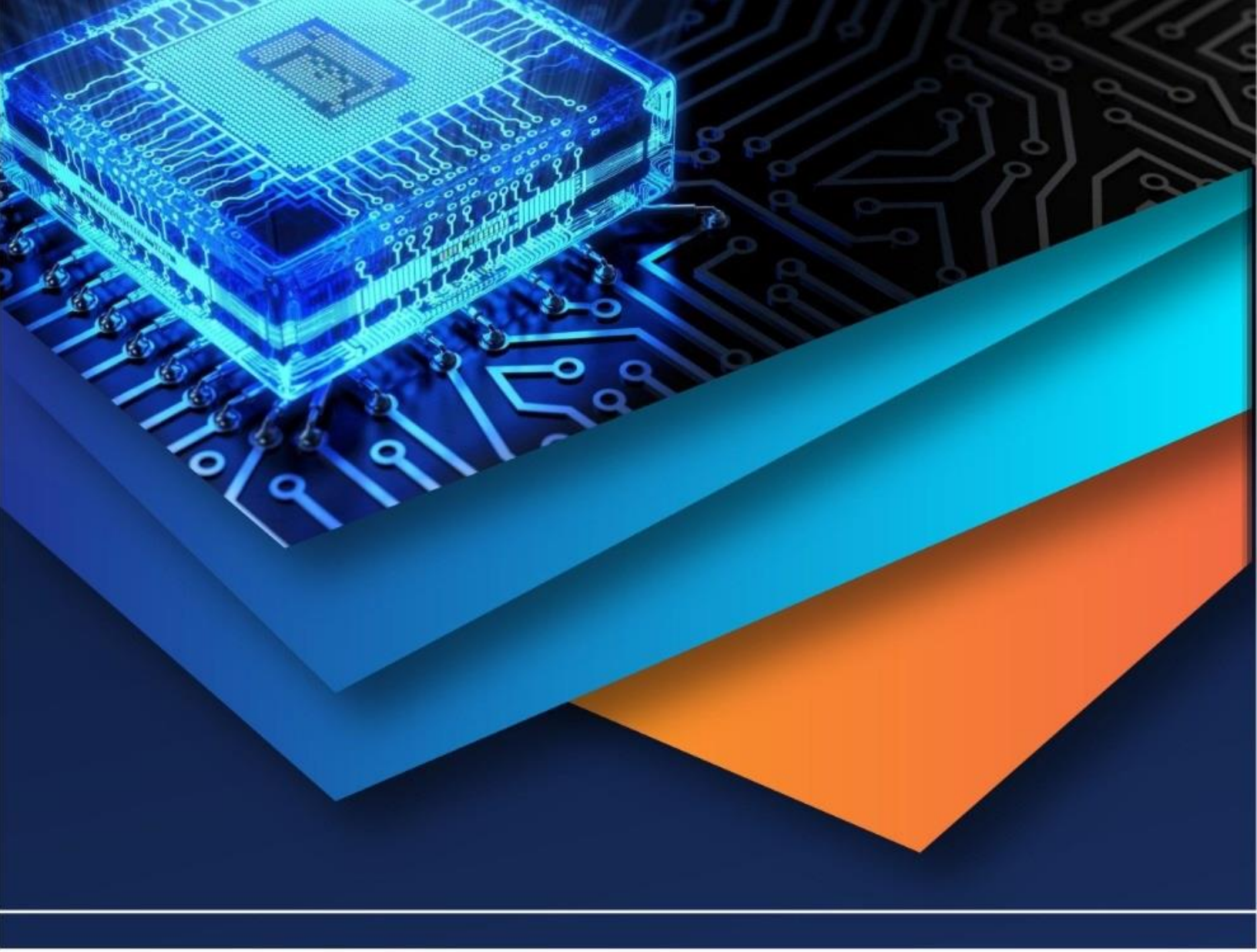
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