iJRASET
International Journal For Research in Applied Science and Engineering Technology

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 13 **Issue:** XII **Month of publication:** December 2025

DOI: https://doi.org/10.22214/ijraset.2025.76158

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 13 Issue XII Dec 2025- Available at www.ijraset.com

Single Phase Multi Level Inverter Design for Resistive Load

Tarakeshwari V, Roshan Naika S, Raghavendra M, Ullasgouda V Patil, Tilak S
Department of Electrical & Electronics Engineering, SJB Institute of Technology, Bengaluru, Karnataka, India

Abstract: ***The need for multilevel inverters has grown rapidly in recent years, particularly in applications involving high power and high voltage. Their ability to generate output waveforms that closely resemble a pure sine wave makes them highly effective in minimizing harmonic distortion and enhancing overall power quality.This paper presents the design and development of a five-level cascaded H-bridge multilevel inverter, realized through MATLAB/Simulink simulations as well as a hardware prototype driven by a microcontroller. The cascaded H-bridge configuration is chosen because of its modular structure, ease of control, and capability to produce higher output voltages using medium-voltage switching devices. By producing multiple voltage steps that shape a smoother sinusoidal waveform, the proposed system successfully lowers switching losses, improves output waveform quality, and offers strong potential for use in high-power industrial systems and renewable energy applications.***

I. INTRODUCTION

Power electronic circuits are essential components of today's energy systems, particularly in the growing field of renewable energy. These circuits are designed to convert, regulate, and control electrical power based on system requirements. For instance, converting AC to DC is performed by a rectifier, while converting DC to AC—known as inversion—is carried out by an inverter.

Multilevel inverters (MLIs) have become increasingly popular in medium-voltage and high-power applications because they offer significant advantages over traditional two-level inverters. They achieve the desired AC output by combining multiple isolated DC sources to produce several voltage steps. This results in lower switching losses, reduced harmonic distortion, improved electromagnetic performance, and enhanced voltage-handling capability.

The number of output voltage levels produced by a multilevel inverter depends on the number of isolated DC sources (s) and is determined by the relation:

$$n = 2s + 1$$

For example, when two isolated DC sources are used $(s = 2)$, the inverter produces five distinct voltage levels, forming a five-level cascaded H-bridge configuration.

In this structure, each H-bridge cell generates a specific voltage level, and the outputs of these cells are connected in series. This series connection creates a stepped output waveform. The total output voltage $(V_0)$of the cascaded H-bridge inverter is obtained by summing the voltages of the individual cells, expressed as:

$$V_0 = V_1 + V_2$$

This approach allows the system to synthesize a smoother and more sinusoidal output waveform, making it suitable for a wide range of high-power applications.

II. OBJECTIVE

The main objective of this project is to design and implement a multilevel inverter that can efficiently convert direct current (DC) into alternating current (AC) with improved power quality. Conventional two-level inverters often produce outputs with noticeable harmonic distortion, which reduces efficiency and affects overall system performance. To address these issues, this work focuses on developing a five-level Cascaded H-Bridge (CHB) inverter. The proposed system is analyzed through MATLAB/Simulink simulations and validated through hardware experimentation. The goal is to generate an output waveform that closely resembles a pure sine wave, reduce harmonic content, enhance conversion efficiency, and confirm system reliability through both theoretical study and practical testing.

Cascaded Multilevel Inverter

A cascaded multilevel inverter is composed of several H-bridge inverter cells connected in series to produce multiple stepped voltage levels. Each H-bridge module provides a portion of the output voltage, and the overall AC waveform is formed by summing the voltages generated by each cell. When the inverter uses *k* cascaded H-bridge cells, the total number of voltage levels is given by:

$$\text{Number of levels} = 2k + 1$$

This topology offers numerous advantages over other multilevel inverter structures. It requires fewer switches, resulting in a design that is simpler, lighter, and more economical. The modular arrangement also enhances scalability, ease of maintenance, and fault isolation. Because of these benefits, cascaded multilevel inverters are widely used in high-power systems, industrial drives, and renewable energy applications.

III. LITERATURE SURVEY

1) *Niraj Vijayashankar Mishra —International Journal of Creative Research Thoughts (IJCRT)*

This study discusses the use of multilevel inverters with switching devices to enhance AC waveform quality. The author emphasizes that multilevel inverter technology is an effective and practical solution for increasing power-handling capability while reducing harmonic distortion. The proposed design uses eight switches to generate multiple voltage levels. The work concludes that increasing the number of output levels while keeping the number of switches low can significantly reduce switching losses, minimize harmonic distortion, and lower both filter and overall system costs.

2) *Mohammed Sameer M. Attar — International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering*

In this paper, the author introduces a single-stage five-level inverter suitable for grid-connected photovoltaic (PV) systems. The inverter adjusts its output current automatically based on the PV array voltage, improving adaptability under varying conditions. A Sinusoidal Pulse Width Modulation (SPWM) control strategy is employed, which removes the need for a phase-locked loop during grid synchronization. MATLAB-based simulations confirm the feasibility and reliability of the proposed design, highlighting its usefulness in renewable energy grid-integration.

3) *Jyoti M. Kharade — International Journal of Innovative Research in Science, Engineering and Technology*

This work provides a comparative analysis of cascaded H-bridge multilevel inverters with three, five, and seven output voltage levels. MATLAB/Simulink is used to evaluate key parameters such as the number of switches required and the independent DC sources needed for each configuration. The results show that increasing the number of voltage levels improves waveform quality but also increases design complexity, emphasizing the trade-off between performance and hardware requirements.

4) *Abhishek Kumar Ranjan — International Conference on Circuit, Power and Computing Technologies (ICCPCT)*

This paper studies the use of level-shifted PWM techniques for symmetric cascaded H-bridge multilevel inverters. Total Harmonic Distortion (THD) is analyzed using Fourier techniques for several voltage-level configurations, including 5-level, 7-level, 9-level, 11-level, 13-level, and 21-level systems. FFT analysis on a resistive load reveals that higher voltage levels produce significantly improved harmonic performance, confirming the effectiveness of multilevel topologies in reducing distortion.

5) *Wahyu Mulyo Utomo &Afarulrazi — International Journal of Engineering & Technology (2018)*

This research proposes a 7-level cascaded H-bridge inverter designed to reduce total harmonic distortion. Two SPWM modulation techniques—Phase Disposition (PD) and Phase Opposition Disposition (POD)—are evaluated. Simulation results from MATLAB/Simulink show that the PD technique performs better, producing lower harmonic content compared to POD. The study demonstrates the capability of the 7-level inverter topology to deliver superior waveform quality and improved efficiency.

IV. METHODOLOGY

The methodology adopted for this project follows a systematic and step-by-step approach, beginning with theoretical study and progressing through simulation, hardware development, and final experimental verification.

The process started with an in-depth review of the working principle of a five-level cascaded H-bridge inverter. This involved understanding how isolated DC sources and multiple H-bridge cells combine to generate a stepped AC output. Particular attention was given to the function of switching devices, PWM-based control strategies, and the influence of multilevel operation on harmonic reduction and power quality enhancement.

The next phase focused on simulation using MATLAB/Simulink. The inverter topology was modelled by connecting two H-bridge modules in cascade. PWM signals were designed to control the switching pattern of each device.

The simulation environment allowed observation of output waveforms, switching behaviour, and voltage transitions. The results clearly displayed the expected five-level stepped waveform and demonstrated a notable reduction in harmonics compared to a conventional two-level inverter.

After obtaining satisfactory simulation results, the hardware prototype was developed. Essential components—including MOSFETs, TLP250 optocoupler-based gate drivers, an ATmega328/Arduino UNO microcontroller, rectifier unit, passive filters, and power supply modules—were chosen according to design requirements. Gate driver circuits were built to ensure proper electrical isolation and reliable triggering of MOSFETs. The PWM control algorithm was programmed and uploaded using the Arduino IDE. To ensure stable operation, each subsystem—the microcontroller unit, gate driver stage, power stage, and rectifier—was individually tested before full system integration.

Once assembled, the inverter prototype was supplied with independent DC sources corresponding to each cascaded H-bridge cell. The output waveform was captured using a CRO and compared with the simulation results. The hardware output exhibited the expected five-level stepped pattern, confirming correct switching behaviour and successful implementation of the cascaded topology.

Finally, the system performance was evaluated based on waveform smoothness, harmonic reduction, switching accuracy, and operational stability. This structured methodology—from theoretical understanding to simulation, hardware construction, and experimental validation—ensured reliable results and confirmed the effectiveness of the proposed five-level cascaded H-bridge multilevel inverter.

V. HARDWARE IMPLEMENTATION

A. *Working Methodology*

Conventional two-level and three-level inverters often struggle to effectively suppress unwanted harmonic components in the output waveform. To address these limitations, multilevel inverter topologies are employed as a superior alternative to traditional PWM-based inverters. In a cascaded multilevel structure, the number of possible phase voltage levels at the output is determined by:

$$\text{Output Levels} = 2N + 1$$

where **N** is the number of H-bridge cells or isolated DC input sources.

In this configuration, each H-bridge cell operates with its own dedicated DC source, enabling independent switching control for every stage. Because each module contains its own DC link capacitor, the voltage across individual cells may vary depending on loading conditions and switching patterns. Every H-bridge unit can generate three fundamental voltage states—positive, zero, and negative. By appropriately combining these states across all cascaded cells, the inverter produces a symmetric and stepped output waveform.

The total output voltage is obtained by summing the voltages contributed by each H-bridge module. Since the voltage levels are arranged symmetrically around a reference neutral point, the resulting number of output levels is always an odd value. This stepped voltage waveform enhances power quality, significantly reduces Total Harmonic Distortion (THD), and minimizes the need for large filtering components when compared to conventional inverter designs.

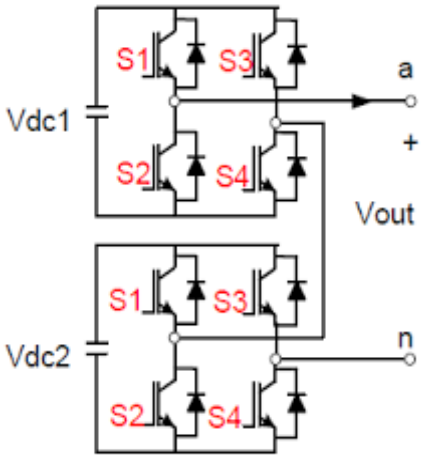


Fig 1: Five level cascaded H-bridge multilevel invert

In a five-level cascaded H-bridge inverter, two H-bridge modules are connected in series, with each module consisting of four switching devices and an independent DC input source. The system is initially designed and analysed using MATLAB/Simulink and the SimPowerSystems toolbox to study the waveform characteristics, switching behaviour, and performance of the topology.
The five-level inverter achieves its output by combining the voltage states produced by the two cascaded H-bridges. Each H-bridge can generate three basic states—positive, zero, and negative voltage. By coordinating these states using an appropriate switching strategy, the inverter produces five distinct output voltage levels. This stepped waveform minimizes harmonic distortion and delivers a smoother AC signal compared to a traditional two-level inverter. As a result, this topology is highly suitable for medium- and high-power applications where high-quality output is essential.

B. Key Features

1) Modular Design

The inverter is composed of two H-bridge modules connected in cascade. Each module operates independently using four switches. This modularity allows easy expansion of voltage levels by adding more H-bridge cells.

2) Independent DC Sources

Each H-bridge requires its own isolated DC power supply. For a five-level configuration, two independent DC sources are used, enabling flexible power input arrangements and improved control over voltage levels.

3) PWM-Based Switching Control

Pulse Width Modulation (PWM) is employed to manage the switching sequence for both H-bridge modules. Accurate PWM control enhances timing precision, reduces switching losses, and ensures smoother output waveforms.

4) Five Discrete Voltage Levels

By combining the switching states of the two cascaded modules, the inverter generates the following voltage levels:

+Vdc, +Vdc/2, 0, –Vdc/2, –Vdc

This multi-step output significantly improves waveform quality and reduces total harmonic distortion.

C. Hardware Components Used

- MOSFET switching devices
- TLP250 optocoupler-based gate driver IC
- 2N222 transistor
- CK100 transistor
- Resistors
- Regulated DC power supply
- Microcontroller (Arduino/ATmega-based)
- Rectifier unit
- Output filter
- PCB board
- Connecting wires

Detailed Hardware Architecture and Circuit Implementation

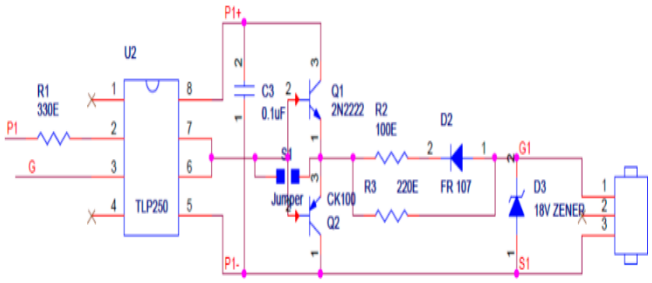


Fig2: Circuit diagram

1) IRFZ44N MOSFET

The IRFZ44N MOSFET serves as the primary switching device in each H-bridge cell of the inverter. It is an N-channel enhancement-type MOSFET rated for a drain current of 49 A and a maximum drain–source voltage of 55 V. Its low on-state resistance of approximately 17.5 mΩ helps minimize conduction losses and enhances overall inverter efficiency. A total of eight MOSFETs—four per H-bridge—are employed to produce the required five-level stepped AC output. Owing to its fast-switching capability, the IRFZ44N supports smooth PWM transitions, which is essential for generating high-quality waveforms.

2) TLP250 Gate Driver

The TLP250 acts as the interface between the low-voltage PWM signals generated by the Arduino and the MOSFET gate terminals. Since MOSFETs require a gate voltage of around 10–15 V for proper switching, the TLP250 boosts and isolates the control signals. Operating within a 10–30 V range, it supports high-frequency switching suitable for SPWM-based inverter operation. Its optical isolation provides protection for the microcontroller against voltage spikes and ensures clean, stable switching.

3) 2N2222 / CK100 Transistor

General-purpose transistors such as the 2N2222 and CK100 are incorporated into the driver circuitry for signal amplification and conditioning. The 2N2222 NPN transistor, with its 600-mA current capacity, strengthens weak PWM signals to ensure reliable triggering. The CK100 performs similar low-power switching tasks. Together, these transistors help maintain stable and consistent gate-drive signals for MOSFET operation.

4) Resistors

Resistors of various values—from 220 Ω to several kilo-ohms—are placed throughout the circuit for current limiting, biasing, and signal stabilization. They are used in the TLP250 input stage, in transistor bias networks, and as pull-down resistors for MOSFET gates. Depending on their role, resistors with power ratings of ¼ W or ½ W are selected to ensure safe and reliable operation without overheating.

5) Power Supply Module

Different regulated voltage levels are required for the inverter's control and power stages. A 5 V regulated source powers the Arduino, while the gate drivers operate from a 12–15 V DC supply. Additionally, two isolated DC voltage sources feed the cascaded H-bridge stages to generate the stepped output waveform. The power supply module ensures electrical isolation, stable voltage levels, and reliable operation of all components.

6) Arduino UNO (ATmega328P Microcontroller)

The Arduino UNO serves as the central control unit responsible for generating sinusoidal PWM (SPWM) signals. Operating at 5 V and driven by a 16 MHz clock, it provides the precise timing required for multilevel switching. With its six PWM-capable output pins and 32 KB of flash memory, the Arduino efficiently manages the switching sequence and overall logic of the inverter.

7) 1N4007 Diode

The 1N4007 diode is used primarily for rectification and reverse-voltage protection. With its 1000 V reverse-voltage rating and 1 A current capability, it safeguards the gate driver and control circuitry during high-voltage transitions. It prevents reverse current flow that could potentially damage sensitive components, thereby improving overall circuit reliability.

8) LC Output Filter

An LC filter—comprising an inductor and capacitor rated for high voltage—is connected at the output of the inverter to smooth the stepped voltage waveform. This filter helps suppress harmonics and shape the waveform closer to a sinusoidal signal. The presence of the LC filter enhances power quality, making the inverter well-suited for resistive load testing during hardware evaluation.

9) PCB Board

A general-purpose printed circuit board (PCB) is used to assemble the driver, transistor, and resistor networks. The PCB layout helps maintain organized routing, reduces noise, and ensures proper thermal management. High-current paths are routed separately from low-signal traces to avoid interference and enhance stability.

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 13 Issue XII Dec 2025- Available at www.ijraset.com

10) Connecting Wires and Jumpers

Insulated connecting wires and jumper cables are used to establish electrical connections between control circuits and the power stage. Proper insulation prevents accidental short circuits and ensures reliable operation, particularly during high-speed switching.

D. WORKING MODEL

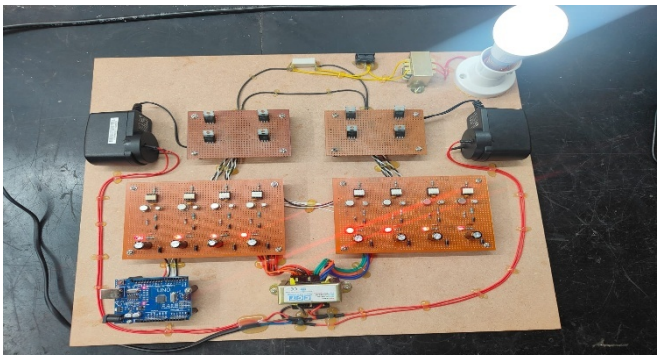


Fig 3: Working model of the project

E. MATLAB simulation

Software (MATLAB Simulink)

Simulation plays an essential role in modern engineering because it allows systems to be tested virtually before building a physical prototype. By using mathematical models and algorithms, simulation helps predict how a system will behave under different operating conditions, making design, testing, and optimization more efficient.

Simulink provides a wide range of tools that support advanced modelling, control design, and implementation. Some key features include:

- State flow – Used for developing state machines and logic-based systems using diagrams and flowcharts.
- Simulink Coder – Automatically converts Simulink models into C source code suitable for real-time applications.
- xPC (External Personal Computer) Target – Together with x86-based real-time systems, allows real-time testing and execution of Simulink and Stateflow models on actual hardware.
- Embedded Coder – Provides optimized code generation tailored for specific embedded processors and platforms.
- HDL Coder – Generates synthesizable VHDL and Verilog code for FPGA and ASIC designs.
- SimEvents – Offers blocks for modelling event-driven and queue-based systems, often used in network or logistics simulations.

Simulink also supports verification and validation processes, ensuring that models meet design requirements. Tools such as requirements traceability, model style checking, and coverage analysis help improve model accuracy and reliability. Additionally, Simulink Design Verifier assists in identifying design flaws and can automatically generate test scenarios for thorough model testing.

1) Simulink

When Simulink is opened, it starts with the Library Browser, which acts as the central workspace for creating simulation models. The Library Browser contains all the built-in blocks and tools needed to design and simulate various systems.

The left panel of the Library Browser displays different block libraries grouped according to their functions, such as power electronics, signal processing, control systems, and mathematical operations. When a category is selected, the corresponding blocks appear on the right panel. From there, users can simply drag and drop the required components into the model workspace.

This intuitive, well-organized interface makes it easy to find the necessary blocks and construct simulation models efficiently and systematically.

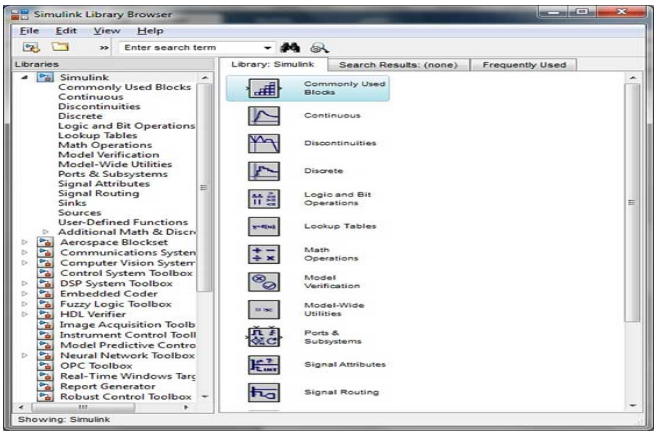


Fig 4: Simulink Library Browser

2) Building Models

To create a new model in Simulink, click on the **new** icon in the Library Browser toolbar. This action opens a blank model workspace, providing an empty canvas where you can start arranging blocks and designing your system. This workspace becomes the primary area for connecting components, defining signal flow, and constructing the simulation model step by step.

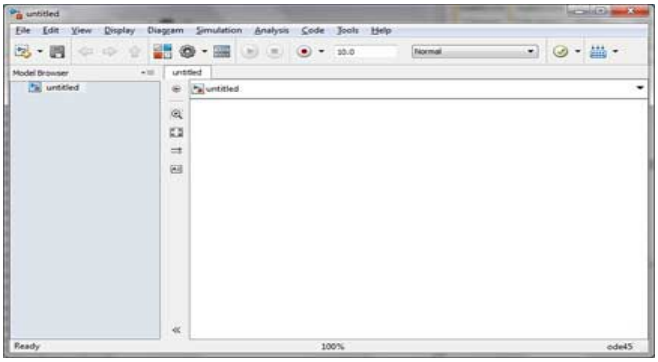


Fig 5: Creating a new model Simulink

To construct a model in Simulink, blocks can be added by selecting them from the Library Browser and dragging them into the model workspace. Alternatively, a block may be copied from the library and pasted directly into the workspace. The drag-and-drop method is commonly preferred because it provides a quick and intuitive way to arrange and organize components while building the simulation.

For a basic demonstration, only two essential blocks are needed: a **Source** and a **Sink**. In this example, a **Signal Generator** is used as the source to create a waveform, while a **Scope** serves as the sink to display the output visually. The generated signal flows through the model and appears on the scope, allowing users to observe system behaviour in real time and understand how the simulation responds.

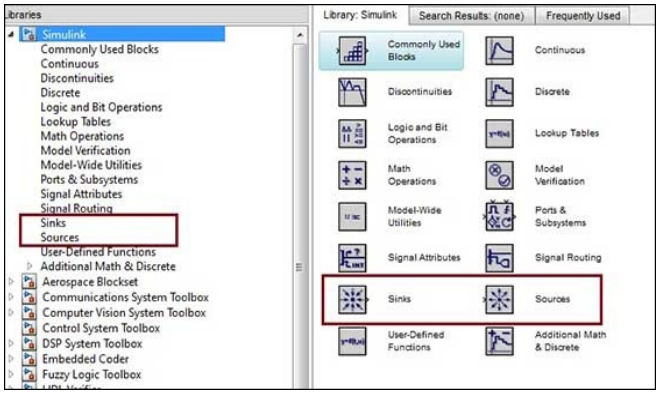


Fig 6: Simulation Library

Once the required blocks are placed in the workspace, the next step is to connect them to create the desired system. This is done by clicking on the output port of one block and dragging the connector to the input port of another. Simulink automatically highlights valid connection points, which makes the wiring process simple and intuitive. By linking the blocks in the correct order, the signal flow is defined, allowing the model to operate exactly as intended.

Let us drag a 'Sine Wave' block into the model.

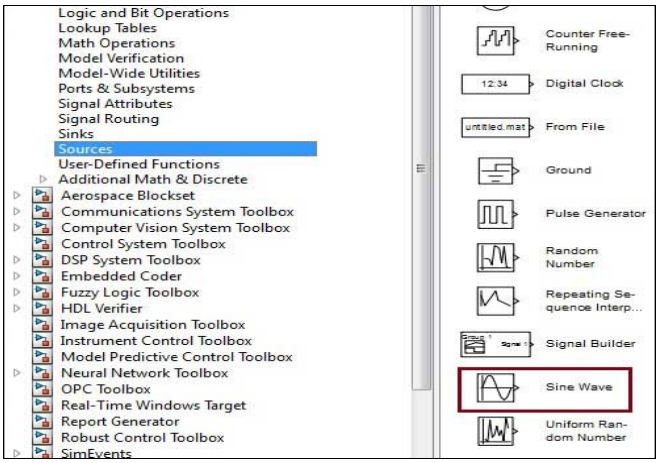


Fig 7: Selection of 'Sine Wave' block into the model

Select 'Sinks' from the library and drag a 'Scope' block into the model.

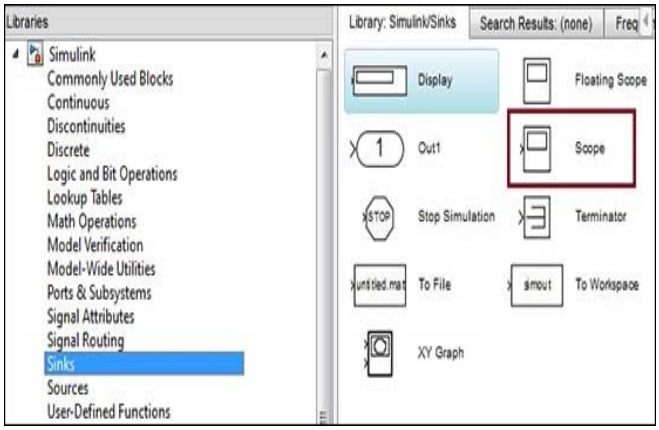


Fig 8: Selection of 'Sinks' block into the model

Drag a signal line from the output of the Sine Wave block to the input of the Scope block.

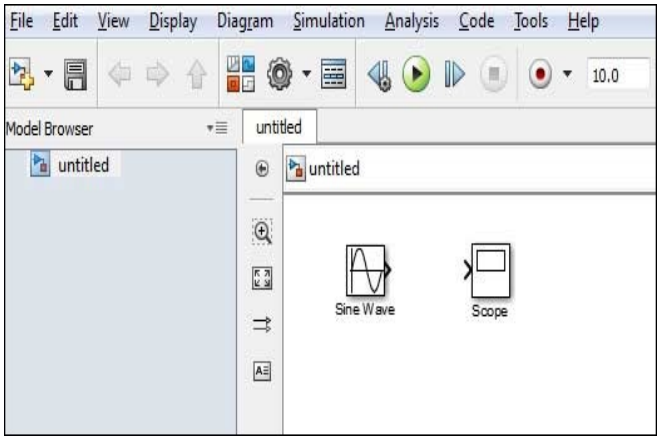


Fig 9: Selection of 'Scope ' block into the model

ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538
Volume 13 Issue XII Dec 2025- Available at www.ijraset.com

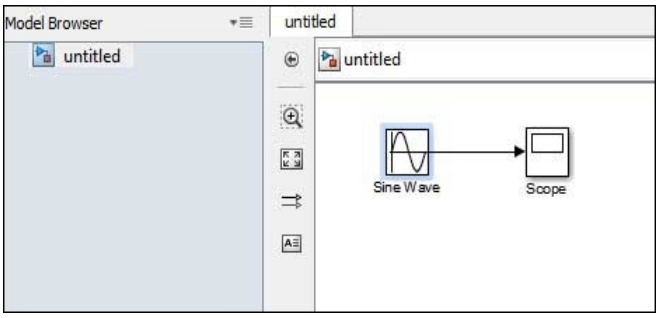


Fig 10:Connection of'Scope ' block

Run the simulation by pressing the 'Run' button, keeping all parameters default (you can change them from the Simulation menu) You should get the below graph from the scope.

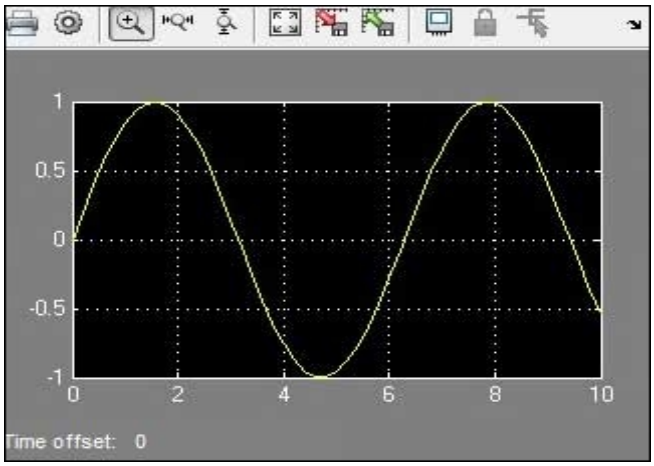


Fig 11: Sample Scope Graph

3) Simulation

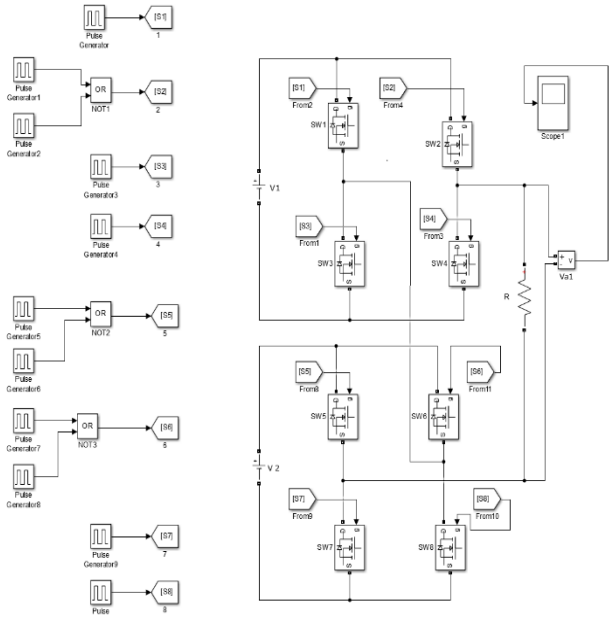


Fig 12: Simulation view

4) Output Waveform

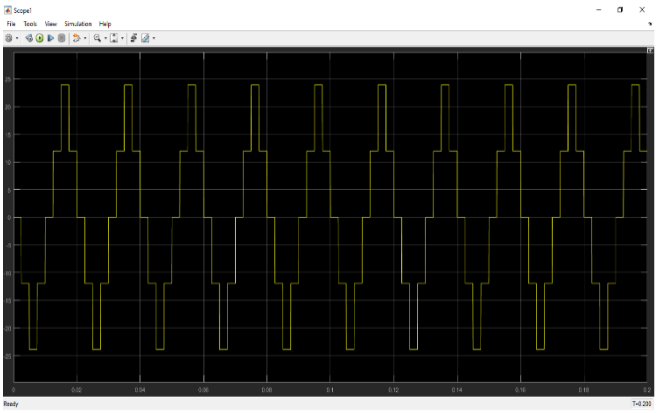


Fig 13: Output Waveform

Advantages

The multilevel inverter offers several benefits that make it suitable for modern power conversion applications. It significantly improves the quality of the output waveform and produces a cleaner sinusoidal signal. The design is simple to use and supports multiple input sources, making it versatile for different configurations. One of the key advantages is the reduction in total harmonic distortion, which enhances system efficiency and performance. The implementation process is comparatively easier and safer, as the topology minimizes the risk of damage to high-power switching components.

VI. FUTURE SCOPE

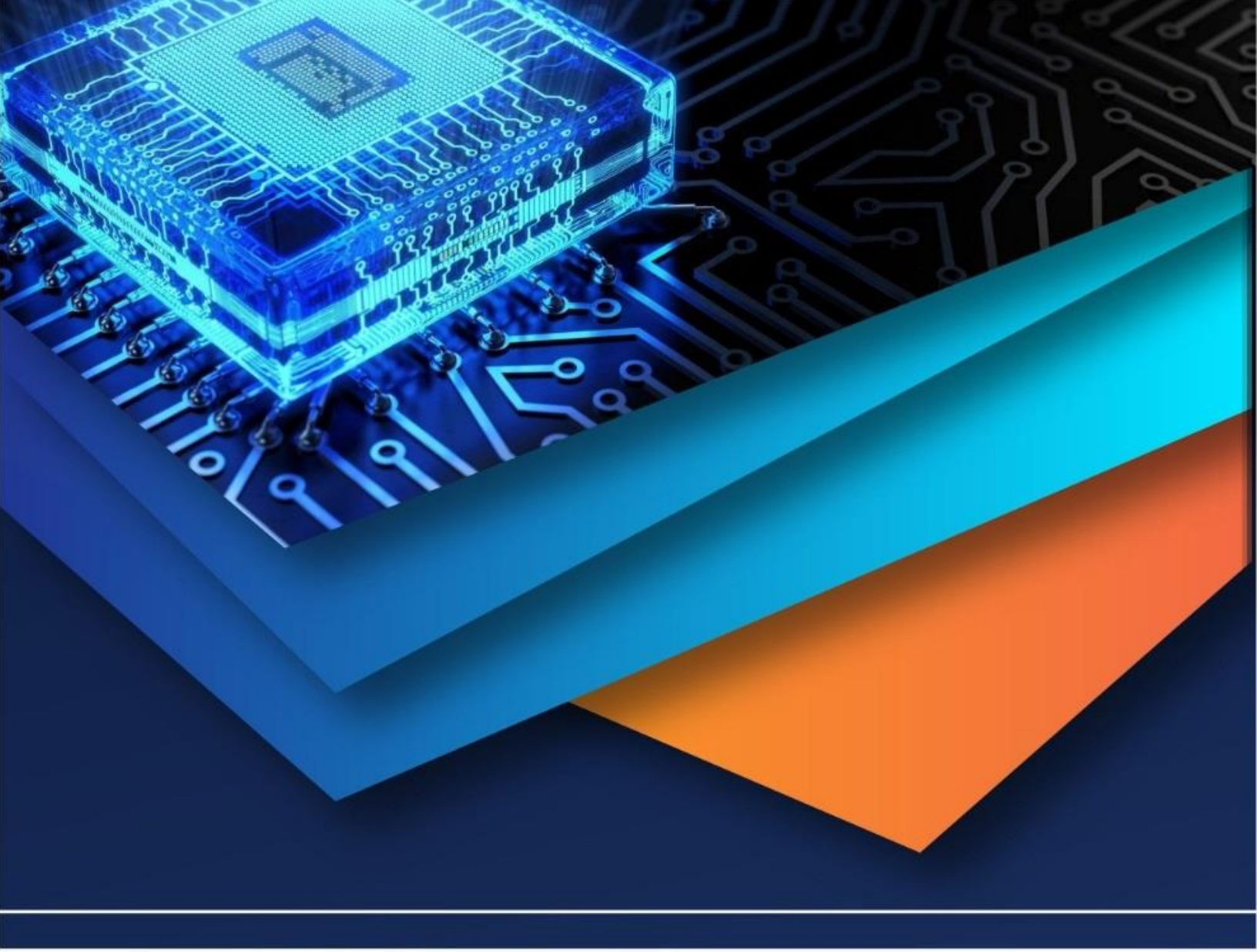
The current implementation demonstrates a complete working model of a multilevel inverter in both simulation and hardware form. Looking ahead, the design can be further enhanced and adapted for real-time industrial applications. While this project uses two independent DC sources, future versions can be optimized to operate using a single power supply. There is also potential to integrate renewable energy sources such as solar or wind power, making the system more efficient, sustainable, and ideal for smart-grid and clean-energy applications.

VII. CONCLUSION

Multilevel inverters play a crucial role in modern power conversion systems, especially in applications requiring high voltage and high power such as industrial drives, power transmission, and transportation systems. Among different topologies, the cascaded multilevel inverter stands out due to its flexibility, modular structure, and improved output waveform quality. In this project, a five-level cascaded inverter was successfully modeled in MATLAB/Simulink and implemented in hardware using an ATmega328 microcontroller. The output waveform was verified using a CRO, and the results confirmed that the hardware closely matched the simulation, proving the effectiveness of the design and its potential for real-world applications.

REFERENCES

[1] N. V. Mishra, “Multilevel Inverter Using Switching Devices for Harmonic Reduction,” International Journal of Creative Research Thoughts (IJCRT).
[2] M. S. M. Attar, “Single-Stage Five-Level Inverter for Grid-Connected PV Systems,” International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering.
[3] J. M. Kharade, “Comparison of Cascaded H-Bridge Multilevel Inverters at Different Voltage Levels,” International Journal of Innovative Research in Science, Engineering and Technology.
[4] A. K. Ranjan, “Level-Shifted PWM Techniques for Cascaded H-Bridge Multilevel Inverters,” International Conference on Circuit, Power and Computing Technologies (ICCPCT).
[5] W. M. Utomo and Afarulrazi, “Analysis of 7-Level Cascaded H-Bridge Inverter Using SPWM Techniques,” International Journal of Engineering & Technology, vol. 7, no. 2.6, pp. 327–330, 2018.
[6] R. Aravindakshan, “Formulation of Performance of Inverters for Solar Photovoltaic Power Plants,” Renewable Energy Grid Integration, 2021. [Online]. Available: https://regridintegrationindia.org
[7] P. Dineshkumar, P. Thirumoorthi, and S. Rajalakshmi, “Hardware Implementation of Grid-Connected Solar PV Inverter,” Energy Research and Development Authority (ERDA), 2020. [Online]. Available: https://www.erda.org



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY