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Smart Implementation of SS Hybrid Single Electron Model and its Simulation using MATLAB

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Abstract: ***The authors present a novel simulation technique for simulating nanodevices. Single Electronics (SE) is a blessing for both business and academia in the post-CMOS age. Due to SE's inherent drawbacks, including its low gain, unpredictable back ground charge creation, and demand for a very low room temperature during manufacturing, it hasn't yet been decided whether it will be the only mode to replace CMOS. This SE-CMOS hybridization is anticipated to bring about great satisfaction in the development of practical and more dependable nanodevice constructions. The delicate part is that this hybridization necessitates the use of two unique simulators in order to replicate a single model. Unfortunately, this causes hybrid model simulation to be quite difficult. On the other hand, the idea of macro-modeling the hybrid models for the purpose of simulation is in fact beneficial. In this instance, the authors utilized one such macro-model to improvise the hybrid SE model, and a very new SS hybrid SE model is subsequently produced. The majority of the research on hybrid SE that has been published so far supports the use of two different simulators, such as SPICE and SIMON; both are sequentially utilized to simulate one particular model, which ultimately takes a lot of time. The authors take a step ahead in this section by simulating the proposed SS hybrid SE model in MATLAB. They predict that this model may eventually be added to SIMULINK's SIMSCAPE since it is more accurate, less time-consuming, and easier to understand.***

Keywords: Single Electronics; Hybrid Single Electronics; SS (Sanjay Soumyendu) Model; Macro Modelling; SIMSCAPE.

I. INTRODUCTION

Downsizing MOSFETs and scaling them in nm span imperiled unwanted short-channel effects, stochastic quantum effects, high power consumption tenacity, high power leakage factor, increased thermal noise. Beyond all, the technological limitations augmented the Red Brick Wall of CMOS technology [1]. This led to deepened research inquisitiveness in reliability analysis, transitive fan-in attributes of new nm devices. Hypothesizing the prompt dissolution of CMOS technology Researchers coxed new device stimulating principle and in accord novel post CMOS technologies were empirically demonstrated. SE made transistors in this category possess an excellent candidature in obtaining triumph over other successor technologies such as Carbon Nano Tubes (CNT), Resonant Tunneling Devices (RTD), Rapid Single Flux Quantum (RSFQ) and Quantum Dots (QD) [2] like devices.

Single Electron Transistor (SET) [3] is a highly charge sensitive device that mimics all physiognomies of MOSFET and is capable of transporting information using one or merely few electrons. Thus it is a promising future-ready nano electronic device having mobility of a speed almost equal to electron speed. Besides, charge sensitivity and low power consumption are considered added virtue of SET. Structurally SET is a quantum device that sways upon electron tunneling phenomena and involves oxidation for switching transition. The power consumption and the heat dissipation reasonably diminish along with the tunneling of electrons in Coulomb Blockade. Persuaded by such tremendous competency SETs now are molded to fabricate logic circuits and even more they are applicable in charge sensor, detection of infrared radiation, ultrasensitive microwave detector, supersensitive electrometer, single-electron Spectroscopy and so on [4]. Meanwhile the proficiency in fundamental fabrication oriented SET revealed intrinsic short comings of SET such as low gain, high output impedance, random background charge and extreme low room temperature operational requirements. But to sustain with the tidal growth of electronic industry SET is to be made omnipresent in future ICs. In view of such prerogative of SETs, researchers initiated amalgamating SET with conventional CMOS and this is considered as a bench-mark research that can postulate novel heuristic reinforcement both for SET and CMOS technology. Hereby the notion of Hybrid CMOS SET (HCS) [5] was administrated and it catered firm pursuit in device research vicinity. Simulation of such prototypes is the key to success for future implementation of HCS modeling. However, simulation of hybrid models pre-requisite two solely distinctive simulating tools and subsequently such simulations are quite painstaking and accuracy of such simulation is linked to larger simulation time. Hence macro modeling of SE is well thought-out as a cognitive remedial to such lingering simulations. The authors here protruded a HCS macro modeling metaphor and has categorically deliberated its testimonials using SIMSCAPE of MATLAB. It is further manifested that offerings of the newly proposed model tunes up in rhythm with physical models proposed by Sarkar et.al [6].

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II. MACRO MODELLING OF SINGLE ELECTRON

The SE system is mounted on tunneling effect and the Coulomb Blockade phenomena. Logically the fabrication of SE circuits tolerate high cost and large processing time alike complications. To overcome such glitches, several attempts has been opted. Efforts are on to make flexible computerized designs with concise simulation time. In this aspects different models are developed continually based on tunneling and quantum mechanics. A number of these simulators are SENECA by Fonseca et al. [7], MOSES by Chen et al. [8], SIMON by Wasshuber et al. [9]. Essentially all of them exploit Monte-Carlo methods for probability calculation of the Coulomb Island in the circuit and thus it takes a large simulation time. In this regard 'Macro Modeling was conceived by Yu e al. [10] which can be simulated in SPICE and also consumes less time compared to its predecessors. Customizing this approximation of macro-modelling the SEs the authors incorporated the macro model of SE in HCS. Eventually, the simulation exhaustion is lessened and accuracy of such designs tender maximized throughput. The authors here in-situ with similar macro models conceived a new hybridized SET-MOS switching device with its macro model namely SS (Sanjay Soumyendu) model.

III. FRAME WORK OF THE SS MODELING

The same cited Yu model while simulated by SPICE diverged from its SIMON based simulation results. The variety of Yu et al., model lies in the Drain current I_{ds} that increases linearly with the Drain to Source voltage V_{ds} whereas in pragmatically I_{ds} increases exponentially with the V_{ds} in Coulomb Blockade region. Besides empirically it has been revealed that base line of I_{ds} increases as Gate to Source voltage V_{gs} increases in Coulomb Oscillation properties. To overcome this problem Wu and Lin [11] amended a new model namely 'Wu Lin SET macro model' where two diodes are connected face to face to block the current flow from the gate to source terminal, thereby mimicking the SE occurrences. It includes the orthodox theory of SE to analyze the circuits. The value of R1 and R2 can be recorded from

$$R1 = CR1+CR2*\cos(CF1*VG) \quad (1)$$

$$R2 = CVp/(CI2-(2CVP/R1(VG))) \quad (2)$$

where CR_1, CR_2, CV_P, CI_2, CF_1 are atypical parameters to fit the input (voltage) and output (current) characteristics at various gate voltages.

A deep insight in all across models the tunneling time is simulated to be 'zero' i.e. expediently the calculation was not viable. To exclude such hindrances Reza Karinian et al. [12] implied another advanced macro-model in which, quantizer blocks were used to calculate the tunneling time; this certainly makes the macro-model more legitimate.

Authors truly motivated by such conceptions improvised SS switching circuit alike Fig. 1; the PMOS is connected in series with the SET macro-model. This particular switch is to be compared with other post CMOS HCS models. Here one significant partial difference is that the SETMOS switch attempted by Sarkar et al., [13] are connected in parallel and thereby the propagation delay in the circuit cannot be ruled out completely. The same said factor is considerably eliminated in SS switch. Moreover, SS switch is merely simulated in one platform (software).

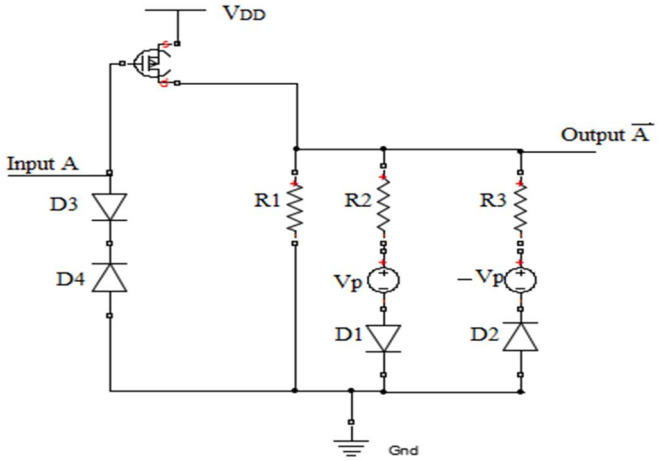


Fig. 1. SS switch

In the subsequent section the authors emphasis upon the reliability of the proposed SS model and chronologically testifies the mobility criterion using SIMSCAPE of MATLAB.

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IV. ORIENTATION OF SS MODEL USING MATLAB

The authors largely counted on SIMSCAPE for modeling the SS model as depicted in figure below (Fig.2). For simplicity and straight forwardness in this inverter model a PMOS is connected just on top of the macro-model of a SET. The input is obtained from the connecting point of the gate of PMOS and SET. The output is taken from the midpoint of drain end and it is add-on to the 'Scope' of the MATLAB [14-20] to avail the desired output as revealed in Fig 2.

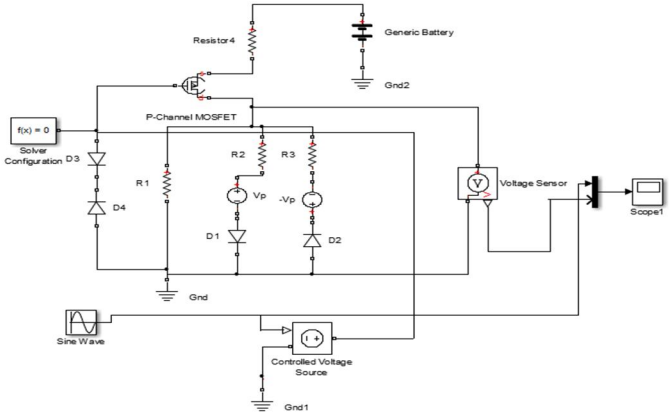


Fig. 2. MATLAB based SS switch made Inverter



Fig. 3. SS switch made inverter output w.r.t given input

Stringent analysis of the resultant waveform in Fig. 3 reveals that the threshold voltage is 2.2V i.e. when the input voltage is below the 2.2V then output is 'high' and when input voltage is above 2.2V then output is 'low' which substantiates the inverter operation.

V. CONCLUSION

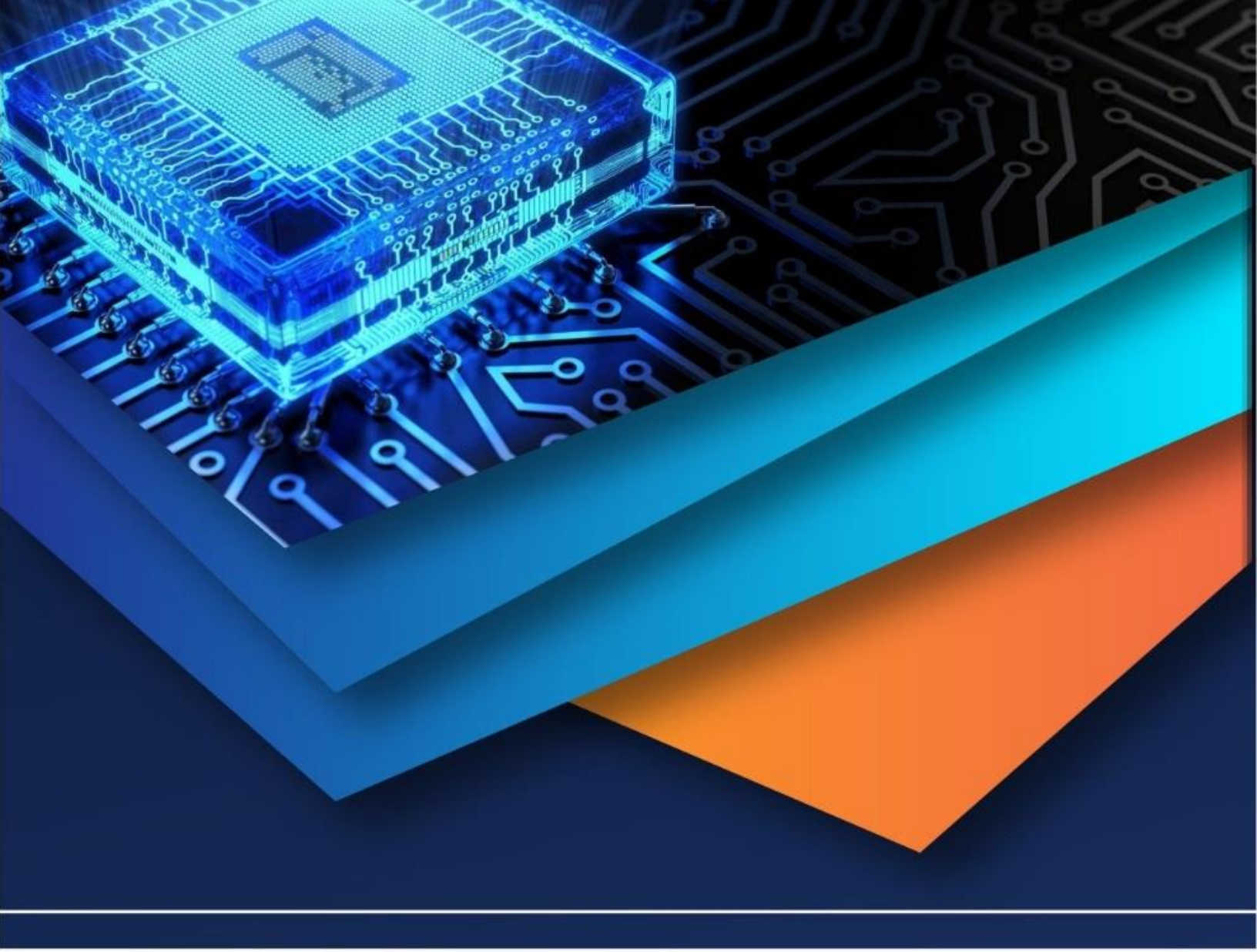
The macro modeling of SE transverse nano device engineering in to a lucrative symphony in future-ready IC topology. The galaxy of single SE is taken forward here to substantiate the SS model. Undoubtedly such modeling is pivotal and forms the basis of advance computing in SE topology as well as it ushers promising ventures in post CMOS era. Subsequently MATLAB has been pondered over to substantiate the simulation in one platform and making it quite straight forward and easy for the Researchers. The results obtained justifies the aspects of HCS likewise low power consumption, high speed of response, low power dissipation. Last but not least the authors here advocate for inclusion of such model in SIMSCAPE of MATLAB so that logical synthesizing can be achieved with linearity.

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