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Transformer Based Cascaded Multilevel Inverter with Reduced Number of Switches

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Abstract: ***This project presents the simulation of "transformer based cascaded multilevel inverter with reduced number of switches" with R-load and. It has the advantages of reduced number of switches and dc sources compared to conventional configurations and consequently higher efficiency. The simulation is accomplished for one stage (3-level), two stage (5-level, 7-level, 9-level), three stage (7-level, 11-level, 15-level, 19-level, 27-level) and four stage (29-level, 31-level, 33-level, 35-level). And their performance is analysed in terms of THD (Total Harmonic Distortion) for output voltages and currents. The FFT (Fast Fourier Transform) analysis is used in order to evaluate the harmonic distortion. The simulation is carried out by using MATLAB/SIMULINK software.***

Index Terms: ***cascaded asymmetric multilevel inverter, transformer-based cascaded multilevel inverter, balance of power distribution.***

I. INTRODUCTION

Multilevel inverters have more popular against conventional inverters based on pulse-width modulation (PWM). This has been gaining importance in the market. Multilevel inverters used in various high power and voltage applications such as wind turbine systems, grid connected systems and motor driven systems and also used for uninterruptible power supply (UPS), photo voltaic generators and generally any DC-AC conversion application. Among different advantages attributed to these converters, such as high power quality that allows high motor performance, low total harmonic distortion (THD) that eliminates the output filters, reduces derivation voltages (dv/dt) that reduces motor insulation damage, reduces switching losses. As drawbacks such that large number of elements in the system. Moreover, as any MLI, the CHB inverter reduces the power quality with the voltage amplitude.

Multilevel inverter topologies are classified into three types: 1) Diode clamped multilevel inverter .2) Flying capacitor multilevel inverter. 3) Cascaded H-bridge multilevel inverter. Compared to these topologies CMLI has the advantage of using independent stages of voltage source inverters. Which leads soft switching techniques can be implemented which reduces switching losses and device stresses, potential of shock reduced due to the separate dc source. Using a single dc source includes low-frequency transformers for each inverter stage. Only one dc power source is used in place of one isolated source per H-bridge. The advantage of only one dc source is automatic voltage balance among H-bridges .By these topologies are known as transformer-based cascaded topologies. The multilevel inverter configuration is defined based on the amplitudes of the input dc sources. If these amplitudes are same, the inverter is said to be symmetric and if the amplitudes are different, the inverter is said to be asymmetric. In this studied topology of transformer based cascaded MLI fed by a single dc source, this definition involves the transformers turn ratios. Turn ratios of all inverter stages are same is said to be symmetric and if they are different said to be asymmetric. Fig 1 represent the circuit diagram of a single phase transformer based cascaded multilevel inverter fed by a single dc source.

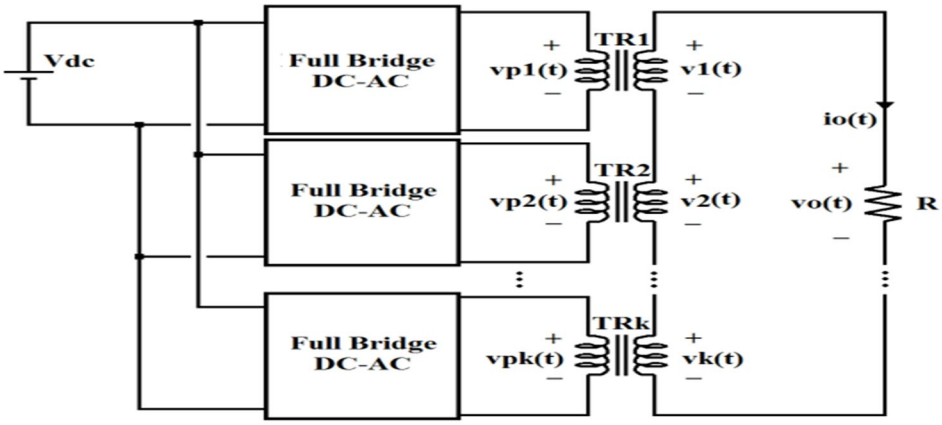


Figure 1: Transformer Based Cascaded Multilevel Inverter

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Symmetric configurations of MLI allow obtaining 2N+1output levels from N stages while asymmetrical configurations permit a high number of levels build upon the ratio between the inverter stages. Using a binary geometric progression to define the ratio between stages, the maximum number of levels at the output will be(2^N+1)-1.using a ternary geometric progression, the number of levels obtained will be 3^N. consider a multilevel inverter with three stages (N=3), a symmetric ratio 1:1:1 allow obtaining a 7-level signal, an asymmetric binary ratio 1:2:4 allows obtaining a 15-level signal and an asymmetric ternary ratio 1:3:9 allows obtaining a 27-level signal. To obtain each level, the converter stages commutate with positive, negative or zero contribution. The way in which the stages of the inverter are commutated to obtain different levels is defined as a switching pattern.

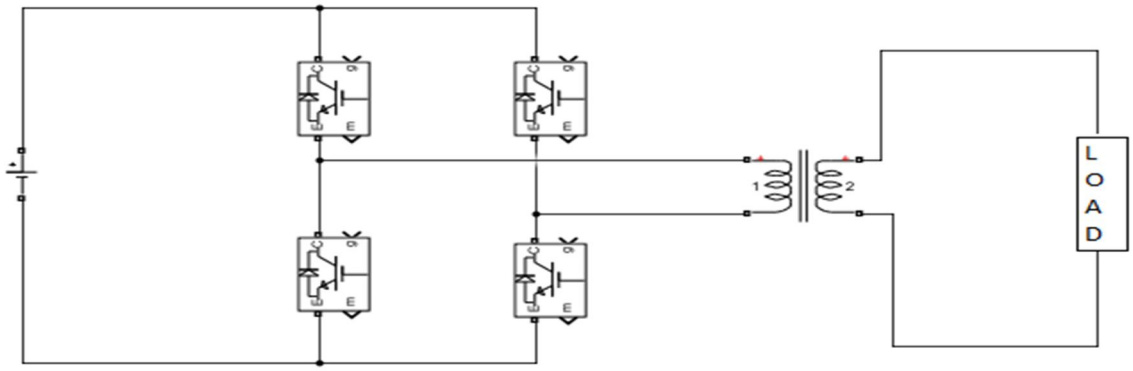


Figure 2: Single Stage Cascaded Multilevel Inverter

The above figure shows the single stage transformer based cascaded MLI. It consists of one dc power source and four switches, one single phase transformer. By the single stage circuit we get the 3-level output waveform as shown in figure below.

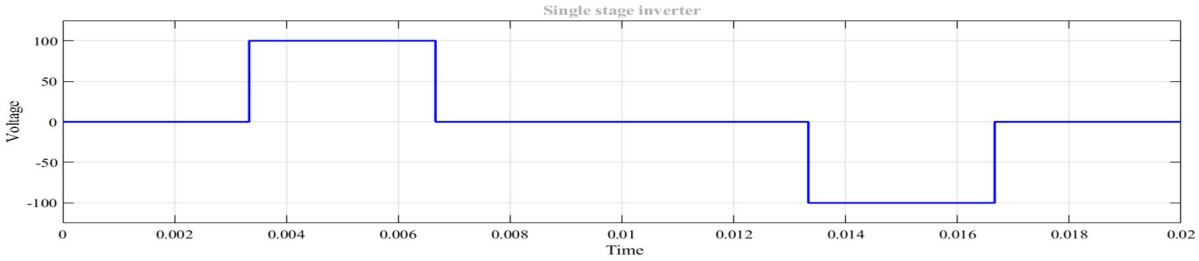


Figure 3: 3-level Cascaded Multilevel Inverter

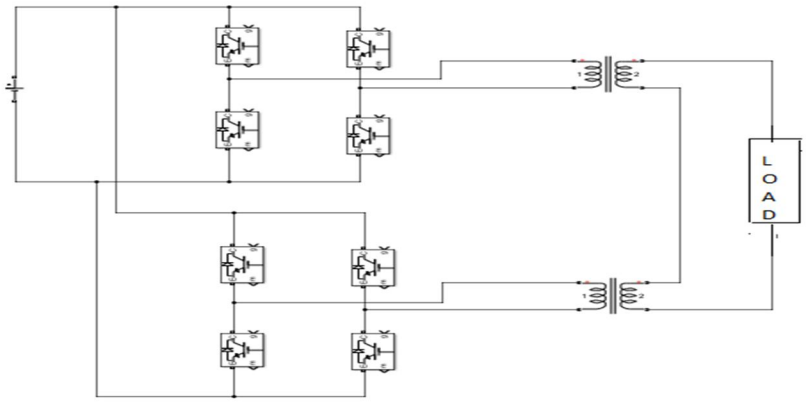


Figure 4: Two Stages Cascaded Multilevel Inverter

The above figure shows the two stage transformer based cascaded MLI. It consists of one dc power source which is connected in parallel and eight switches, two single phase transformers which are connected in series. from the two stage circuit onwards we get symmetric and asymmetric concept.

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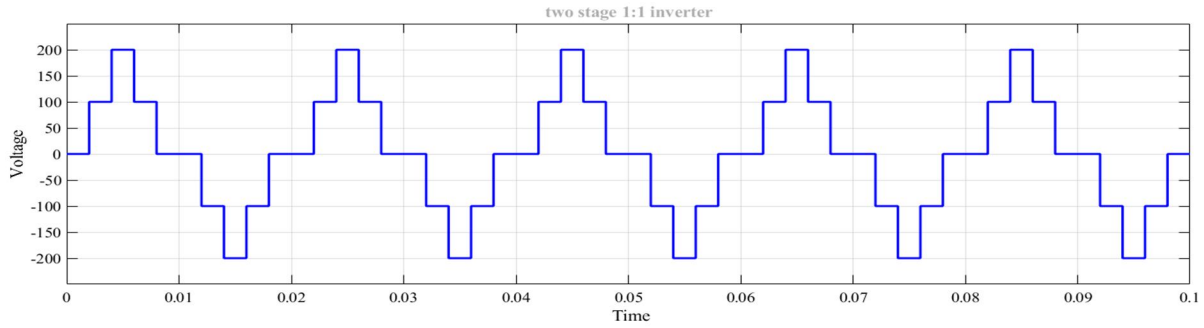


Figure 5: Symmetric (1:1) 5-level Cascaded Multilevel Inverter

Time period = 1/ (frequency) = 1/ (50) =0.02milli sec.
Number of levels = m = 10/cycle.
Total cycle = 360 deg.
Pulse width = 360/m
Phase delay is calculated according to the below formulae by considering each cycle pulse width= 360/10 = 36^0
Phase delay $\frac{T_2-T_1}{T}$ *100%
The above waveform shows the symmetrical ratio of 1:1. By the formula which is stated in above we get 5-level.

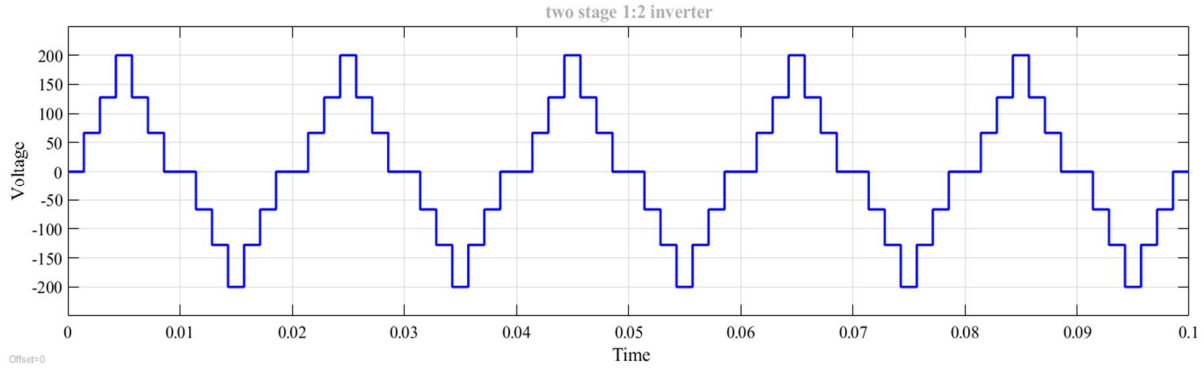


Figure 6: Asymmetric (1:2) 7-level Cascaded Multilevel Inverter

The above waveform shows the asymmetrical binary ratio of 1:2. By the binary ratio formula which is stated in above we get 7-level.

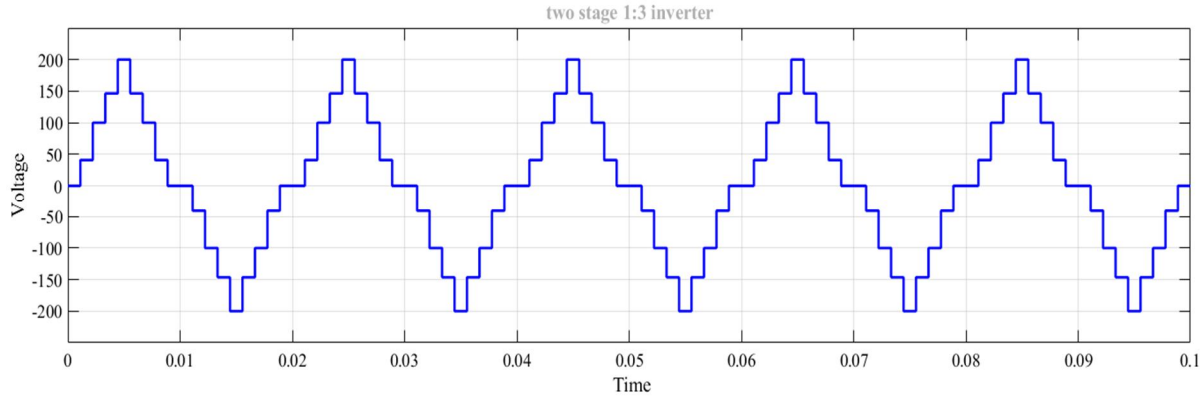


Figure 7: Asymmetric (1:3) 9-level Cascaded Multilevel Inverter

The above waveform shows the asymmetrical binary ratio of 1:2. By the binary ratio formula which is stated in above we get 7-level.

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In two stage cascaded MLI with the 8- switches as shown in above figure we can get 5-level, 7-level and 9-level output voltages. With the same number of switches the output voltage level increases.

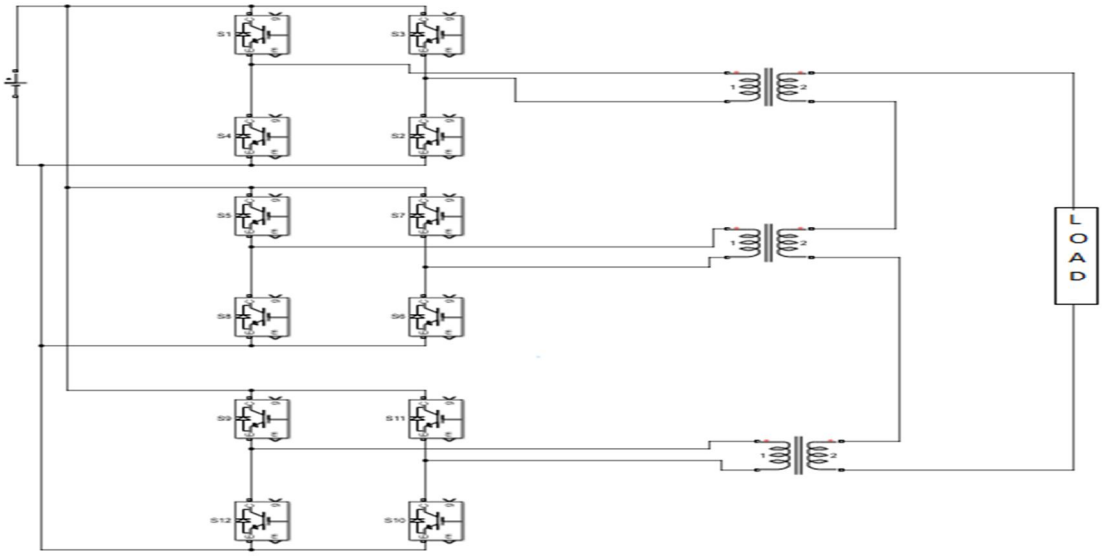


Figure 8: Three Stages Cascaded Multilevel Inverter

The above figure shows the three stage transformer based cascaded MLI. The three bridges are connected to a single dc source which is connected in parallel. And also three transformers, which are connected in series. The primary of transformers connected to a h bridge and secondary's are connected in series to the load in order to synthesis +Vdc, 0, -Vdc.

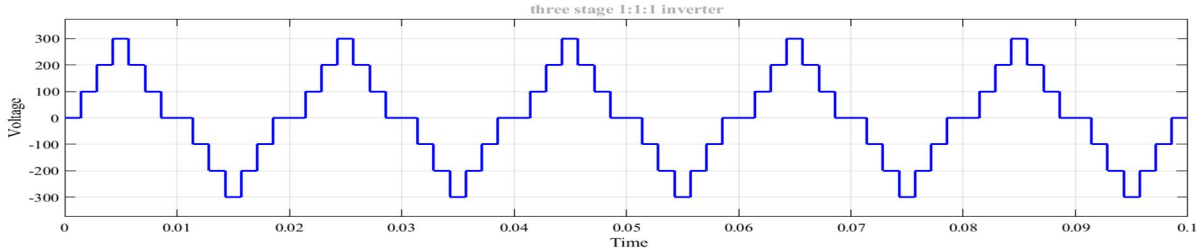


Figure 9: Symmetric (1:1:1) 7-level Cascaded Multilevel Inverter

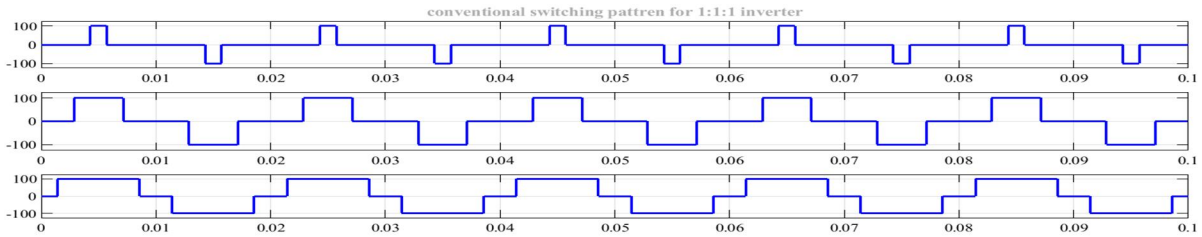


Figure 9(a): Conventional Switching Pattern

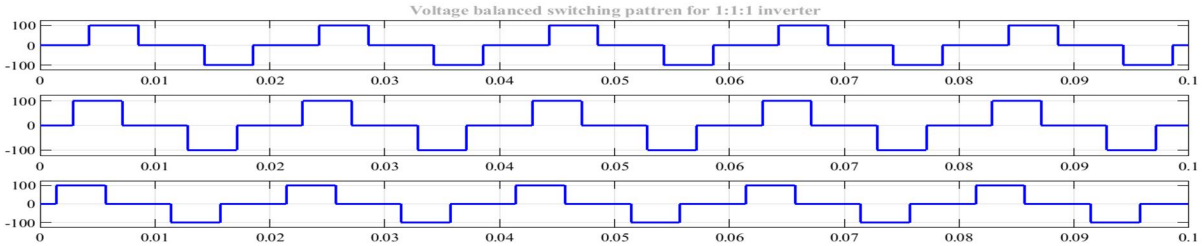


Figure 9(b): Voltage Balanced Switching Pattern

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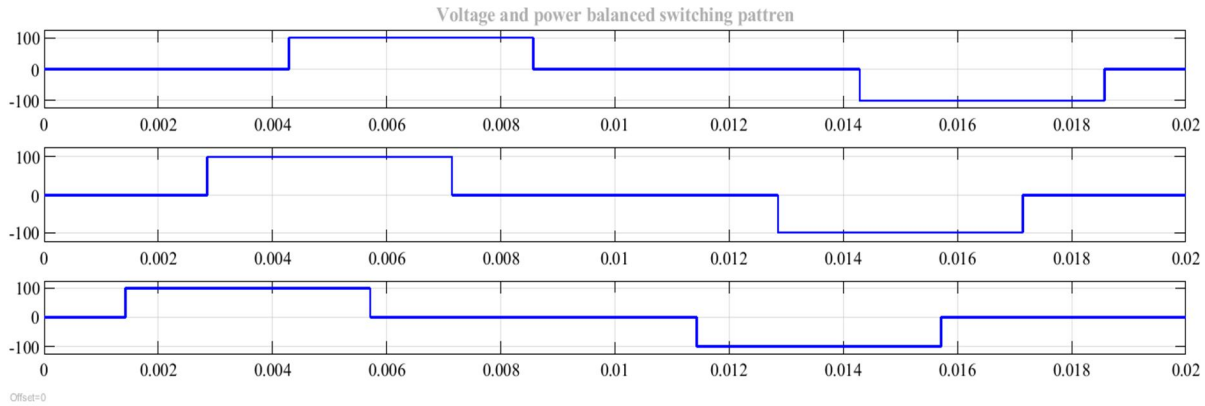


Figure 9(c): Voltage and Power Balanced Switching Pattern

Figure 9(a) depicts the conventional switching pattern for a three stage symmetric MLI. The three stages operate in unbalanced voltage and power regime.in Figure 2(b) the switching pattern balances the voltage distribution of the inverter. this feature is evident by regarding that the voltages have a different phase shift with respect to the output voltage.in figure 2(c) the switching pattern yields a balanced operation in voltage showing a two-cycle symmetry.

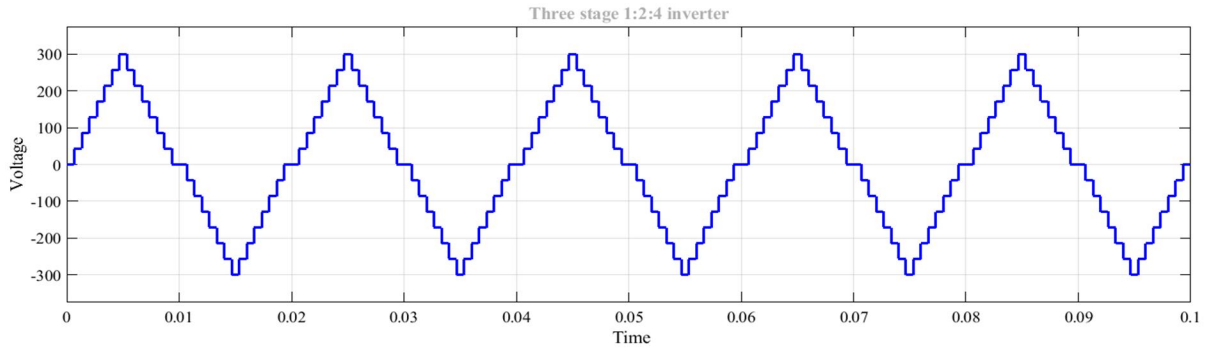


Figure 10: Asymmetric (1:2:4) 15-level Cascaded Multilevel Inverter**.**

The above waveform shows the asymmetrical binary ratio of 1:2:4. By the binary ratio formula which is stated in above we get 15-level.

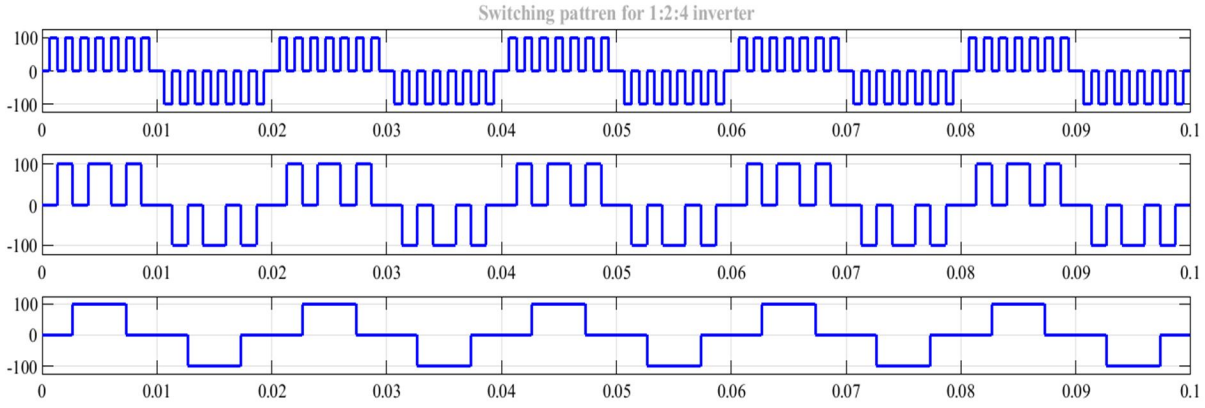


Figure 11: Switching Pattern for Asymmetric (1:2:4) 15-level Cascaded Multilevel Inverter

Figure 11 shows possible switching pattern balancing voltage and power by repeating sequence method. For three inverter stages, the asymmetric ratio 1:2:4 allows a 15-level signal. The 15-level signal yields an unbalance power distribution of 15.01%:36.03%:48.96% By ternary ratio 1:3:9 allows a 27-level signal gives deficient power distribution of 3.47%:15.14%:81.39%.

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To overcome this drawback, another asymmetric configuration has been proposed 1:1:3 allows 11-levels. Showing the power distribution of 20%:20%:60% the power balance is slightly improved at expenses of additional pulse width modulation control to get a high quality of the output signal. By 1:2:6 allows 19-level signal. And showing power distribution of 11%:22%:66%.

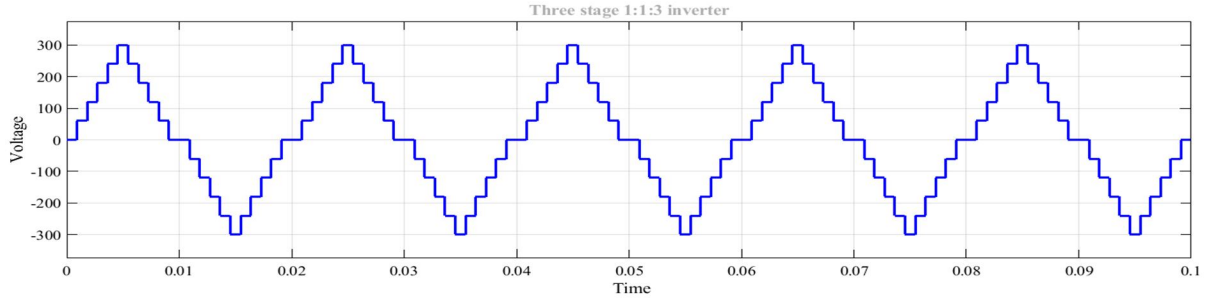


Figure 12: Asymmetric (1:1:3) 11-level Cascaded Multilevel Inverter

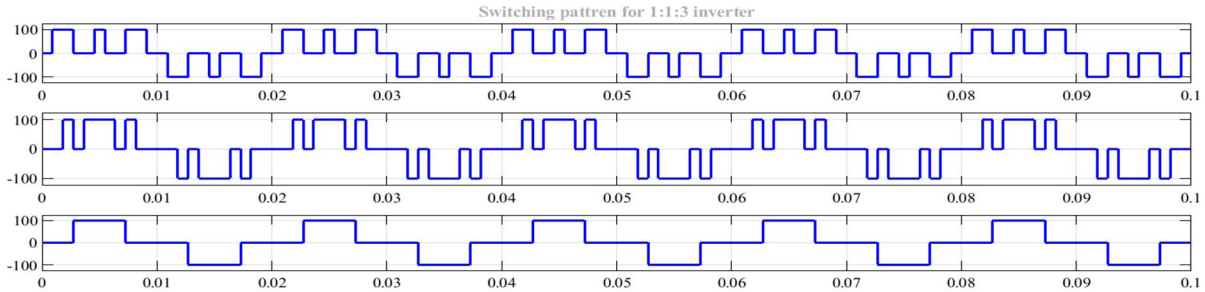


Figure 13: Switching pattern for Asymmetric (1:2:4) 11-level cascaded multilevel inverter

In transformer based MLI the use of four inverter stages is limited because of additional transformer increases the cost and size of the inverter. A symmetric relation was used in a four stage inverter producing a nine levels output signal. The asymmetric binary ratio 1:2:4:8 was used providing a 31-level output signal with some power distribution. By using ternary ratio 1:3:9:27, an 81-level signal is produced this increases the quality of output voltage. The output signals of inverter stages for binary asymmetric ratios are shown below

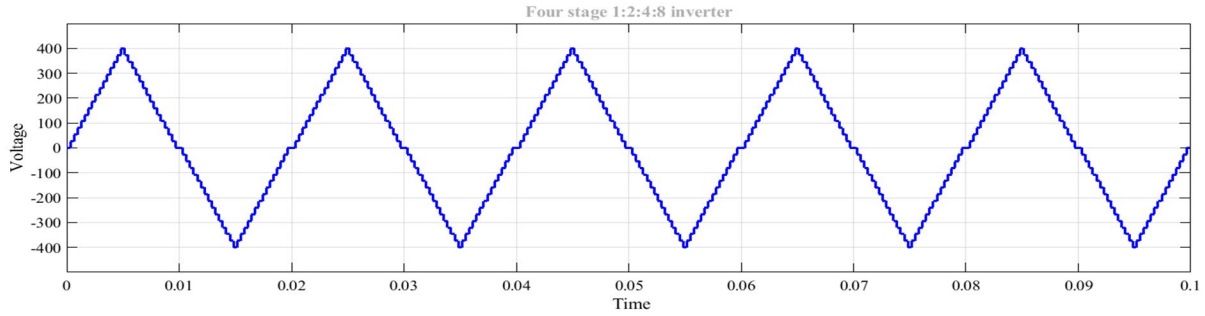


Figure 14: Asymmetric (1:2:4:8) 31-level cascaded multilevel inverter

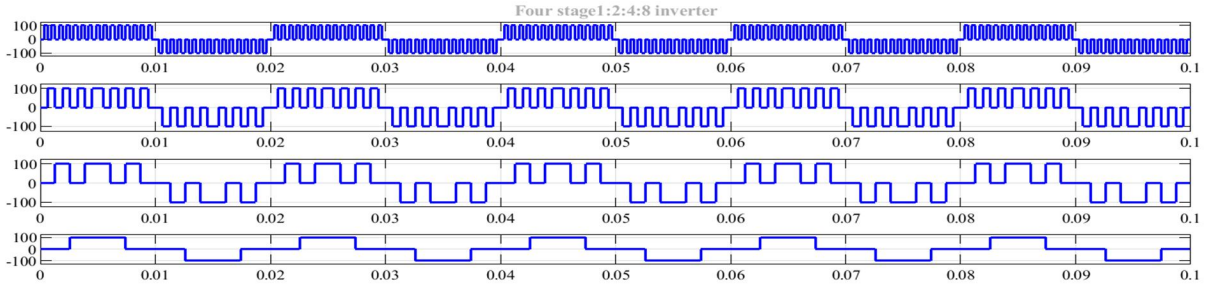


Figure 15: Switching pattern for Asymmetric (1:2:4:8) 31-level cascaded multilevel inverter

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Improving the voltage and power distribution between bridges depends on the ratio between stages. Repeating sequence method is the only way to obtain highly accurate uniform power distribution for symmetric inverters. This project presents the asymmetric ratio 6:7:8:9 for the first time in a four level cascaded multilevel inverter allows obtaining until 35-level signal. In which optimization of the switching pattern leads to a highly balanced power distribution. In order to provide regulation a signal of 31 level is selected as base or nominal , also producing 29 or 33 levels when the output voltage increase or decrease outside of a defined range in the input dc voltage or load.

II. TRANSFORMER BASED ASYMMETRICAL MULTILEVEL INVERTER

The following will give fundamentals to understand the operation and design of inverter and its components

A. Producing the Multilevel Output Signal

The output voltage of inverter for N cascaded stage is computed as

$$v_0(\omega t) = v_1(\omega t) + v_2(\omega t) + \cdots + v_N(\omega t) = \sum_{k=1}^{N} v_k(\omega t)$$

$v_k(\omega t)$ is the instantaneous output voltage of each stage which is defined as

$v_k(\omega t) = v_{dc}\, T_{Rk}\, S_{Fk}$

V_{dc} = Magnitude of DC input voltage

T_{Rk} = Turns ratio of the transformer of each k stage

S_{Fk} = Instantaneous switching function of each k stage

S_{Fk} takes the values -1, 0, 1.

$\theta_{m} = \sin^{-1}(2m-1/2M)$

θ_m determines the end of the m interval and starting point of the following interval, so it can expressed in radians for m = 1, 2, 3 …M. then, each level is defined for interval $[\theta_m, \theta_{m+1}]$. The output signal building based on θ_m angles is shown in below table.

Table 1
Optimized Switching Function

Level	Interval start angle	Interval end angle
0	…	θ_1
1	θ_1	θ_2
…	…	…
M-1	θ_{M-1}	θ_M
M	θ_M	$\pi - \theta_M$
M-1	$\pi - \theta_M$	$\pi - \theta_{M-1}$
…	…	…
1	$\pi - \theta_2$	$\pi - \theta_1$
0	$\pi - \theta_1$	$\pi + \theta_1$
-1	$\pi + \theta_1$	$\pi + \theta_2$
…	…	…
-(M-1)	$\pi + \theta_{M-1}$	$\pi + \theta_M$
-M	$\pi + \theta_M$	$2\pi - \theta_M$
-(M-1)	$2\pi - \theta_M$	$2\pi - \theta_{M-1}$
…	…	…
-1	$2\pi - \theta_2$	$2\pi - \theta_1$
0	$2\pi - \theta_1$	θ_1
1	θ_1	θ_2
…	…	…

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B. THD and RMS as Functions of Number of Integer Levels

As the number of levels increases we have to obtain lower harmonic distortion mean while greater amount of stages is also required in the inverter. The RMS (root mean square) value of the output signal of the inverter also depends on the number of levels but in a smaller manner. To get the quality of the waveform THD and RMS values are play important role

$$V_0 = \frac{V_{max}}{M}\sqrt{\left(M^2 - \frac{2}{\pi}\sum_{m=1}^{M}(2m-1)\theta_m\right)}$$

Where $\theta_m = \sin^{-1}\left(\frac{2m-1}{2M}\right)$

The output signal expressed in fourier series expansion as

$v_{0(\omega t)} = \sum_{n=1}^{\infty}\left(a_n \cos(n\omega t) + b_n \sin(n\omega t)\right)$

Considering odd symmetry

$v_{0(\omega t)} = b_1 \sin \omega t + \sum_{n=2}^{\infty} b_n \sin n\omega t$

$b_1 \sin \omega t = v_{01(\omega t)}$

$\sum_{n=2}^{\infty} b_n \sin n\omega t = v_{0h(\omega t)}$

$v_{01(\omega t)}$ and $v_{0h(\omega t)}$ are the fundamental and harmonic components of voltage

$V_{01(\omega t)} = \frac{4V_{max}}{\pi M}\sum_{m=1}^{M}\cos\theta_m$

The RMS value is

$V_{01_{Rms}} = \frac{4V_{max}}{\sqrt{2}\,M\pi}\sum_{m=1}^{M}\cos(\theta_m)$

To determine THD

$$\text{THD} = \frac{v_{0h_{Rms}}}{v_{01_{Rms}}} = \sqrt{\left(\frac{v_{0h_{Rms}}}{v_{01_{Rms}}}\right)^2 - 1}$$

As it can be noted, the THD is not dependent on the input voltage Vdc or the transformer ratios TR_k.

C. Turns Ratio of Transformer

$TR_k = \frac{W_k V_{max}}{M V_{dc}}$

V_{max} can be obtained as the algebraic sum of the state output voltages

M is positive integer levels

W_k defines ratio between stages ($w_1 : w_2 : w_3 : w_4$)

V_{dc} is the input voltage

For example take four stage 1:2:4:8 asymmetric binary ratio that means 31-level

w_1=1, w_2=2, w_3=4, w_4=8

M=15

$V_{dc} = 100$

$TR_1 = \frac{W_1 V_{max}}{M V_{dc}} = \frac{1*400}{15*100} = \frac{4}{15}$

$TR_2 = \frac{W_2 V_{max}}{M V_{dc}} = \frac{2*400}{15*100} = \frac{8}{15}$

$TR_3 = \frac{W_3 V_{max}}{M V_{dc}} = \frac{4*400}{15*100} = \frac{16}{15}$

$TR_4 = \frac{W_4 V_{max}}{M V_{dc}} = \frac{8*400}{15*100} = \frac{32}{15}$

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III. SYNTHESIS OF SWITCHING PATTREN

The asymmetrical relation uses $w_k \in N$, the selection of $w_k$implies finding a relation between the levels in the stages that allows entire signal levels through the algebraic sum of them but also providing redundancy for optimization.

A. Redundancy Signal Levels

The all stages of inverter fed by a single dc source, so the voltage stress in semiconductor of all stages is same. So as to secure similar current stress rating in semiconductor device we goes for consecutive integer weights. $w_k = w, w+1, w+2, w+3$ to get a half of cycle of M level signal, by changing the value of w we can find more than one solution that presents all voltage levels in interval of zero and M . this is how we apply the redundancy to get the levels. For M=15 redundancy in values defined by $\{w, w \in N : 3 \leq w \leq 7\}$.

For weight w=4 (4:5:6:7) promote a great redundancy in the lower levels, which have lower duration for voltage waveform. Using w=5 (5:6:7:8) for all levels distributed redundancy is found for w= 6 (6:7:8:9) for the two more levels redundancy is obtained ,which is major duration in voltage waveform. For w=7 (7:8:9:10) the 13th level is not getting at the highest level there is no redundancy.

For lower values of w the number of possible switching pattern is higher. The missing of redundancy in the maximum level decreases the possibility to achieve a balanced power distribution between stages. By choosing w=6, it is possible to obtain 16 and 17.

B. Power Distribution among Stages

The average power for each stage as follows

$$\bar{P}_k = \frac{I_{max} V_{k1max}}{2} \cos\varphi$$

Mean value of total power is

$$\bar{P} = \sum_{k=1}^{4} \bar{P}_k = \frac{I_{max} V_{max}}{2} \cos\varphi$$

The best power distribution among the stages of inverter is obtained when powers $\bar{P}_k$ are equal. An ideal distribution being obtained when these values are 25% for four stages.

$$\frac{\bar{P}_k}{\bar{P}} = \frac{V_{k1max}}{4V_{max}} \times 100\%\text{X}$$

Table 2
Switching Functions of the Inverter Stages for Selected Ratio

Positive level	Stage 1 (w_1 = 6)	Stage 2 (w_2 = 7)	Stage 3 (w_3 = 8)	Stage 4 (w_4 = 9)
0	0	0	0	0
	1	-1	-1	1
	-1	1	1	-1
1	-1	1	0	0
	0	-1	1	0
	0	0	-1	1
2	-1	0	1	0
	0	-1	0	1
	-1	1	-1	1
3	-1	0	0	1
4	1	1	0	-1
	-1	-1	1	1
5	1	1	-1	0

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	1	0	1	-1
6	1	0	0	0
	0	1	1	-1
7	0	1	0	0
	1	-1	1	0
	1	0	-1	1
8	0	0	1	0
	1	-1	0	1
	0	1	-1	1
9	0	0	0	1
	-1	1	1	0
10	-1	1	0	1
	0	-1	1	1
11	-1	0	1	1
12	1	1	1	-1
13	1	1	0	0
14	1	0	1	0
	1	1	-1	1
15	1	0	0	1
	0	1	1	0
16	0	1	0	1
17	0	0	1	1

For each possible switching sequence, we can compute this percentage for all inverter stages. For selected switching pattern, the distribution of output power of 100w among four stages is $P_1 = 40W$, $P_2 = 15W$, $P_3 = 25W$, $P_4 = 20W$ the ideal distribution of power is $P_k = \frac{100W}{4} = 25W$ which corresponds to a 25% of total power. Only P_3 has no error since the other stage powers are lower or higher compared to ideal distribution of power. P_1 has a deviation from ideal distribution to a 60% (15W/25W), stage P_2 has deviation of 40% (10W/25W), state P_4 has deviation of 20% (5W/25W).

The proposed ratio 6:7:8:9 allows 31 level signal like 1:2:4:8 asymmetric binary ratio. It was advantage in balancing power distribution. The number of commutations in case of ratio 1:2:4:8 is lower than in proposed case. Using the proposed ratio, the system has capability to operate with three or two sources and PWM control which is possible in case of binary ratio. The power distribution is optimum in proposed case and deficient in case of binary relation.

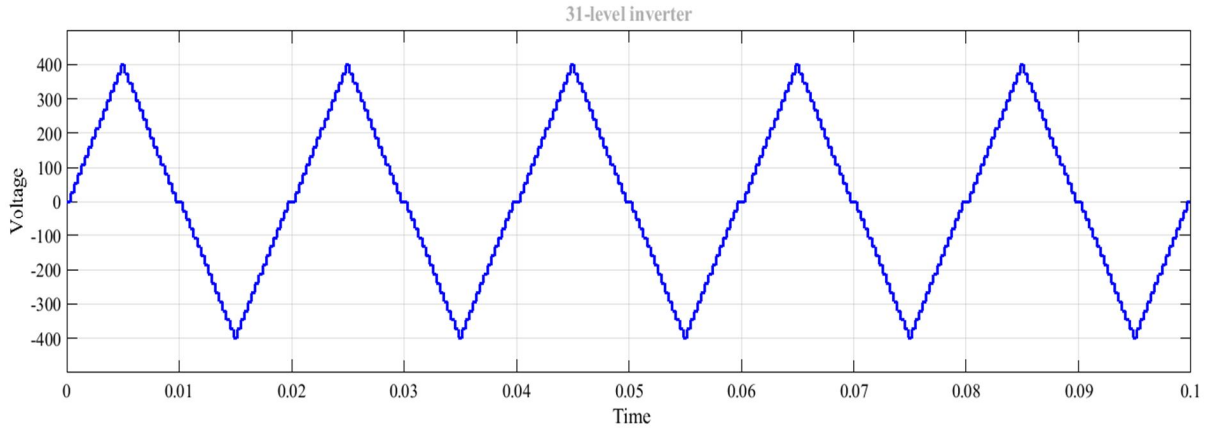


Figure 16: Optimum Voltage Signal of 31- level Inverter (6:7:8:9)

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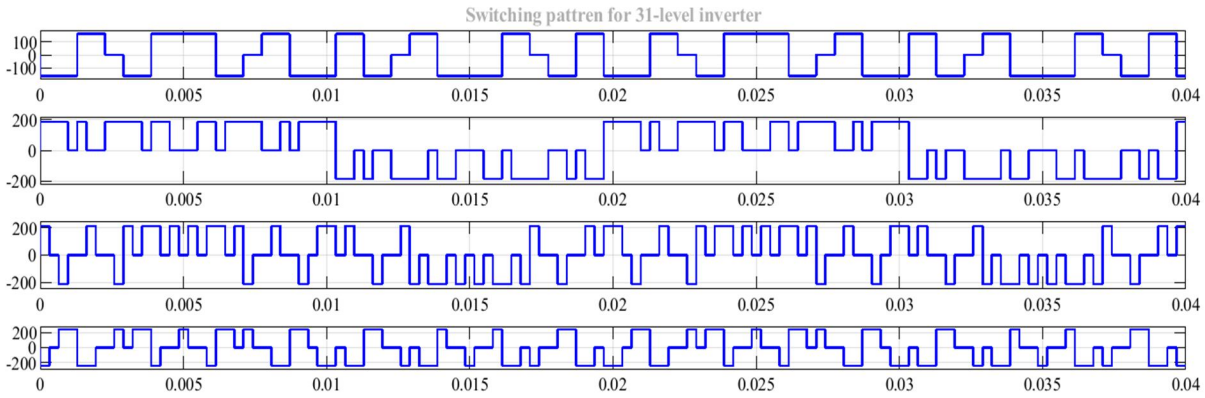


Figure 17: Optimum Switching Pattern Producing 31-levels Signal

By using optimum switching pattern corresponding to produce between 27 and 35 levels. As higher the quality of output signals, higher the number of levels.

Below figure presents the optimized switching pattern for balanced power distribution when the inverter operates generating an output signal of 29-level.

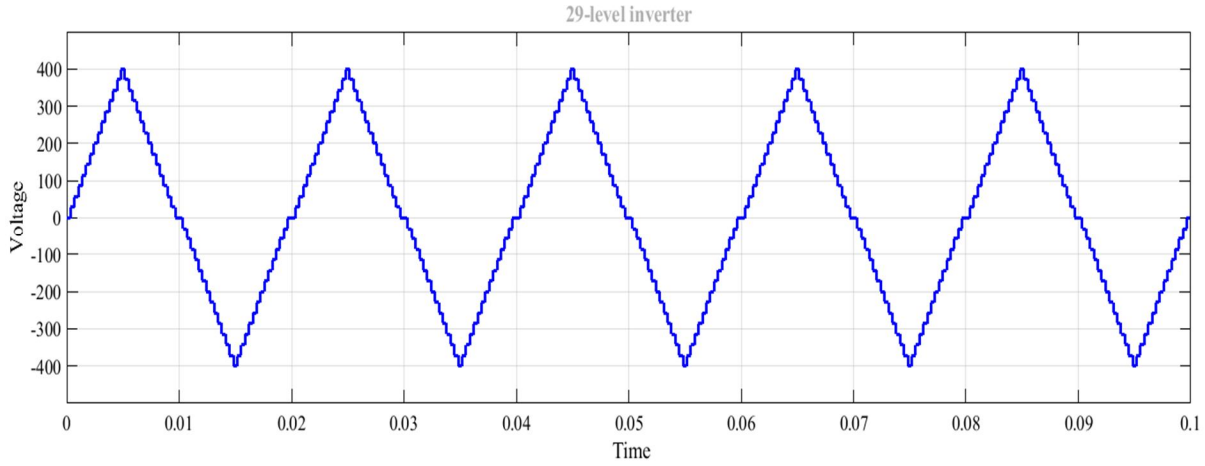


Figure 18: Optimum Voltage Signal of 29- level Inverter (6:7:8:9)

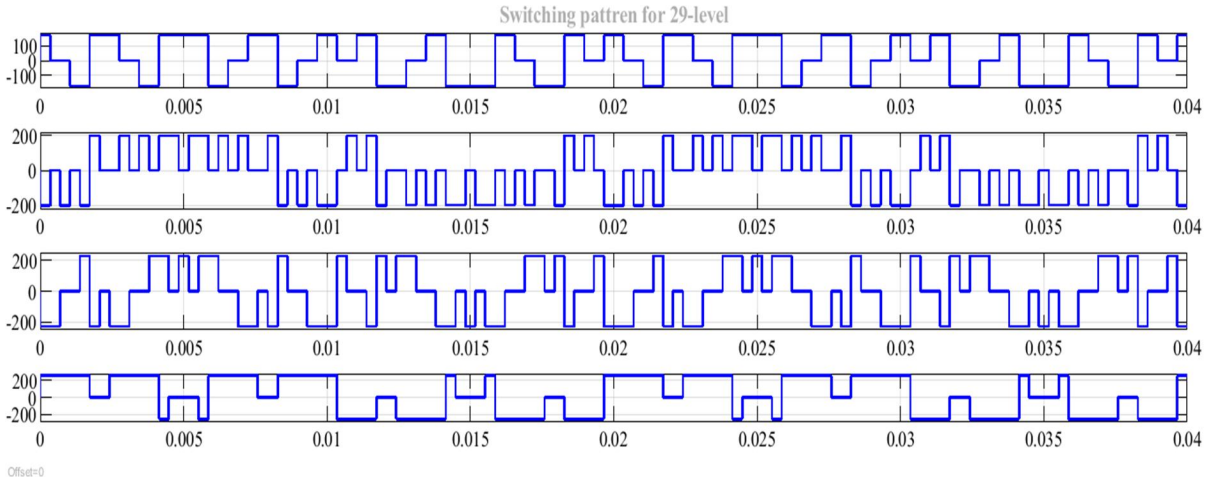


Figure 20: Optimum Switching Pattern Producing 29-levels Signal

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Below figure presents the optimized switching pattern for balanced power distribution when the inverter operates generating an output signal of 33-level

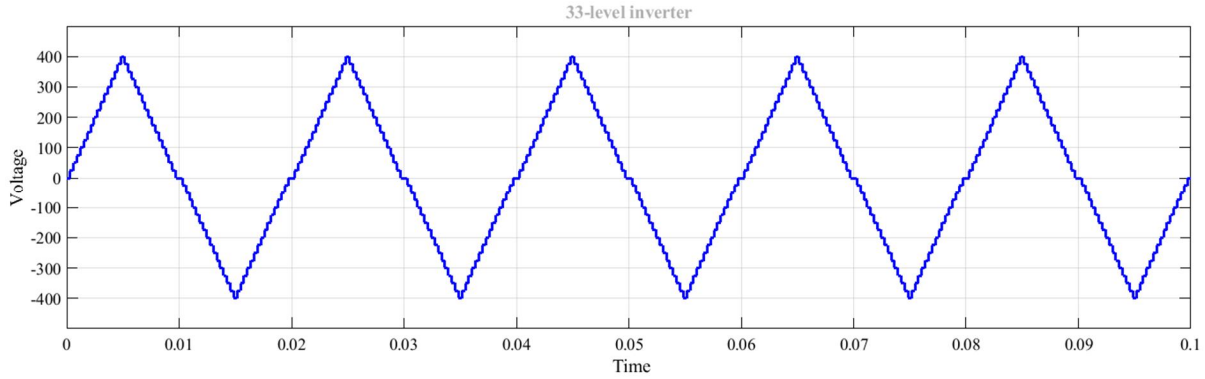


Figure 19: Optimum Voltage Signal of 33- level Inverter (6:7:8:9)

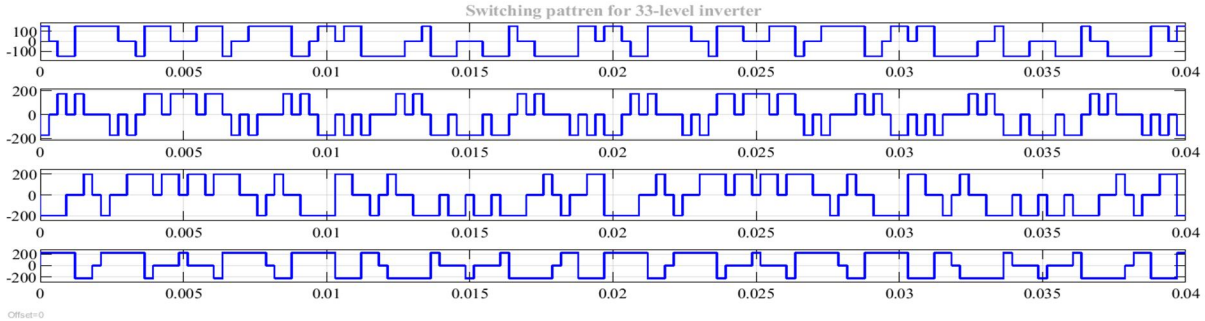


Figure 20: Optimum Switching Pattern Producing 33-levels Signal

Below figure presents the optimized switching pattern for balanced power distribution when the inverter operates generating an output signal of 35-level

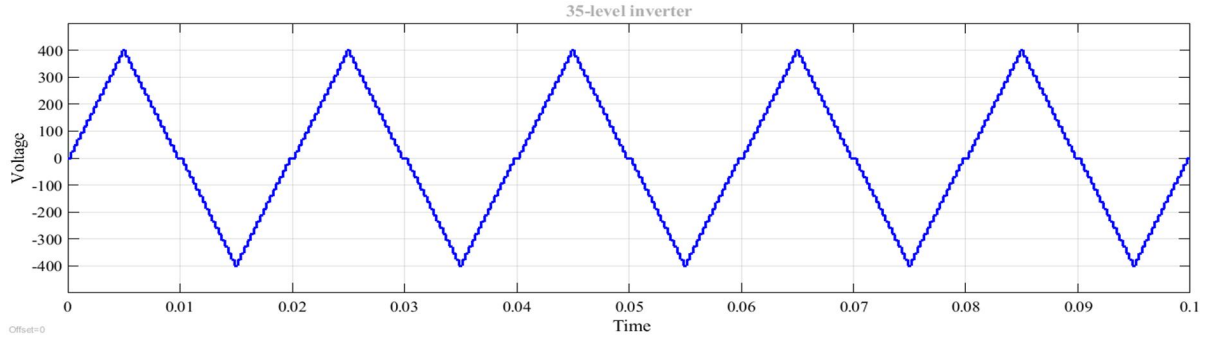


Figure 21: Optimum Voltage Signal of 35- level Inverter (6:7:8:9)

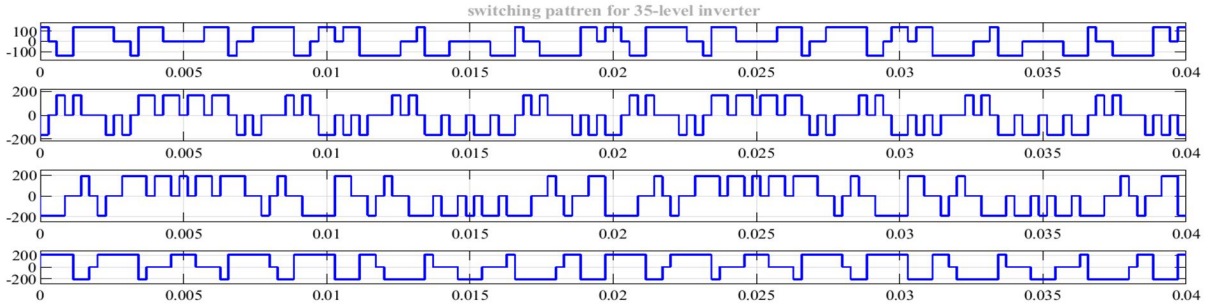


Figure 22: Optimum Switching Pattern Producing 35-levels Signal

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C. SHEPWM Technique

Selective harmonic elimination pulse width modulation is implemented for harmonic elimination in multilevel inverters. SHEPWM is a eminent technique for switching pulse generation. SPWM method is very effective for observing the inverter output current but this method can cause high switching loss due to high switching frequency. SHEPWM is the more effective method to eliminate low-order harmonics and subjected to a low switching frequency. It improves output power quality and reduces the cost of filter. Switching angle equation is a set of nonlinear transcendental equations. Some methods like Newton-rapson (N-R method), Walsh functions and Block-pulse functions are involved in the harmonic minimization process in multilevel inverter SHEPWM. All this methods have its own disadvantages to solve this harmonic problem. N-R method requires initial guess, and divergence problem gives no optimum solution. Walsh function and Black-pulse function only solve linear equations, in the case of nonlinear transcendental equations, are difficult to find better switching result. The method requires proper initial guess to converge to a proper solution. Recently, non-traditional methods based on evolutionary algorithms, such as Particle Swarm Optimization (PSO) have been employed for inverter harmonic elimination.

In this concept, an improved Particle Swarm Optimization (PSO) approach can be programmed in the SHEPWM method to solve transcendental equation of switching angles. The proposed method can compute the optimal solution of switching angles to eliminate the low order harmonics and minimize the THD value as compared to Genetic Algorithm (GA). With the proposed method, the required switching angles are computed efficiently by improved PSO. Selective harmonic elimination method is used for the computation of switching angles

Selective harmonic elimination method is used for the computation of switching angles

$V_{0(t)} = \frac{a_0}{2} + \sum_{i=0}^{n} a_n \cos\left(\frac{2\pi nt}{T}\right) + b_n \sin\left(\frac{2\pi nt}{T}\right)$

a_0 *represents* the dc term

a_n Represents the even harmonic

b_n Represents the odd harmonic

In this SHEPWM technique, firing angles $(\theta_1, \theta_2, \theta_3, \dots \dots \dots \dots \dots \theta_m)$ are calculated using the formula of

$\theta_m = \sin^{-1}\left(\frac{2m-1}{2M}\right)$ (10)

where m = 0, 1,…..M

M is the highest positive level

By maintaining the relationship of $(0 < \theta_1 < \theta_2, \dots, < \theta_m < \pi/2)$

The simulation is accomplished for 11-level and 35-level. By selective harmonic elimination [SHEPWM] technique we got THD value low compared to the repeating sequence method which is stated in above [25].

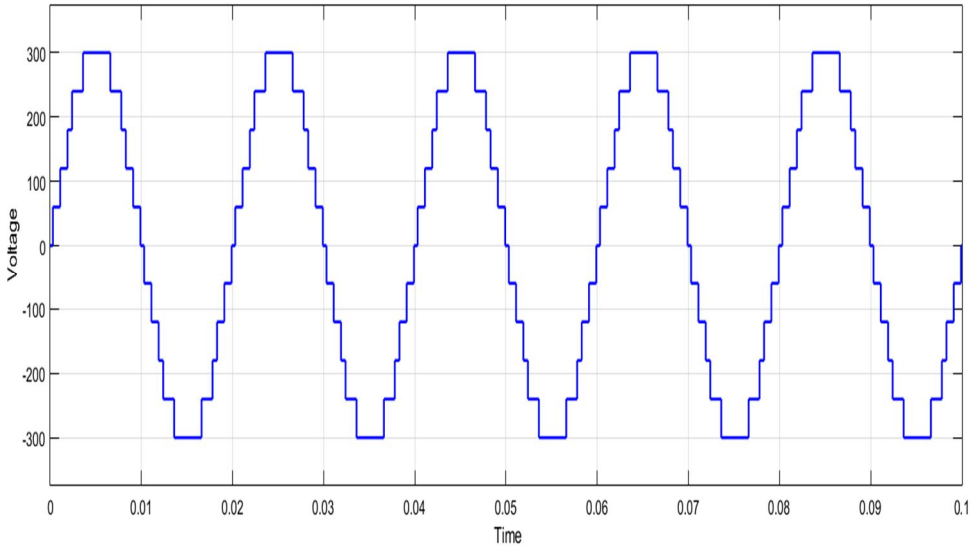


FIGURE 23: Asymmetric (1:1:3) 11-level Cascaded Multilevel Inverter by SHEPWM Technique.

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From equation (10)

$$\theta_1 = \sin^{-1}\left(\frac{(2*1)-1}{2*5}\right) = 5.739^0$$

$$\theta_2 = \sin^{-1}\left(\frac{(2*2)-1}{2*5}\right) = 17.457^0$$

$$\theta_3 = \sin^{-1}\left(\frac{(2*3)-1}{2*5}\right) = 30^0$$

$$\theta_4 = \sin^{-1}\left(\frac{(2*4)-1}{2*5}\right) = 44.42^0$$

$$\theta_5 = \sin^{-1}\left(\frac{(2*5)-1}{2*5}\right) = 64.15^0$$

The above waveform generates 11-level at the output. With 11 levels, four harmonics can be eliminated. Several combinations of these four harmonic orders can be made to be eliminated. Generally, lower order harmonic orders are eliminated. But in this case $3^{rd}, 5^{th}, 7^{th}, 9^{th}$ order harmonics are chosen to eliminate from the output voltage waveform

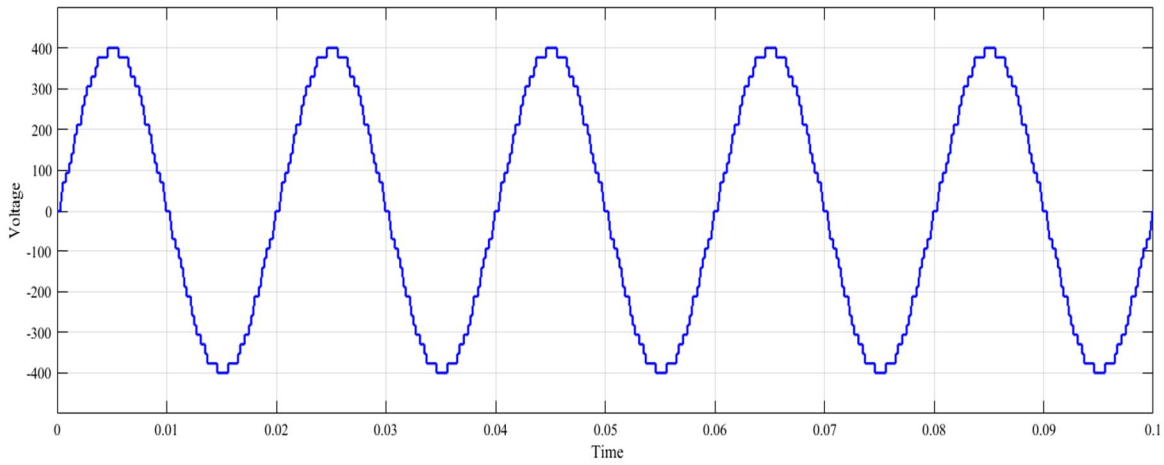


Figure 24: Optimum Voltage Signal of 35- level Inverter (6:7:8:9) by SHEPWM Technique.

The above waveform generates 35-level at the output. With 11 levels, sixteen harmonics can be eliminated. Several combinations of these sixteen harmonic orders can be made to be eliminated. Generally, lower order harmonic orders are eliminated. But in this case$3^{rd}, 5^{th}, 7^{th}, 9^{th}, , 11^{th}, , 13^{th}, , 15^{th}, , 17^{th}, , 19^{th}, 21^{th}, 23^{th}, 25^{th}, 27^{th}, 29^{th}, 31^{th}, 33^{th}$ order harmonics are chosen to eliminate from the output voltage waveform

Table 3
Parameter Table for Three Stages

PARAMETER	VALUE
Input voltage	300V
Output voltage(RMS)	212.13V
Peak voltage	300V
Load resistor	100Ω
Time period	0.02Sec
Frequency	50Hz

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Table 4
Comparison of Different Levels Using Switches

S.NO	NUMBER OF LEVELS	SYMMETRIC CONFIGURATION	ASYMMETRIC CONFIGURATION
1.	5-LEVEL	8 SWITCHES	8 SWITCHES
2.	7-LEVEL	12 SWITCHES	8 SWITCHES
3.	9-LEVEL	16 SWITCHES	8-SWITCHES
4.	11-LEVEL	20-SWITCHES	12-SWITCHES
5.	15-LEVEL	28-SWITCHES	12-SWITCHES
6.	19-LEVEL	36-SWITCHES	12-SWITCHES
7.	27-LEVEL	52-SWITCHES	12-SWITCHES
8.	29-LEVEL	56-SWITCHES	16-SWITCHES
9.	31-LEVEL	60-SWITCHES	16-SWITCHES
10.	33-LEVEL	64-SWITCHES	16-SWITCHES
11.	35-LEVEL	68-SWITCHES	16-SWITCHES

IV. CONCLUSION

This project presents the method to enforce balanced power distribution on a transformer based cascaded multilevel inverter. The method is found on the selection of optimal switching pattern for each stage of the inverter. The proposal has developed using a 31 level output voltage signal obtained from a four stage common dc source inverter after selecting the best combination of integer weights for the stages of the inverter.

The proposed asymmetric ratio 6:7:8:9 allows the inverter can be controlled using optimized switching patterns for a subsequent number of levels (27, 29, 31, 33, 35).

A new multilevel inverter topology is studied which uses less number of switches than the conventional inverter topology and hence the possibility of producing higher number of level with same switches as in conventional topology is made. The harmonic content is reduced by using a new repeating sequence method and pwm control, which basically changes the step angle of each level so as to resemble to the sine waveform. The switching sequence multilevel inverter is designed to generate 35-level waveform from Asymmetrical turns ratio is performed using MATLAB. The results are compared and proved that with the proposed topology the harmonic content is reduced.

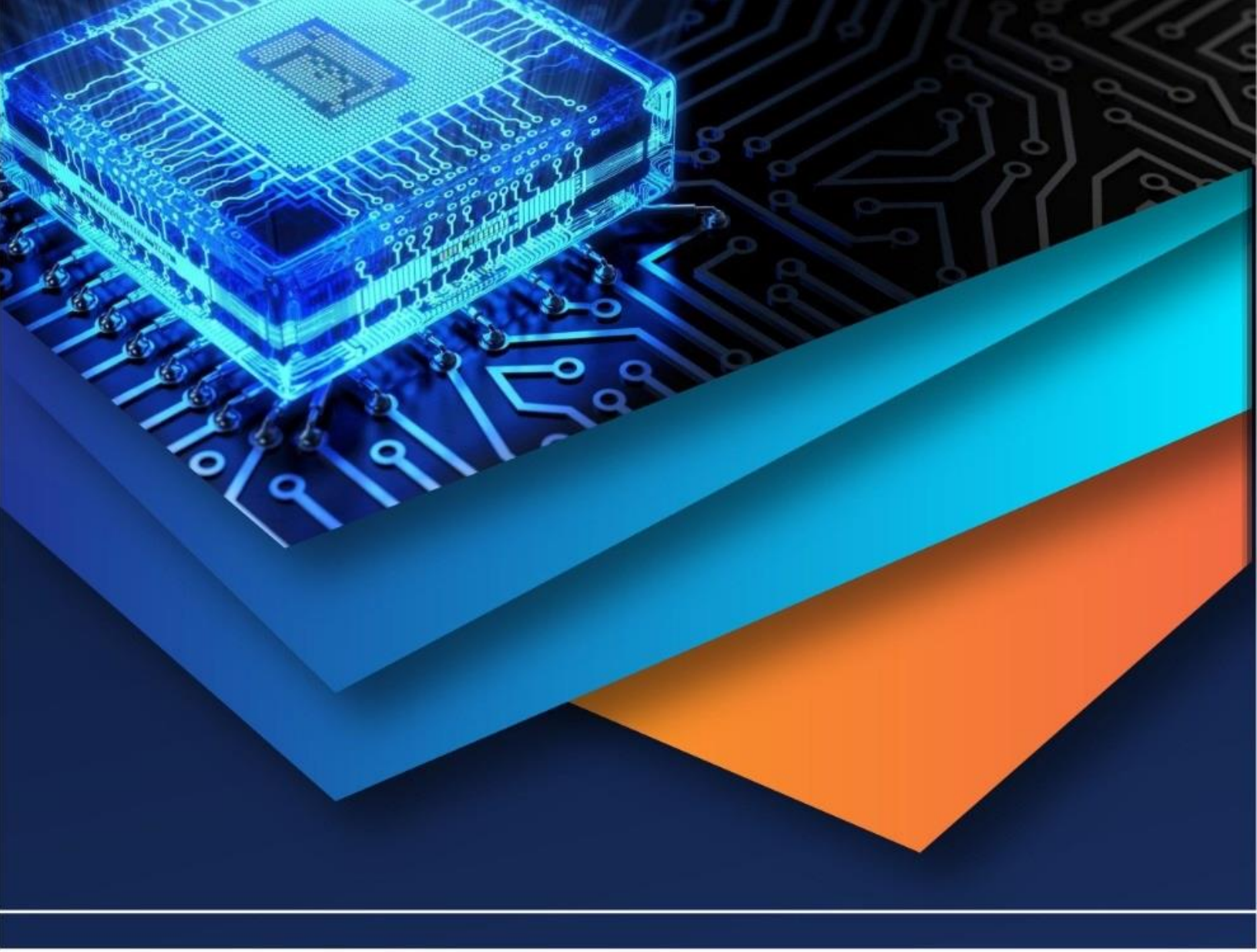
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