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Transmission Gate Based 8T SRAM Cell for Biomedical Applications

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Abstract: ***There is an immense necessity for several kB of embedded memory for Biomedical systems which typically operate in the sub-threshold domain with perfect efficiency. SRAMS dominates the total power consumption and the overall silicon area, as 70% of the die has been occupied by them. This brief proposes the design of a Transmission gate-based SRAM cell for Biomedical applications eliminating the use of peripheral circuitry during the read operation. This topology offers a smaller area, reduced delay, low power consumption, and improved data stability in the read operation. Static Random Access Memories mostly contribute to the performance, area, and power dissipation of digitally integrated systems.***
The mentioned implantable and wireless applications require low-power circuits operating for a long time, occupying less area without degrading the performance, as it provides inconvenience and may even be risky especially while considering the implantable devices.

I. INTRODUCTION

Static random-access memory is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance but is still volatile in a conventional sense, that data is eventually lost when memory is not powered. The continuous scaling down of bulk CMOS creates major issues due to its base material. The primary obstacles to the scaling of bulk CMOS to 32nmgatelengths include short channel effects Sub-threshold leakage gate-dielectric leakage and device-to-device variations. Due to the sudden increase in threshold voltage ie. Vt oscillation produced by overall and general process variations occur in ultra-short channel devices, 6T SRAM cell and their modifications cannot be operated at advance scaling of supply voltages without functional and parametric failure causing yield loss. The design of a standard 6T SRAM cell undergoes a lot of problems with write delay. The design of Low power 6T SRAM cell could decrease the write power and access delay but could not improve their stability. In deep submicron ranges, none of the earlier works has studied about the improvement of variability in SRAM cells at the schematic level.

II. EXISTING SRAM'S

In SRAMS, the memory cell is a basic element as it occupies a significant portion of the area. Implementation of the 6T SRAM cell is very simple as depicted in Fig 1. The cell is well structured with two pass transistors and two cross-coupled inverters. The two cross-coupled inverters form a simple latch capable of accumulating one bit of the data. The two Pass transistors are connected with the two complementary types of Bit Lines (BL and BL Bar) and a Word Line (WL), providing a connection between the cell and the outside world. SRAMS usually operates in three states namely Read, Write, and Hold.

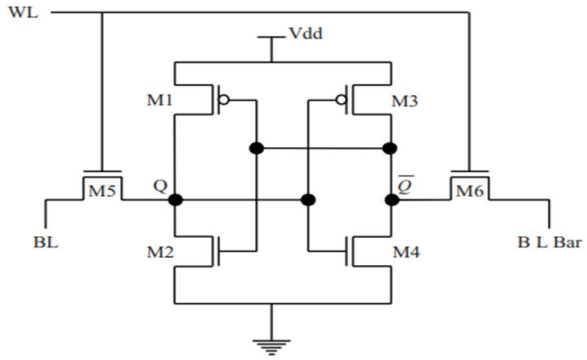


Figure 1: 6T SRAM cell

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The Conventional 6T SRAM cell declines in various conditions such as read stability due to the conflict between Pull up or Pull down and the access transistors and Variability i.e. less reliable in Submicron technology due to the process parameters variations. To overwhelm these issues various cells have been designed which started with the 8T SRAM cell design as given in Fig 2.
The cell comprises a decoupled read path With two extra nmos transistors to eradicate the read disturb issue. But, it suffers from the leakage problem due to the added transistors relying on the information stored in the cell.

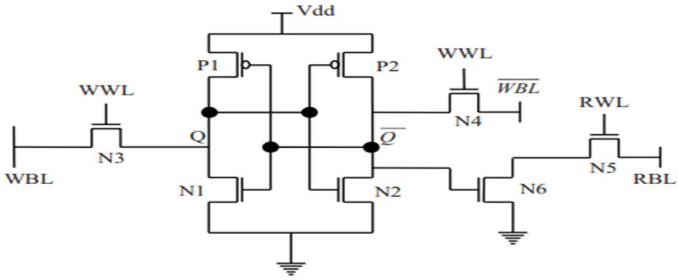


Figure 2: 8T SRAM cell

In order to solve the leakage problem many other cells have been designed. A recent work was proposed in as shown in Fig 3. (referred to as 10T-E1) which includes a pmos transistor at the read path reducing the leaking current passing through the M6 transistor. But the design at the same time also causes to the flow of leaking current from the node into the RBL which thereby leads to the reduction of sensing margin and is also data dependent.

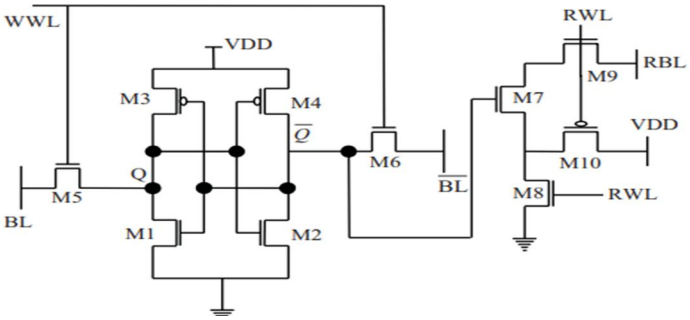


Figure 3: 10T-E1 SRAM cell

10T-E1 is modified in by designing the SRAM cells with NMOS-only based read ports as depicted in Fig 4 and Fig 5(referred to as 10T-E2 and 10T-E3). These designs use a separate read port consisting of four NMOS transistors (R1, R2, R3, and R4) to perform the read functionality.
The isolated read ports in both the designs cause a destruction-free read operation with better read stability. Bit Line Leakage is also improved in such cases as the separated read port uses a stack of transistors. But Fig 4 is still data dependent whereas Fig 5 maintains a complete data-independent leakage path.

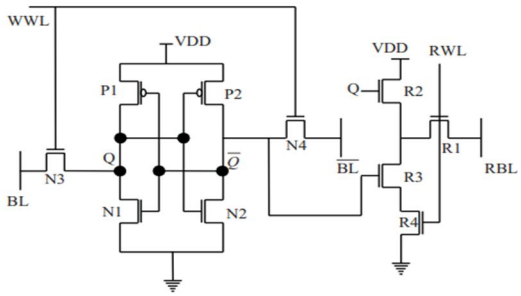


Figure 4: 10T-E2 SRAM cell

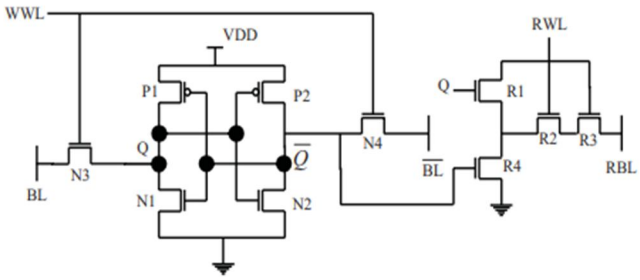


Figure 5: 10T-E3 SRAM cell

III. PROPOSED WORK

A. Proposed Transmission Gate Based 8t Sram Cell

The existing cells succeed in improving the read stability but at the cost of an increase in area as they require more number of transistors to do so. However, for many applications such as Biomedical and Wireless, area occupancy also plays a vital role. If considered in Biomedical Implants, less area occupancy of the device inside the body provides less invasive to the human body.

In view of such an issue related to the SRAM design, this brief presents a Transmission gate based 8T SRAM cell as shown in Fig 1. This design reduces the area occupancy by eliminating the peripheral circuitry.

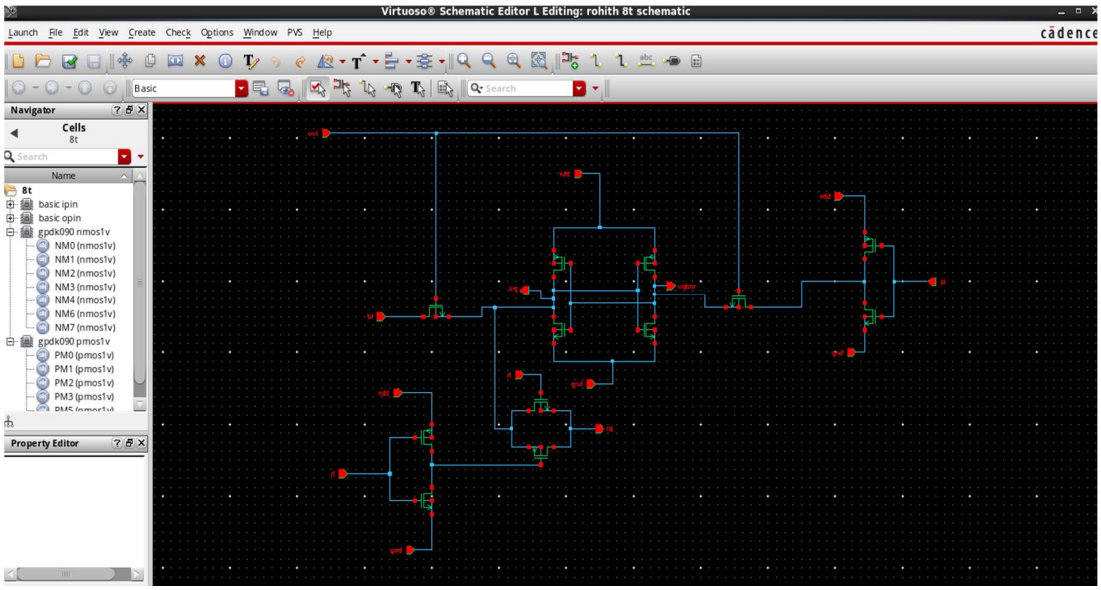


Figure 1: Proposed Transmission Gate Based 8T SRAM Cell

The proposed design chiefly concentrates on the read operation, which in the existing designs exclusively instills on the peripheral circuits. The Write operation is homogeneous to the Conventional and the other SRAM cells.

The Write functionality is controlled by the Word Line (WWL). The content which we are inclined to write is given to the Bit Lines BL and BL Bar. Now, the enabled Word Line, making the access transistors active, allows the data of the Bit Lines to intrude into the memory cell. The intruded data will thus be cached into the two storage nodes WQ and WQ Bar.

IV. EXPERIMENTAL RESULTS

The tools used are Cadence Virtuoso and the technology used is 45nm.

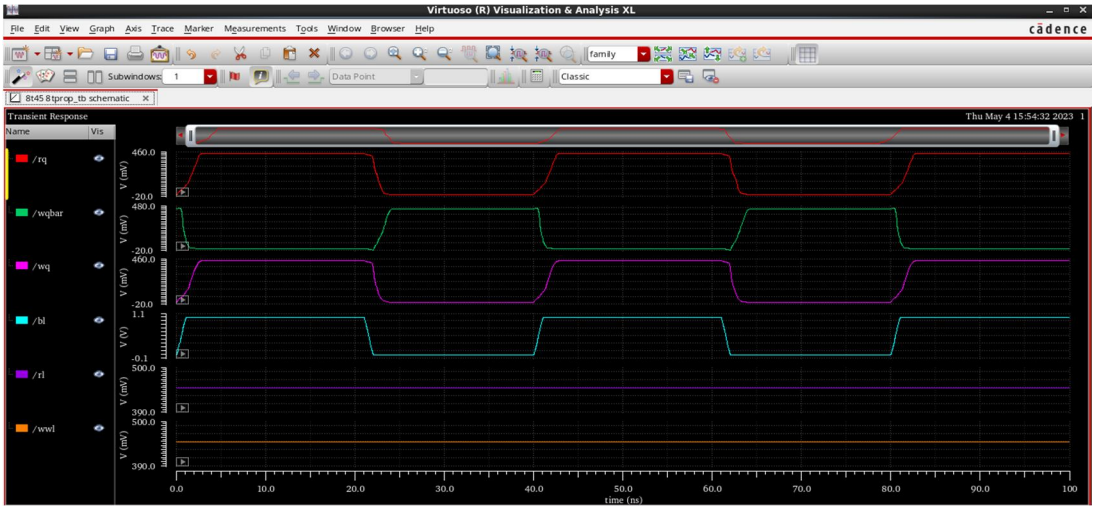


Figure 2: TG-8T SRAM simulation result using 45nm technology

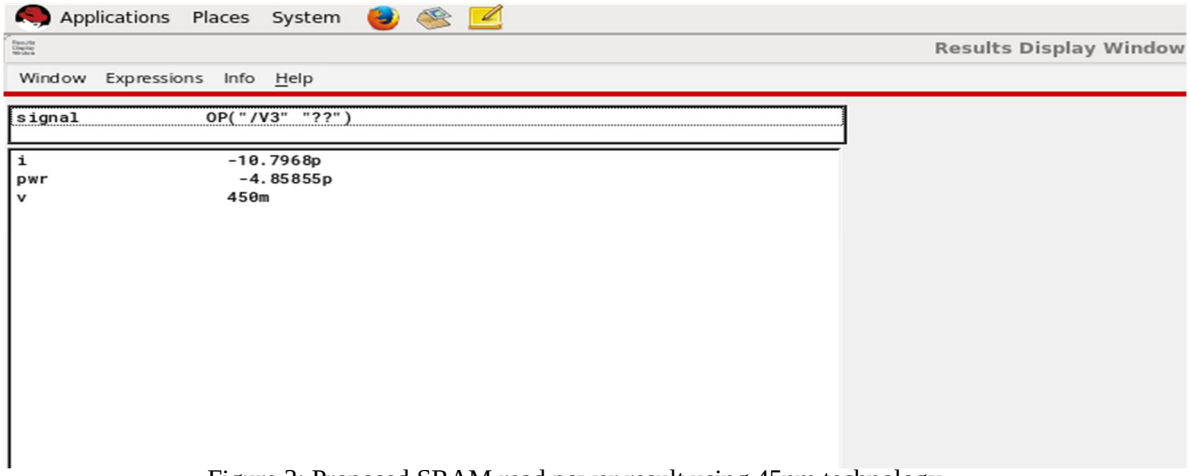


Figure 3: Proposed SRAM read power result using 45nm technology.

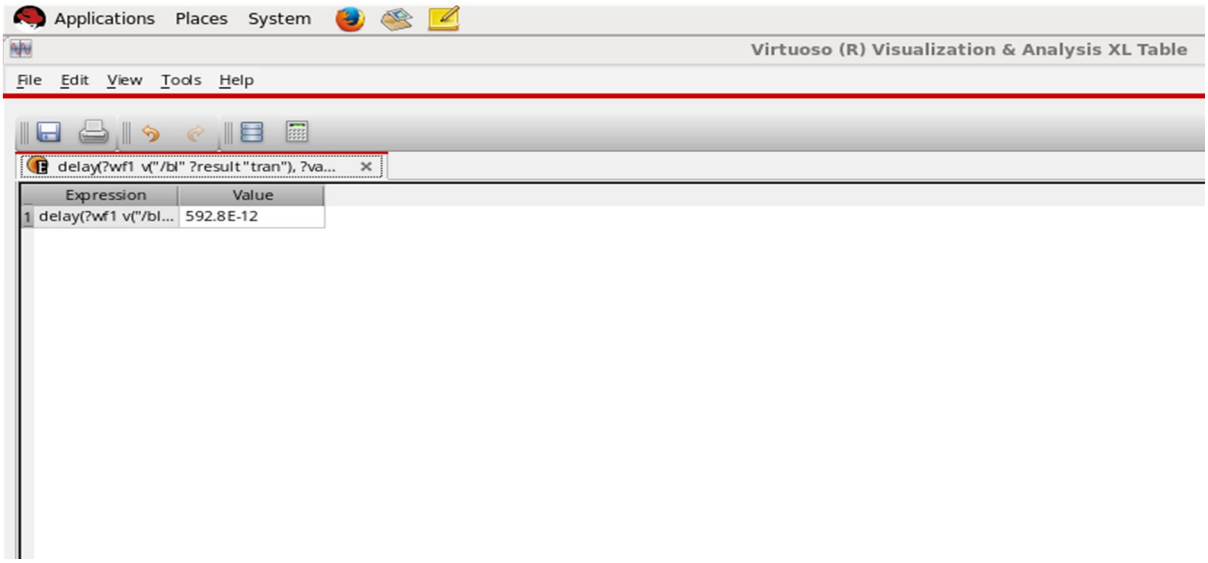


Figure 3: Proposed SRAM delay result using 45nm technology.

V. ANALYSIS OF RESULT

Results mainly contains information regarding performance analysis of different parameters of SRAM's.

Using 45nm Technology.

	C6T	8T	10T-E1	10T-E2	10T-E3	8T-P
Technology	45	45	45	45	45	45
Supply (mv)	450	450	450	450	450	450
Read Power (w)	112.2n	19.84n	12.74n	12.73n	12.74n	4.8585p
Read Delay (s)	0.3106 µ	0.077 µ	0.0756 µ	0.0629 µ	0.0775 µ	592.8E12

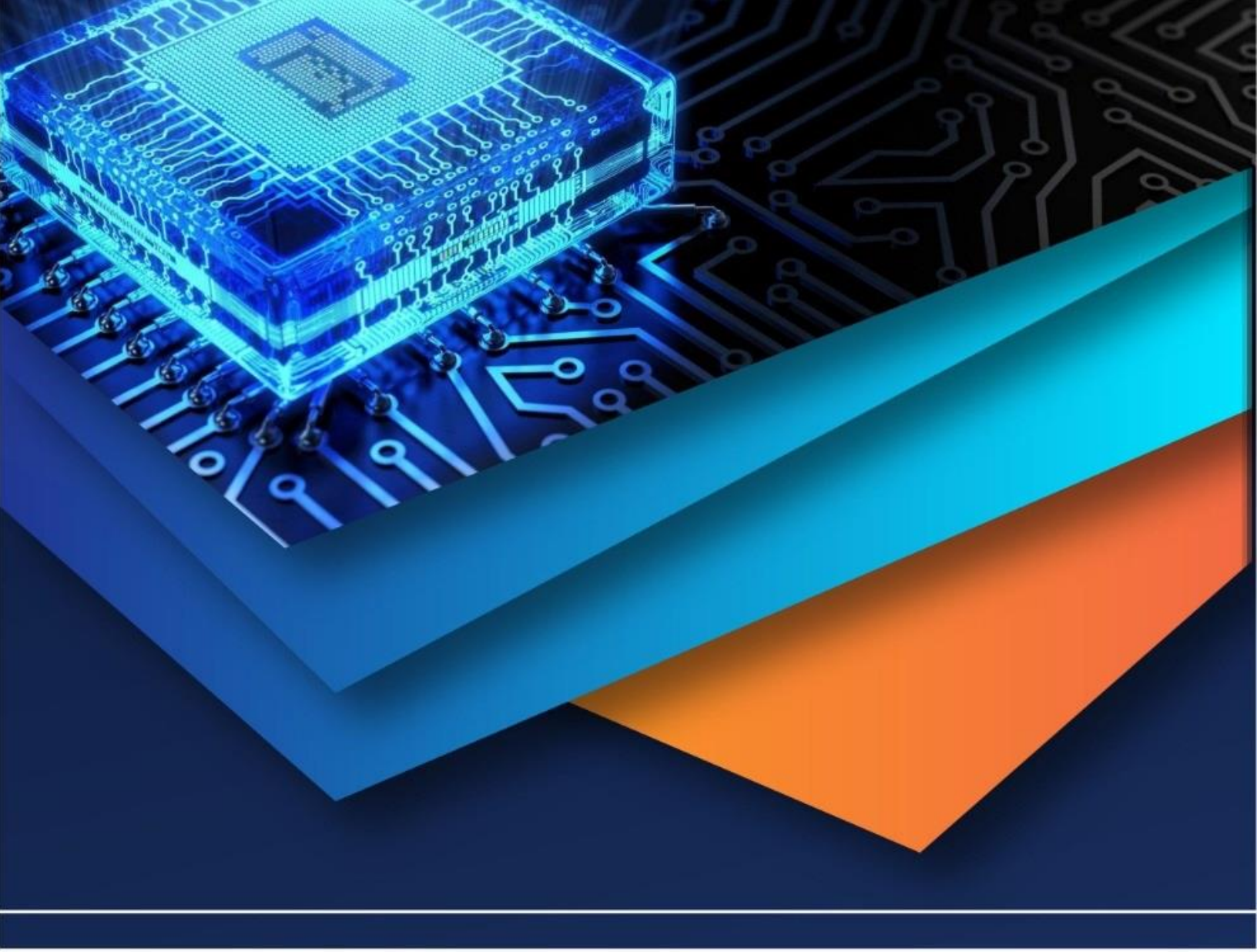
VI. CONCLUSION

In this paper, Cadence virtuoso tool along with 45nm technology is used to observe the behaviors of different types of SRAM. This design provides a virtuous improvement in Delay and Area. This proposed work enlarges the overall performance of the system by reducing complexity and cost. By analyzing overall performance, the proposed SRAM has more advantages. The Speed is also improved to some extent from the existing SRAMs.

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