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Two-Timescale Modelling of a Single-Inductor Dual-Input DC-DC Converter: Power Sharing, Output Ripple and Stability of the Averaged Plant

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Abstract: A single-inductor dual-input single-output (DISO) DC-DC converter shares one inductor between two sources by time-division scheduling. When the sources lie on opposite sides of the regulated output, the converter alternates between step-down and step-up operation within every scheduling frame. This paper develops a two-timescale model in which the switching-period-averaged models of the two modes are combined over the frame. The model gives closed-form relations for the delivery ratio that sets the required inductor current, the power share produced by a given time allocation, the quantisation of that allocation by the digital control period, and the output ripple on the frame and switching timescales. For fixed duties and positive parameters, the continuous-conduction frame-averaged model is globally exponentially stable about its unique equilibrium. For a 14.3 V / 5.0 V to 6.7 V converter with a 250 μ s frame, a 70 % time allocation gives a 76.35 % power share. In 75 controller-free simulations spanning allocation, load and scheduling period, the relations predicted the mean inductor current within 0.0113 % and the power share within 0.0555 %, and the frame-rate ripple within 4.7 %, in every case slightly overestimating it. A switched model confirms the frame-rate ripple of the switching-period-averaged output and shows that the instantaneous terminal voltage carries an additional switching-frequency step of about $R_{esr} \cdot i_L$ during step-up intervals, which raises its peak-to-peak ripple by a factor of 2.5–2.8.

Keywords: Single-inductor multi-input converter; time-division scheduling; averaged modelling; power sharing; output ripple; equivalent series resistance; Lyapunov stability.

I. INTRODUCTION

Systems that draw on more than one energy source — a battery with a photovoltaic panel, a supercapacitor or a regulated external supply — need a converter that combines dissimilar sources onto one regulated bus [1]–[3]. Giving each source its own converter is straightforward, but every additional inductor costs volume and parts. Single-inductor multi-input converters remove that duplication by connecting the sources to one shared inductor in turn [4]. Reviews of multi-input and multiport converters describe a wide range of such topologies and their control [5]–[8].

Sharing the inductor has two consequences that standard models do not capture. First, when one source is above and the other below the output voltage, the converter must operate in step-down mode for one source and step-up mode for the other. With time-division scheduling the operating mode, and with it the plant structure, changes twice in every frame. Second, the time allocated to a source is not the power drawn from it, because the sources differ in voltage and are connected through different current paths. Earlier work on this converter [9] treated the allocation as if it set the power share directly.

This paper develops and checks a model that accounts for both effects. Its contributions are:

- a two-timescale averaged model that combines the step-down and step-up averaged models over the scheduling frame;
- closed-form design relations for the delivery ratio, the time-share to power-share relation and the allocation quantisation;
- a ripple analysis that separates the frame-rate component of the switching-period-averaged output from the switching-frequency ESR component of the instantaneous terminal voltage;
- a proof that the fixed-duty frame-averaged plant is globally exponentially stable for positive parameters;
- a check of these relations by controller-free simulations over a 75-point grid and a switched model, with error metrics reported over the whole grid.

No controller is designed or compared here; the stability result concerns only the fixed-duty averaged plant.

II. LITERATURE SURVEY

Multi-input converter topologies have been classified as independent stages feeding a common bus, magnetically coupled arrangements, and converters sharing a single inductor [1], [2]. Systematic synthesis procedures and feasibility conditions for multiple-input topologies have been derived [10], [11], and early multiple-input designs showed how dissimilar sources can be combined by sharing time on a common stage [12]. Khaligh *et al.* [3] proposed a multiple-input converter in which the sources share one inductor, and Li and Wolfs [4] reviewed the single-inductor multiple-input family, including time-multiplexed operation; time-multiplexed control of a shared inductor is also the basis of single-inductor multiple-output converters [13]. Recent reviews cover application to electric vehicles and renewable systems [5], [6] and survey the control techniques used for non-isolated multiport converters [7]. Dual-input single-output converters have been designed for high step-up gain and hybrid energy systems [14], [15], a three-input boost converter has been modelled and controlled for a hybrid photovoltaic, fuel-cell and battery system [16], and work on a single-inductor double-output converter [17] shows that the shared inductor current couples the channels.

The modelling in this literature generally applies switching-period state-space averaging [18], [19] separately to each operating mode. Averaging is valid when the state changes little over the averaging window [20], and generalized averaging retains the harmonics that are needed when it does not [21]. Mode-by-mode averaging is adequate when many switching periods elapse before the mode changes. In a time-division scheduled converter it is not: in the converter studied here a 250 μ s frame contains only 12.5 periods of the 50 kHz switching frequency. Two further points are rarely treated explicitly: the difference between the share of time and the share of power drawn from a source, which is related to the power-budgeting problem of multiple-input converters [22], and the origin of the output ripple when the delivery path is interrupted during step-up intervals. This paper addresses both.

III. PROPOSED METHODOLOGY AND DISCUSSION

A. Converter and Operating Modes

The converter of Fig. 1 connects a primary source V_1 and an auxiliary source V_2 through input-selection switches S_1 and S_2 to a shared inductor L . A mode-control switch S_3 grounds the inductor output node for step-up operation, a freewheel diode D_1 returns the inductor current during step-down operation, and a delivery diode D_2 passes it to the output capacitor C and the load. S_1 and S_2 are never closed together. Table I lists the parameters, which are those of the authors' earlier design [9].

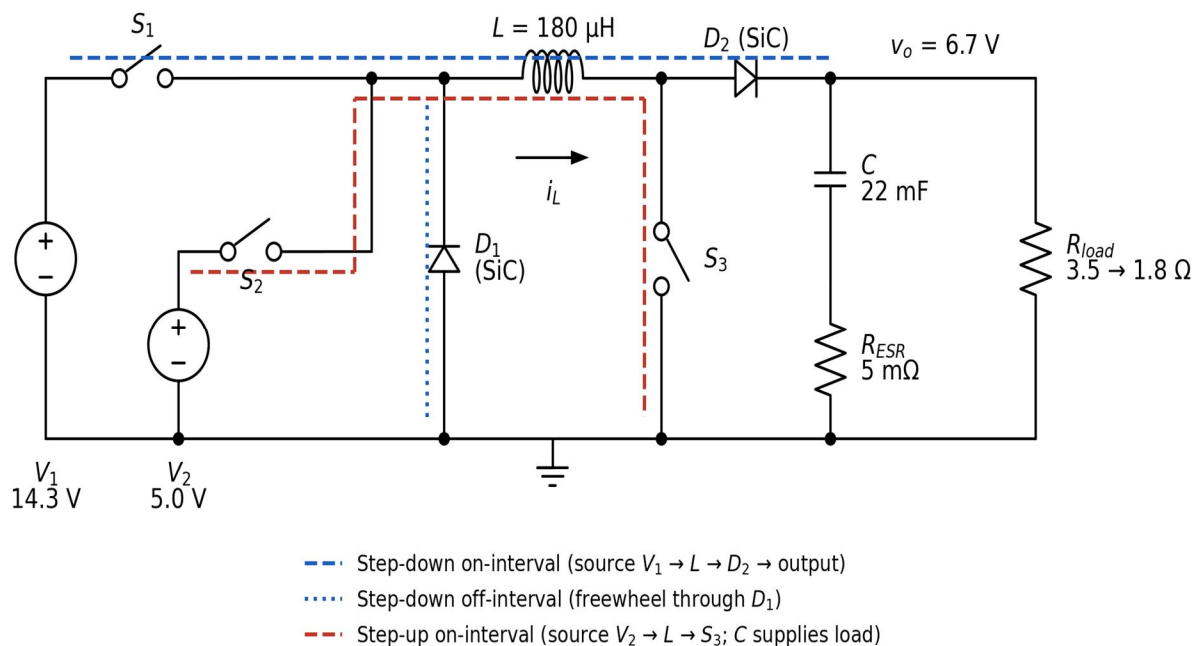


Fig. 1 Single-inductor DISO converter. Dashed and dotted paths show the step-down on- and off-intervals and the step-up on-interval.

TABLE I
CONVERTER PARAMETERS

Quantity	Symbol	Value
Primary source	V_1	14.3 V
Auxiliary source	V_2	5.0 V
Regulated output	V_{ref}	6.7 V
Inductance / DC resistance	L / r_L	180 μ H / 15 m Ω
Output capacitance / ESR	C / R_{esr}	22 mF / 5 m Ω
Switch on-resistance / diode drop	R_{on} / V_f	0.3 m Ω / 0.3 V
Switching frequency	f_{sw}	50 kHz
Control period (update rate)	T_s	5 μ s (200 kHz)
Scheduling period (rate)	T_{TDM}	250 μ s (4 kHz)
Nominal time allocation to V_1	β	0.70
Load	R	1.8–3.5 Ω

With $V_1 = 14.3$ V the primary source requires step-down operation: the active input switch is modulated and D_2 conducts in both sub-intervals, so the output receives the full inductor current. With $V_2 = 5.0$ V the auxiliary source requires step-up operation: the input switch stays closed, S_3 is modulated, and during the S_3 on-interval the output is isolated from the inductor (Table II).

TABLE II
SWITCHING STATES IN EACH MODE

Mode / interval	S_1 or S_2	S_3	D_1	D_2	Current path
Step-down, on (dT)	closed	open	off	on	source $\rightarrow L \rightarrow D_2 \rightarrow$ output
Step-down, off ($(1-d)T$)	open	open	on	on	$L \rightarrow D_2 \rightarrow$ output $\rightarrow D_1$
Step-up, on (dT)	closed	closed	off	off	source $\rightarrow L \rightarrow S_3$; C supplies load
Step-up, off ($(1-d)T$)	closed	open	off	on	source $\rightarrow L \rightarrow D_2 \rightarrow$ output

Setting the average inductor voltage to zero, with the diode and resistive drops included, gives the steady-state duties

$$D_{buck} = \frac{V_o + V_f + r_L i_L}{V_1 + V_f - R_{on} i_L} \quad (1)$$

$$D_{boost} = 1 - \frac{V_2 - (r_L + R_{on}) i_L}{V_o + V_f} \quad (2)$$

At $i_L = 4.1$ A these give $D_{buck} = 0.4837$ (ideal 0.4685) and $D_{boost} = 0.2947$ (ideal 0.2537). In the simulations below the duties are held at these values; (1) and (2) are an operating-point calculation, not a feedback law.

B. Switching-Period Averaged Model

With state $\mathbf{x} = [i_L, v_C]^T$ and duty d , weighting each sub-interval by its duration gives, for step-down operation,

$$L \frac{di_L}{dt} = dV_1 - v_o - (1-d)V_f - (r_L + dR_{on})i_L, \quad C \frac{dv_C}{dt} = i_L - \frac{v_o}{R} \quad (3)$$

and for step-up operation

$$L \frac{di_L}{dt} = V_2 - (1-d)(v_o + V_f) - (r_L + R_{on})i_L, \quad C \frac{dv_C}{dt} = (1-d)i_L - \frac{v_o}{R} \quad (4)$$

The terminal voltage differs from the capacitor voltage because the delivered current i_{del} flows through the ESR:

$$v_o = \frac{v_C + R_{esr} i_{del}}{1 + R_{esr}/R} \quad (5)$$

where $i_{del} = i_L$ in step-down operation and $i_{del} = (1-d)i_L$ in step-up operation. The switch resistance carries weight d in step-down operation but unity in step-up operation, because the input switch is closed for the whole period, and the capacitor equation carries the factor $(1-d)$ in step-up operation, reflecting the interrupted delivery path. The model describes continuous-conduction operation ($i_L > 0$).

C. Frame Averaging Over the Scheduling Period

Two timescales govern the converter: $T_{\text{TDM}}/T_s = 50$ control updates per frame, but only $T_{\text{TDM}}f_{\text{sw}} = 12.5$ switching periods. Because the source, the mode and the delivery path all change within the frame, the quantities of interest are frame averages. Let β be the fraction of the frame allocated to V_1 . Writing (3) and (4) as $\mathbf{f}_{\text{buck}}$ and $\mathbf{f}_{\text{boost}}$, the frame-averaged dynamics are

$$\frac{d\mathbf{x}}{dt} = \beta \mathbf{f}_{\text{buck}}(\mathbf{x}, d_1, V_1) + (1 - \beta) \mathbf{f}_{\text{boost}}(\mathbf{x}, d_2, V_2) \quad (6)$$

Equation (6) combines two vector fields of different structure, not one field with a varying coefficient. Its main assumption is that i_L changes little within a frame, so that the same i_L can be used in both intervals. Applied to the capacitor equations, it gives the average delivered current $i_{\text{del}} = \kappa i_L$, with the delivery ratio

$$\kappa = \beta + (1 - \beta)(1 - D_{\text{boost}}) \quad (7)$$

At $\beta = 0.70$ and $D_{\text{boost}} = 0.2947$, $\kappa = 0.9116$: the inductor must carry about 10 % more current than the load draws. At 1.8 Ω (3.722 A) the required inductor current is 4.083 A.

D. Time Share and Power Share

In step-down operation the source supplies current only while its switch conducts, so its average current is $D_{\text{buck}}i_L$; in step-up operation the input switch is closed throughout and the source supplies i_L . Neglecting switching and transition losses, $P_1 = \beta V_1 D_{\text{buck}}i_L$ and $P_2 = (1 - \beta)V_2 i_L$, and the share drawn from the primary source is

$$S = \frac{\beta V_1 D_{\text{buck}}}{\beta V_1 D_{\text{buck}} + (1 - \beta)V_2} \quad (8)$$

The inductor current cancels, so S depends only on the allocation, the two source voltages and the step-down duty. At $\beta = 0.70$, $S = 0.7635$: a 70 % time allocation produces a 76 % power share. Fixing β therefore does not fix the power share.

E. Quantisation of the Allocation

A source can be switched only on a control boundary. In the implementation used here, control step k is assigned to V_1 when the frame phase $(kT_s \bmod T_{\text{TDM}})/T_{\text{TDM}}$ is less than β , so the realised allocation is quantised with a resolution of

$$\Delta\beta = \frac{T_s}{T_{\text{TDM}}} \quad (9)$$

which is 0.02 at $T_{\text{TDM}} = 250 \mu\text{s}$ and 0.04 at 125 μs . At 62.5 μs a frame is 12.5 control periods, so the pattern repeats every two frames (25 periods) and the average resolution is again 0.04. In both short-frame cases a commanded 0.70 (17.5 of 25 periods) is realised as 18/25 = 0.72. The commanded allocation, the realised allocation and the resulting power share are therefore three different quantities, and a sharing loop that ignores (9) sees a residual it cannot remove.

F. Output Ripple on Two Timescales

Over one frame the delivered current changes twice: it equals i_L in the step-down interval and $(1 - D_{\text{boost}})i_L$, on average, in the step-up interval. At $\beta = 0.70$ and 1.8 Ω the converter delivers 4.083 A for 175 μs and 2.880 A for 75 μs against a load of 3.722 A, so the capacitor stores $\Delta Q = 63.2 \mu\text{C}$ and returns it once per frame. In the switching-period-averaged output this gives a capacitive ramp and a step at each mode change:

$$\Delta V_{\text{frame}} \approx \frac{\Delta Q}{C} + R_{\text{esr}} D_{\text{boost}} i_L, \quad \Delta Q = (i_L - i_o)\beta T_{\text{TDM}} \quad (10)$$

The instantaneous terminal voltage contains one further component. Within each step-up switching period the delivered current alternates between zero and i_L , so v_o steps by approximately $R_{\text{esr}}i_L$ at the switching frequency. To first order the instantaneous peak-to-peak ripple is therefore

$$\Delta V_{\text{inst}} \approx \frac{\Delta Q}{C} + \frac{R_{\text{esr}} i_L}{1 + R_{\text{esr}}/R} \quad (11)$$

Equations (10) and (11) are first-order estimates, not bounds. The ESR enters both. The small-signal response confirms that it cannot be neglected here: $\omega_0 = 1/\sqrt{LC} = 502.5 \text{ rad/s}$ (80 Hz), $Z_0 = \sqrt{L/C} = 0.0905 \Omega$, of the same order as the parasitic resistances, and the ESR zero lies at $1/(2\pi R_{\text{esr}}C) = 1447 \text{ Hz}$.

G. Stability of the Frame-Averaged Plant with Fixed Duties

With β , D_{buck} and D_{boost} fixed, (6) is affine in $\mathbf{x}$. Let $\alpha = 1 - D_{\text{boost}}$, $G = 1/(1 + R_{\text{esr}}/R)$ and κ as in (7). In each mode $\partial v_o / \partial v_c = G$ and $\partial v_o / \partial i_L = GR_{\text{esr}}\alpha_j$, where $\alpha_j = 1$ (step-down) or α (step-up); in the capacitor equation the i_L coefficient $\alpha_j(1 - GR_{\text{esr}}/R)$ simplifies to $\alpha_j G$. Weighting the two modes by β and $1 - \beta$, the Jacobian is

$$\mathbf{A} = \begin{bmatrix} -r_{\text{eq}}/L & -G\kappa/L \\ G\kappa/C & -G/(RC) \end{bmatrix} \quad (12)$$

$$r_{\text{eq}} = r_L + \beta D_{\text{buck}} R_{\text{on}} + (1 - \beta) R_{\text{on}} + GR_{\text{esr}}[\beta + (1 - \beta)\alpha^2] \quad (13)$$

The α^2 term arises because the step-up inductor equation multiplies v_o by α , and the ESR part of v_o is itself proportional to the delivered current αi_L . For $R, L, C, r_L, R_{\text{esr}} > 0$, $R_{\text{on}} \geq 0$ and $0 \leq \beta, D_{\text{buck}}, D_{\text{boost}} \leq 1$,

$$\text{tr } \mathbf{A} = -\frac{r_{\text{eq}}}{L} - \frac{G}{RC} < 0, \quad \det \mathbf{A} = \frac{r_{\text{eq}} G}{RLC} + \frac{G^2 \kappa^2}{LC} > 0 \quad (14)$$

so both eigenvalues of the 2×2 matrix $\mathbf{A}$ have negative real parts and $\mathbf{A}$ is Hurwitz. Since $\det \mathbf{A} \neq 0$ the affine system has a unique equilibrium $\mathbf{x}_e$, and with $\mathbf{e} = \mathbf{x} - \mathbf{x}_e$ the error obeys $d\mathbf{e}/dt = \mathbf{A}\mathbf{e}$. For the positive-definite solution $\mathbf{M}$ of $\mathbf{A}^T \mathbf{M} + \mathbf{M} \mathbf{A} = -\mathbf{I}$, the Lyapunov function $V = \mathbf{e}^T \mathbf{M} \mathbf{e}$ gives $dV/dt = -\mathbf{e}^T \mathbf{e}$ [23], so the equilibrium is globally exponentially stable for the averaged model. In the physical converter the result holds while operation remains in continuous conduction. It does not imply that the equilibrium voltage equals V_{ref} for arbitrary duties, and it does not extend by itself to duty feedback, saturation, delay or the periodically switched converter, for which switched-system results apply [24], [25]; those cases need separate analysis.

H. Validation Protocol and Data Provenance

The relations above were checked without any controller, so that the result depends only on the plant and the scheduling. The averaged model (3)–(5) with explicit source scheduling was integrated with a second-order (Heun) method at the 5 μs control period. The source schedule was computed from an integer clock (kT_s on an integer-nanosecond timebase), so that the mode-selection decision does not drift over long runs. The duties were held at the values of (1) and (2) for 6.7 V at each operating point; each run lasted 500 ms and quantities were evaluated over the final 25 ms. The grid covered $\beta = 0.5$ – 0.9 in steps of 0.1, $R = 3.5$, 2.5 and 1.8 Ω , and $T_{\text{TDM}} = 62.5$, 125, 250, 500 and 1000 μs : 75 operating points. The power share was obtained by integrating the source power, the realised allocation by counting control intervals, and the ripple as the peak-to-peak output over the window. Equations (7), (8) and (10) were evaluated with the realised allocation, the applied duties and the simulated mean output; each error is (predicted – simulated)/simulated.

A switched model, which resolves every switch transition at 50 kHz and records the instantaneous terminal voltage, was run at five operating points with the same timebase. PWM periods start at control boundaries; because T_{TDM} equals 12.5 switching periods and the step-down interval at $\beta = 0.70$ is 8.75 switching periods, each mode change falls part-way through a switching period, and the alignment alternates between successive frames.

The simulations were run in a Python implementation of the plant equations of the authors' MATLAB testbench. Because the simulations and the derivation share the plant equations (3)–(5), this is a check of the frame-averaging, quantisation and constant-current assumptions behind (7)–(11) within that model, not an independent validation of the component model; a closely related model was compared with prototype measurements in [9].

The same converter and parameter set are used in a separate controller-benchmarking manuscript by the authors; no controller results, tables or figures from that study are reported here.

IV. RESULTS

A. Accuracy Over the Operating Grid

Table III summarises the agreement by scheduling period. The delivery ratio predicts the mean inductor current within 0.0113 % and the share relation predicts the power share within 0.0555 % at every one of the 75 points; both errors grow slowly with the frame length, as the constant-current assumption becomes less exact. The quantisation of (9) is visible directly: at 62.5 μs and 125 μs a commanded 0.70 is realised as 0.72, and the share follows the realised value (0.7806 rather than 0.7635). The frame-rate ripple of (10) is predicted within 4.69 % over the whole grid. The error is positive at every point, between 1.53 % and 4.69 %, so (10) slightly overestimates the ripple and is conservative for design.

TABLE III
MODEL ACCURACY OVER 75 CONTROLLER-FREE OPERATING POINTS

T_{TDM}	Realised β (commanded 0.70)	Max error i_L , eq. (7)	Max error S , eq. (8)	Ripple error, eq. (10): mean / max
62.5 μ s	0.72	0.0001 %	0.0009 %	3.45 % / 4.66 %
125 μ s	0.72	0.0002 %	0.0015 %	4.19 % / 4.69 %
250 μ s	0.70	0.0007 %	0.0041 %	3.63 % / 4.27 %
500 μ s	0.70	0.0028 %	0.0144 %	2.92 % / 3.74 %
1000 μ s	0.70	0.0113 %	0.0555 %	2.06 % / 3.01 %

B. Simulated Power Share and Delivery Ratio

Table IV and Fig. 2 compare the share relation with the simulated share at 1.8 Ω and 250 μ s. Assuming $S = \beta$ understates the primary source's share by between 2.6 and 8.1 percentage points over $\beta = 0.5$ –0.9, the largest error occurring near $\beta = 0.5$ –0.6. The delivery ratio rises from 0.852 to 0.971 over the same range, so the inductor current needed for the same load falls from 4.37 A to 3.83 A as more time is given to the step-down source.

TABLE IV
POWER SHARE AND DELIVERY RATIO AGAINST TIME ALLOCATION (1.8 Ω , 250 μ s)

β	S , eq. (8)	S , simulated	κ , eq. (7)	i_L , simulated (A)
0.50	0.5806	0.5806	0.8524	4.367
0.60	0.6749	0.6749	0.8820	4.220
0.70	0.7635	0.7635	0.9116	4.083
0.80	0.8469	0.8469	0.9411	3.955
0.90	0.9256	0.9256	0.9706	3.835

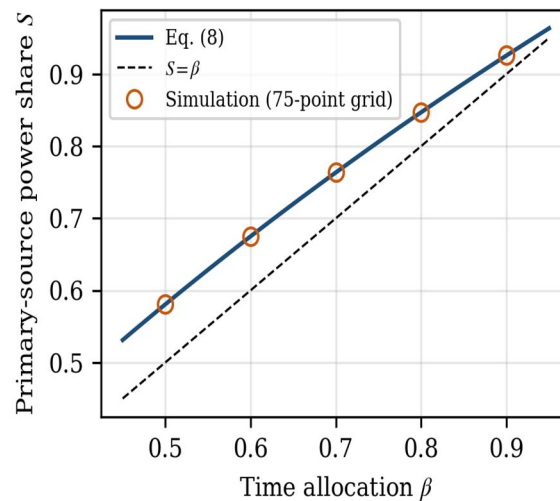


Fig. 2 Power share against time allocation at 1.8 Ω and 250 μ s: eq. (8) and controller-free simulation.

C. Frame-Rate Ripple and the Scheduling Period

Fig. 3 shows the switching-period-averaged ripple against scheduling period at $\beta = 0.70$ for three loads. The ripple grows with both the frame length and the load current, as (10) predicts, because the stored charge ΔQ scales with both. At 250 μ s and 1.8 Ω the prediction is 8.89 mV (0.133 %) against a simulated 8.58 mV (0.128 %); the ESR step (6.02 mV) contributes about two thirds and the capacitive ramp (2.87 mV) one third. The scheduling period is therefore a first-order design variable for ripple.

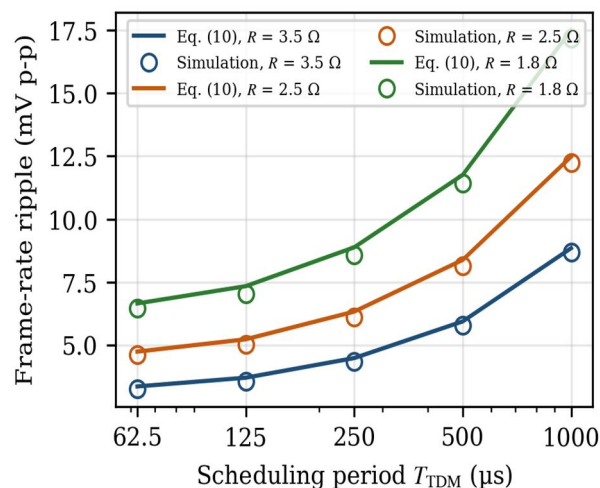


Fig. 3 Switching-period-averaged output ripple against scheduling period at $\beta = 0.70$: eq. (10) and simulation.

D. Switched-Model Check and the Instantaneous Ripple

Table V compares the averaged and switched models at five operating points. The largest power-share difference is 1.23 % relative (0.94 percentage points) and the largest mean-inductor-current difference is 0.90 %; with the duties held open-loop, the switched model's mean output is 25–31 mV lower than the averaged model's, an offset caused by the partial switching periods at each mode change, which a voltage controller would remove. The switching-period average of the switched output reproduces the shape of the frame-rate ripple; (10) underestimates its amplitude by 6–17 %, because the partial switching periods at the mode changes add to the step at each transition. The instantaneous terminal voltage has a peak-to-peak ripple 2.5 to 2.8 times larger than the switching-period average, because of the $R_{esr} i_L$ step in every step-up switching period (Fig. 4). Equation (11) predicts that ripple within 12 %, slightly low because it uses the mean rather than the peak inductor current.

TABLE V
AVERAGED AND SWITCHED MODELS COMPARED ($T_{TDM} = 250 \mu s$, FIXED DUTIES)

β, R	S_{avg} / s_w	i_L_{avg} / s_w (A)	Ripple, avg model	Ripple, sw, period-averaged (pred. eq. 10)	Ripple, sw, instantaneous (pred. eq. 11)
0.7, 3.5 Ω	0.7627 / 0.7533	2.097 / 2.081	4.35 mV	5.43 mV (4.50)	13.52 mV (11.92)
0.7, 2.5 Ω	0.7630 / 0.7565	2.937 / 2.914	6.12 mV	7.17 mV (6.34)	18.26 mV (16.70)
0.7, 1.8 Ω	0.7635 / 0.7588	4.083 / 4.050	8.58 mV	9.60 mV (8.89)	24.72 mV (23.23)
0.5, 1.8 Ω	0.5806 / 0.5749	4.367 / 4.327	9.77 mV	10.76 mV (10.11)	26.92 mV (25.43)
0.9, 1.8 Ω	0.9256 / 0.9237	3.835 / 3.805	6.51 mV	7.87 mV (6.79)	22.23 mV (20.27)

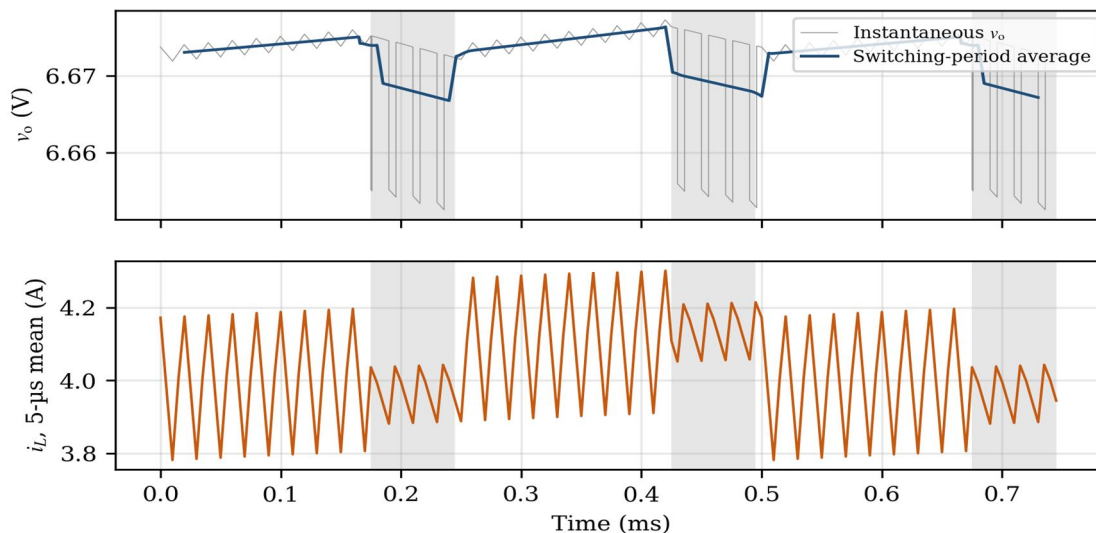


Fig. 4 Switched model at $\beta = 0.70$, 1.8Ω , $250 \mu\text{s}$, final three frames: instantaneous and switching-period-averaged output voltage (top) and inductor current averaged over each $5 \mu\text{s}$ control period (bottom). Shaded: step-up intervals.

Two practical consequences follow. A controller that samples the output synchronously with the switching period, or a measurement with limited bandwidth, sees essentially the frame-rate ripple of (10); a wide-band measurement of the terminal voltage sees (11). Reported ripple figures for this class of converter should therefore state how the ripple was measured. In both cases the ESR is the largest single contributor, so it is the main ripple design parameter alongside the scheduling period.

E. Stability Margins of the Averaged Plant

Fig. 5 shows the eigenvalues of (12) for the 15 combinations of β and R in the grid; T_{TDM} does not enter the averaged Jacobian, so these cover all 75 points. The trace lies between -135.72 and -118.39 s^{-1} and the determinant between 1.851×10^5 and $2.394 \times 10^5 \text{ s}^{-2}$, as (14) requires. At $\beta = 0.70$ and 1.8Ω the eigenvalues are $-66.55 \pm j454.95 \text{ s}^{-1}$: a lightly damped mode near the 80 Hz LC resonance (damping ratio about 0.14), which is consistent with the slow settling of the open-loop runs and is the mode a voltage controller must damp.

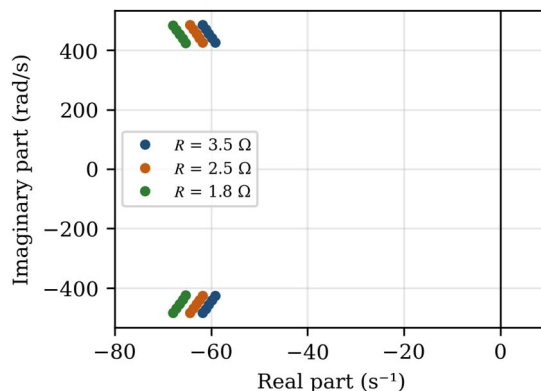


Fig. 5 Eigenvalues of the fixed-duty frame-averaged plant (12) for $\beta = 0.5\text{--}0.9$ and $R = 1.8\text{--}3.5 \Omega$.

V. CONCLUSIONS

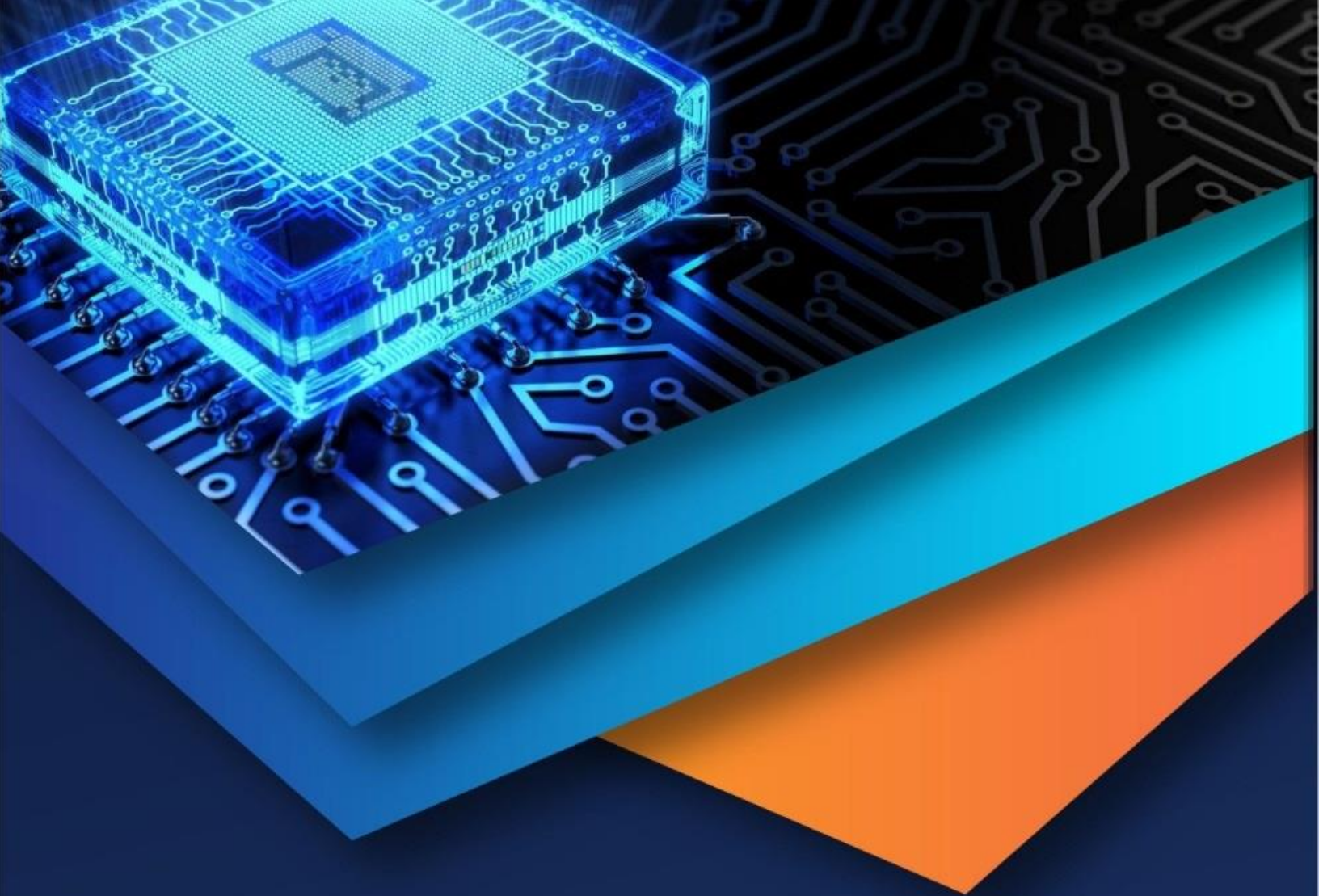
A time-division scheduled single-inductor DISO converter changes its plant structure twice per frame, and a frame contains only a few switching periods. Averaging the step-down and step-up models over the frame gives three design relations — the delivery ratio κ , the power share S as a function of the time allocation β , and the allocation quantisation T_s/T_{TDM} — and a two-timescale description of the output ripple. With fixed duties and positive parameters, the continuous-conduction frame-averaged model is globally exponentially stable about its unique equilibrium.

For the 14.3 V / 5.0 V to 6.7 V converter studied, a 70 % time allocation gives a 76 % power share, so the share must be regulated explicitly if it matters. Over 75 controller-free operating points the relations predicted the inductor current within 0.0113 %, the power share within 0.0555 % and the frame-rate ripple within 4.7 %, conservatively. The ripple has two parts: a frame-rate part set by the stored charge and the ESR step at each mode change, and, in the instantaneous terminal voltage, a switching-frequency ESR step during step-up intervals that raises the peak-to-peak value by a factor of 2.5–2.8. The study is a simulation study with fixed duties that shares its plant equations with the derivation; closed-loop and switched-system stability, three or more sources and hardware confirmation of the instantaneous ripple are left for future work.

The simulation code (model, sweep, switched-model, stability and figure scripts) and the result files from which every table and figure was generated are available from the corresponding author on request.

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