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Universal Asyncronous Receiver Transmitter

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Abstract: ***This project focuses on the Verilog-based design and implementation of a Universal Asynchronous Receiver-Transmitter (UART) communication module. The UART is a fundamental component in digital systems, facilitating serial data transmission between devices. Our objective is to develop a robust and efficient Verilog description of the UART module, emphasizing simplicity, modularity, and ease of integration. The baud rate generator allows for flexible communication speeds, accommodating diverse applications. The module ensures accurate framing of transmitted and received data through the proper generation of start and stop bits. Error-detection mechanisms are implemented to enhance data integrity.***
The project enhances the digital design field by delivering a Verilog implementation of a UART communication module that is both dependable and efficient.
Keywords: Verilog, UART, hardware description language, digital communication, baud rate, start bit, stop bit, data framing, error detection, asynchronous serial communication, FPGA, simulation, testing, reliability.

I. INTRODUCTION

Universal Asynchronous Receiver/Transmitter (UART) stands as a fundamental component in the landscape of digital communication, serving as a linchpin in the seamless exchange of data between electronic devices. Integrating the Verilog-based UART into the FPGA facilitates compact, stable, and dependable data transmission.

The Universal Asynchronous Receiver Transmitter (UART) functions as a serial communication protocol, primarily employed for the exchange of data between computers and peripherals in scenarios characterized by short distances, low speeds, and cost considerations. In the realm of asynchronous serial data communication, UARTs play a key role by transforming data from parallel to serial at the transmitter. This process introduces additional overhead bits using a shift register. Conversely, at the receiver, the UART converts serial data back to parallel. Typically, UARTs are interposed between a processor and a peripheral device. From the perspective of the processor, the UART presents itself as an 8-bit read/write parallel port.

As we navigate the dynamic landscape of digital systems, the synergy between UART and Verilog becomes increasingly pivotal, influencing the efficiency, scalability, and adaptability of communication protocols.

FPGA chip to achieve compact, stable and reliable data transmission to avoid waste of resources and decrease cost, programmable logic to enable interfacing between asynchronous communications 2 protocols and DSP having synchronous serial ports. It also supports configurable baud rate generator and variable data length from 8 bits per frame.

It manages the conversion between serial and parallel data, a critical function in digital communication systems. Serial communication, facilitated by this process, offers advantages such as minimizing signal distortion, enabling reliable data transfer over considerable distances between two systems. This capability is pivotal in overcoming challenges posed by long-distance communication scenarios, ensuring the integrity and accuracy of transmitted data.

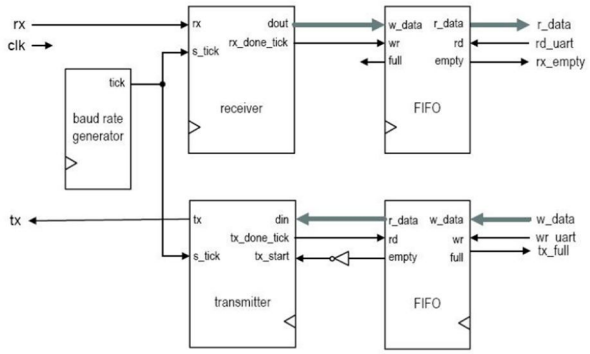


Fig. UART Circuit Diagram

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II. LITERATURE REVIEW

The Universal Asynchronous Receiver-Transmitter (UART) protocol serves as a cornerstone in serial communication, facilitating data exchange between diverse digital devices. As the need for effective and scalable communication interfaces grows, the incorporation of UART using the Verilog hardware description language becomes an appealing path for both researchers and engineers. These modules, both reusable and synthesizable, serve as data detectors in an IR ranging system for obtaining distance information from objects. Additionally, they function as data detectors in a digital compass to receive the robot's head direction and a transceiver of a wireless modem to communicate with the other robots and host computer.[1]

UARTs are used for communication between two devices. UARTs are used to connect terminals to computers. UARTs are also used in systems using MIDI. The data is sent bit-serially, and no clock signal is sent along with it. The sender and receiver operate with independent clock signals that lack synchronization. Universal Asynchronous Receiver Transmitter) is used for serial communication. It serves as a cost-effective solution for long-distance data transfer between a PC and its peripherals In general a UART operated with specific baud rate.[2]

The UART requires an expanded internal buffer to retain incoming data from the modem until the CPU can manage its processing. Meeting the intricate communication requirements goes beyond adequacy. To overcome this difficulty a multichannel UART is proposed in this paper. And the whole design is simulated with modelsim and synthesized with Xilinx software.[3] Therefore, the implementation of the UART communication module is actually the realization of the three sub-modules. Utilized for the reception of serial signals at RXD, the UART receiver module transforms them into parallel data. The UART transmit module converts it encodes bytes into serial bits following the fundamental frame format and sends these bits through the TXD transmission.

Within the UART, there exists both a receiver, responsible for serial-to-parallel conversion, and a transmitter, which performs parallel-to-serial conversion. It handles the conversion between serial and parallel data. Serial communication reduces the distortion of a signal, therefore makes data transfer between two systems separated in great distance possible.[4] The importance for System-on-Chip (SOC) using a reusable IP is increasing in modern design methodology. The old design method is not suitable to design chip which operates on a required function in a given time.[5] The FPGA-based system is also useful because it can reduce development time greatly. In designing hardware, many design processes entail modeling hardware in varied levels of detail.[6]

III. METHODOLOGIES

Implementing UART functionality using Verilog involves a systematic and modular approach to design. The following methodologies provide a structured framework for developing a robust UART module in Verilog.

A. Understanding UART Basics

Begin by comprehensively understanding the fundamental principles of UART communication. This includes asynchronous data transmission, start and stop bits, baud rate generation, and the structure of UART frames. A solid grasp of these concepts lays the groundwork for an effective Verilog implementation.

B. Receiver Module

The receiver of the UART is composed of a state machine, a de-serializer, and a support logic. The main goal of the receiver is to detect the start-bit, then de-serialize the following bit-stream, detect the stop-bit, and make the data available to the host. Fig. illustrates the functional block diagram of the receiver. The design is minimalist, and no error checking logic is presented by default. All of these features are to become user-enhancements. The receiver needs to detect the start and stop bits to properly frame the incoming data. The module looks for a falling edge (start bit) to initiate the reception process. The actual data bits are sampled on each rising edge of the clock, and a rising edge (stop bit) indicates the completion of the data frame.

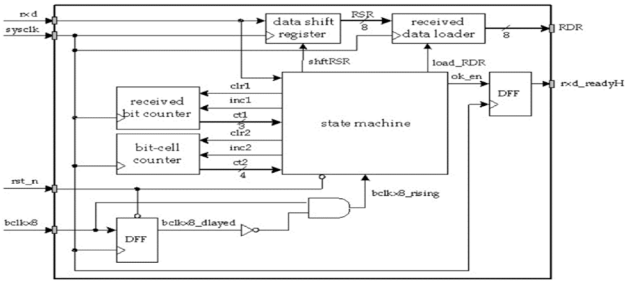


Fig. Functional block-diagram of the UART receiver

C. Transmitter Module

The transmitter of UART is composed of transmitted bit counter, a data shift register, a state machine and support logic. Fig. illustrates the functional block diagram of the UART transmitter. The transmitted bit counter has the same function and implementation as that of the receiver, only the signal name have changed slightly.

The transmitter module of a UART implementation is responsible for converting parallel data into a serial format suitable for transmission over a communication channel.The receiver tests the state of the incoming signal on each clock pulse looking for the beginning of the startbit. As soon as the start bit is detected.

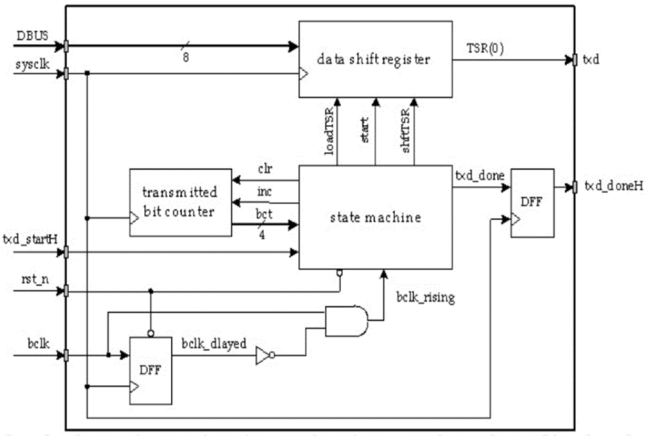


Fig. Functional block-diagram of the UART transmitter

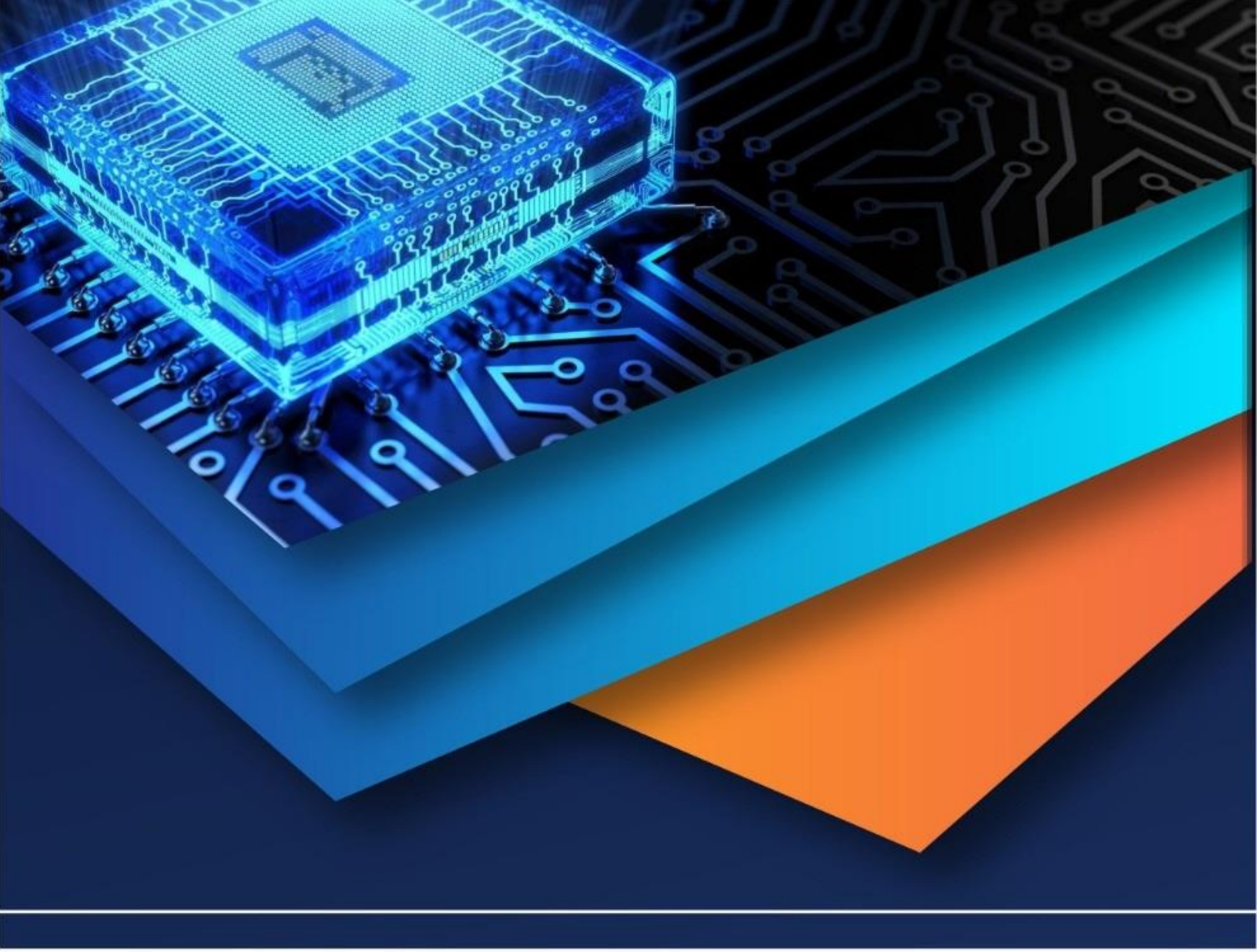
IV. CONCLUSION

This paper introduces our proposed UART design, comprising an internal transmitter, receiver, and baud rate generator. Successful simulation using Xilinx ISE 8.2 software validates the stability, reliability, and correct functionality of the design. Hence, we can improve the speed of UART by sending 16 bits per second of time. But by sending 16 bits, it becomes more complex to count number ofclock bit per unit time, so this can be overcome by using multichannel UART in future.

Throughout this review, we delved into the basics of UART communication, emphasizing its asynchronous nature, the significance of start and stop bits, and the impact of baud rate on data transmission speed. The integration of Verilog into the discussion provided insights into the language's role in digital design and FPGA programming, highlighting its advantages in the context of UART implementation.

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