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Abstract: This paper proposed the layout of Vedic Multiplier based totally on Urdhva Trigbhyam approach of multiplication. It is most effective Vedic sutras for multiplication. Urdhva triyagbhyam is a vertical and crosswise approach to discover product of two numbers. Multiplication is an essential quintessential feature in arithmetic logic operation. Computational overall performance of a DSP device is limited via its multiplication overall performance and since, multiplication dominates the execution time of most DSP algorithms. Multiplication is one of the simple arithmetic operations and it requires extensively extra hardware assets and processing time than addition and subtraction. Our work is to compare different bit Vedic multiplier structure using carry look ahead adder technique.

Keywords: Carry Look Ahead Adder, Urdhva Trigbhyam, DSP algorithms, Vedic Multiplier

## I. INTRODUCTION

Multipliers play an vital role in today's digital signal processing and various other applocations. In excessive overall performance structures such as microprocessor, DSP and many others addition and multiplication of two binary numbers is necessary and most regularly used arithmetic operations. Statics suggests that greater than 70% instructions in microprocessor and most of DSP algorithms operate addition and multiplication. So, these operation dominates the execution time. That's why, there is need of excessive pace multiplier. The demand of excessive pace processing has been growing as a end result of increasing computer and signal processing applications. A standard technique of array multiplication shown below:

			x	A3 B3	A2 B2	A1 B1	A0 B0	Inputs
			С	B0 x A3	B0 x A2	B0 x A1	B0 x A0	
		+	B1 x A3	B1 x A2	Bl x Al	B1 x A0		
		C	sum	sum	sum	sum		
	+	B2 x A3	B2 x A2	B2 x A1	B2 x A0			Internal Signals
	C	sum	sum	sum	sum			
+	B3 x A3	B3 x A2	B3 x A1	B3 x A0				
C	sum	sum	sum	sum				
Y7	¥6	¥5	Y4	Y3	Y2	Y1	Y0	Outputs

Fig.1 Array Multiplication

## II. PROPOSED SYSTEM

The proposed gadget is used to limit the raise propagation time and to optimize the hardware complexity degree for Vedic multiplier operation. The proposed device is to put in force vertical and cross-wise equation primarily based logical distinct bits multiplier operation.

Vedic Mathematics Swami Bharati Krishna Tirtha, known as a set of sixteen Sutras (aphorisms) and thirteen Sub-Sutras (Corollaries) from the Atharva Veda. He developed approach and strategies for amplifying the ideas contained in the aphorisms and their corollaries, and referred to as it Vedic Mathematics. In Vedic Mathematics partial products are generated in parallel, which will increase the pace of operation. In this paper we are proposing a format for accumulation of these intermediate products, with minimal delay Multiplication if an operation much needed in Digital Signal Processing for more than a few applications. This paper places ahead a excessive pace Vedic multiplier which is efficient in phrases of speed, making use of Urdhva Tiryakbhyam, a sutra from Vedic Math for multiplication.

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Fig2: Algorithm of UT sutra

## B. Carry Look Ahead Adder

"A carry-look ahead adder(CLA) is a type of fast parallel adder used in digital logic to calculate the carry signals in advance from the input signals." They reduce carry propogation time and implement addition of binary numbers. It is also known as: carry look ahead generator or fast adder or carry predictor. It is an improvement over "Ripple carry adder circuit".





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### C. Vedic Multiplier

Multiplication strategies that many of processors are using nowadays has stimulated by way of Vedic multiplier delivered in Indian Vedas with distinctive sixteen sutras. Vedic multiplier makes use of bit-wise multiplication with simultaneous product term finding and it's column-wise addition. It is one of the fine benchmark for fast multiplication algorithm.



Fig4(a): 2\*2 bit Vedic Multiplier Block Diagram



Fig4(b): 4\*4 bit Vedic Multiplier Block Diagram



Fig4(c): 8\*8 bit Vedic Multiplier Block Diagram



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Fig4(d): 16\*16 bit Vedic Multiplier Block Diagram



Fig4(e): 32\*32 bit Vedic Multiplier Block Diagram

III. SYNTHESIS & SIMULATION

Name	Value	10 ns 15	50 ns	100 ns	150 ns	200 ns	250 ns
🕨 🍓 c[3:0]	1001	000	)0 )	( 01	10	10	01
🕨 🏹 a[1:0]	11	( <u>op</u>		( 1	) )	1	1
▶ 📷 b[1:0]	11	01			1	1	

Fig. 5 Simulation Result of 2-bit Vedic Multiplier

Name	Value		945 ns	950 ns	955 ns	960 ns	965 ns		970 ns
🕨 式 c[7:0]	10011010	00100100	1001	1100	0011	0000		10011010	
🕨 📷 a[3:0]	1110	0110	11	01	01	10		1110	
🕨 📷 b[3:0]	1011	0110	11	00	10	00		1011	
🔚 cik	1								
🕨 📷 m[7:0]	10011010	00100100	1001	1100	0011	0000		10011010	

Fig. 6 Simulation Result of 4-bit Vedic Multiplier



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Name	Value	90 ns	95 ns	100 ns	105 ns	110 ns	115 ns	120
🕨 📑 c[15:0]	01101010011	10000010110100	01101010	01110011	00001010	00001110	110000101011110	0
🕨 📷 a[7:0]	11100101	11000101	1110	0101	x 0001	010	11110010	
🕨 📷 b[7:0]	01110111	10101010	0111	0111	1000	1111	11001110	
🔚 cik	1	1						
🕨 📷 m[15:0]	01101010011	10000010110100)	01101010	01110011	00001010	00001110	110000101011110	0

Fig. 7 Simulation Result of 8-bit Vedic Multiplier

Name	Value	1988 ns	1990 ns	1992 ns	994 ns		1996 ns	998 ns
▶ 📑 c[31:0]	11010101001	110	01010011011100101	1010111010		0000	0100010010000111	111101110111
🕨 📷 a[15:0]	11100100111		11100100111110	10		$\square$	000010010001	0111
Þ 📷 b[15:0]	11101110011		11101110011000	01			011110001010	0001
🔚 clk	1							
🕨 📷 m[31:0]	11010101001	110	01010011011100101	1010111010		0000	0100010010000111	111101110111

Fig. 8 Simulation Result of 16-bit Vedic Multiplier

Name	Value		945 ns	950 ns	955 ns	960 ns	965 ns	970 ns
▶ 🍓 c[63:0]	00111010110	00	000110101111110	10011010101010110	000011111100101	111011101111001	0011101011001	001111001101011
▶ 🃷 a[31:0]	00111111010	00	001111101001100	11000001101111101	010000110110000	10101011110000110	0011111101011	010100110110111
▶ 🃷 b[31:0]	11101101100	11	011011100101111	10000111111011100	001111000000001	1111111101111000	1110110110001	101100000001101
🐻 clk	1					1		
▶ 📷 m[63:0]	00111010110	00	000110101111110	100110101010101	000011111100101	111011101111001	0011101011001	001111001101011

Fig. 9 Simulation Result of 32-bit Vedic Multiplier

IV.



## Fig.10 RTL Schematic for 2 bit Vedic multiplier



Fig.11 RTL Schematic for 4 bit Vedic multiplie

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Fig.12RTL Schematic for 8 bit Vedic multiplier





Fig.14 RTL Schematic for 32 bit Vedic multiplier



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Device-Spartan6				
XC6SLX45-CSG324				
Vedic Multiplier	Delay (ns)	Levels of Logics	No. of slice LUTs	Memory (KB)
2-Bit	0.948	3	4	4617500
4-Bit	3.976	8	25	4617456
8-Bit	7.965	14	129	4617516
16-Bit	17.752	32	603	4617444
32-Bit	44.652	88	2618	4618656

Table1. Using Look Ahead Carry Adder

#### V. CONCLUSION

This paper presents a highly efficient approach of multiplication– "Urdhva Tiryakbhyam Sutra" primarily based on Vedic mathematics. It offers us approach for modular multiplier design and certainly shows the computational advantages provided by means of Vedic methods. The computational route delay for proposed new Vedic multiplier is observed to be much less as contrast to different multiplier. Hence motivation to minimize delay is finely fulfilled. Therefore, the new Vedic multiplier is much more efficient than Array and traditional multiplier in phrases of execution time (speed).

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