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Design, Implementation & Performance of Vedic Multiplier Based on Look Ahead Carry Adder for Different Bit Lengths

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Abstract: ***This paper proposed the layout of Vedic Multiplier based totally on Urdhva Trigbhyam approach of multiplication. It is most effective Vedic sutras for multiplication. Urdhva triyagbhyam is a vertical and crosswise approach to discover product of two numbers. Multiplication is an essential quintessential feature in arithmetic logic operation. Computational overall performance of a DSP device is limited via its multiplication overall performance and since, multiplication dominates the execution time of most DSP algorithms. Multiplication is one of the simple arithmetic operations and it requires extensively extra hardware assets and processing time than addition and subtraction. Our work is to compare different bit Vedic multiplier structure using carry look ahead adder technique.***

Keywords: Carry Look Ahead Adder, Urdhva Trigbhyam, DSP algorithms, Vedic Multiplier

I. INTRODUCTION

Multipliers play an vital role in today's digital signal processing and various other applocations. In excessive overall performance structures such as microprocessor, DSP and many others addition and multiplication of two binary numbers is necessary and most regularly used arithmetic operations. Statics suggests that greater than 70% instructions in microprocessor and most of DSP algorithms operate addition and multiplication. So, these operation dominates the execution time. That's why, there is need of excessive pace multiplier. The demand of excessive pace processing has been growing as a end result of increasing computer and signal processing applications. A standard technique of array multiplication shown below:

				A3	A2	A1	A0	Inputs
			x	B3	B2	B1	B0	
			C	B0 x A3	B0 x A2	B0 x A1	B0 x A0	
		+	B1 x A3	B1 x A2	B1 x A1	B1 x A0		
		C	sum	sum	sum	sum		
	+	B2 x A3	B2 x A2	B2 x A1	B2 x A0			Internal Signals
	C	sum	sum	sum	sum			
+	B3 x A3	B3 x A2	B3 x A1	B3 x A0				
C	sum	sum	sum	sum				
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Outputs

Fig.1 Array Multiplication

II. PROPOSED SYSTEM

The proposed gadget is used to limit the raise propagation time and to optimize the hardware complexity degree for Vedic multiplier operation. The proposed device is to put in force vertical and cross-wise equation primarily based logical distinct bits multiplier operation.

Vedic Mathematics Swami Bharati Krishna Tirtha, known as a set of sixteen Sutras (aphorisms) and thirteen Sub-Sutras (Corollaries) from the Atharva Veda. He developed approach and strategies for amplifying the ideas contained in the aphorisms and their corollaries, and referred to as it Vedic Mathematics. In Vedic Mathematics partial products are generated in parallel, which will increase the pace of operation. In this paper we are proposing a format for accumulation of these intermediate products, with minimal delay Multiplication if an operation much needed in Digital Signal Processing for more than a few applications. This paper places ahead a excessive pace Vedic multiplier which is efficient in phrases of speed, making use of Urdhva Tiryakbhyam, a sutra from Vedic Math for multiplication.

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A. Multiplication Algorithim For Urdhva Tiryakbhyam Sutra

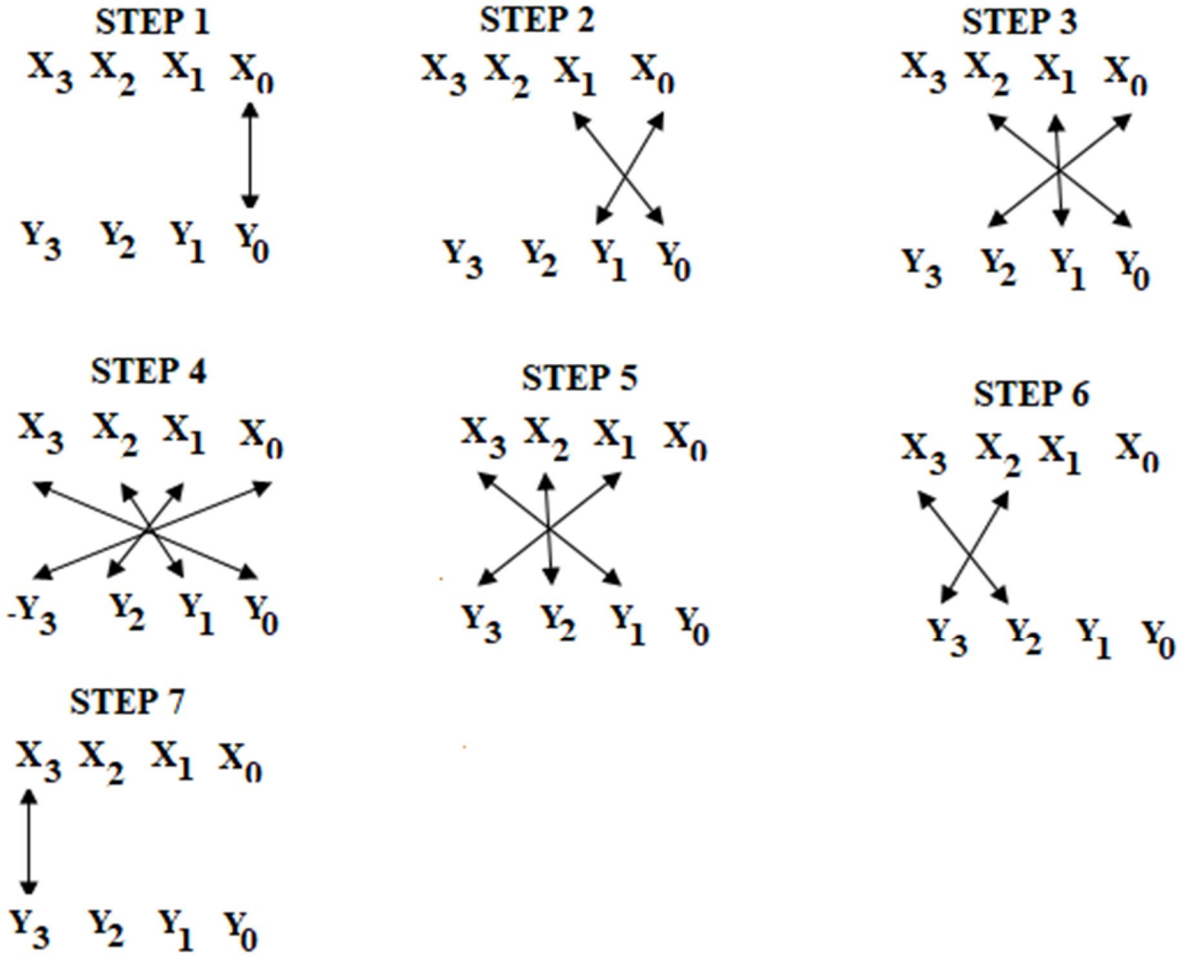

Fig2: Algorithm of UT sutra

B. Carry Look Ahead Adder

"A carry-look ahead adder(CLA) is a type of fast parallel adder used in digital logic to calculate the carry signals in advance from the input signals." They reduce carry propogation time and implement addition of binary numbers. It is also known as: carry look ahead generator or fast adder or carry predictor . It is an improvement over 'Ripple carry adder circuit'.

CLA is used to eliminate the wastage of time occur at each stage of parallel binary adder.

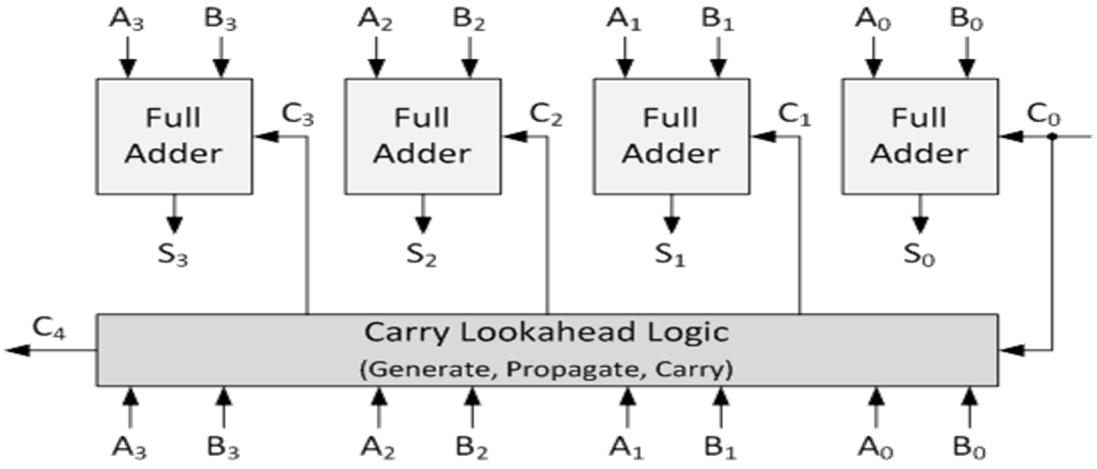

Fig3: 4-bit carry look ahead adder

C. Vedic Multiplier

Multiplication strategies that many of processors are using nowadays has stimulated by way of Vedic multiplier delivered in Indian Vedas with distinctive sixteen sutras. Vedic multiplier makes use of bit-wise multiplication with simultaneous product term finding and it's column-wise addition. It is one of the fine benchmark for fast multiplication algorithm.

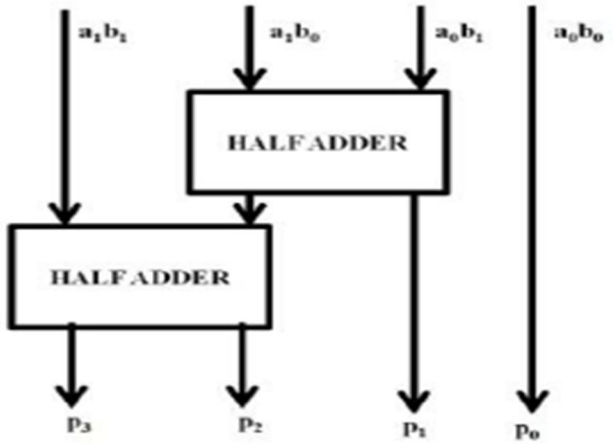

Fig4(a): 2*2 bit Vedic Multiplier Block Diagram

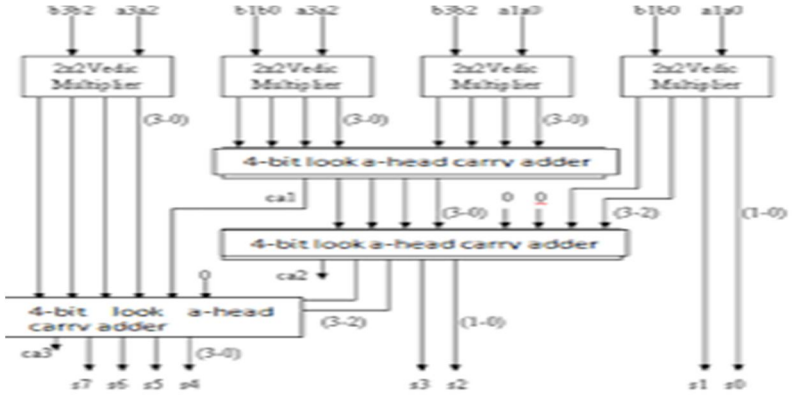

Fig4(b): 4*4 bit Vedic Multiplier Block Diagram

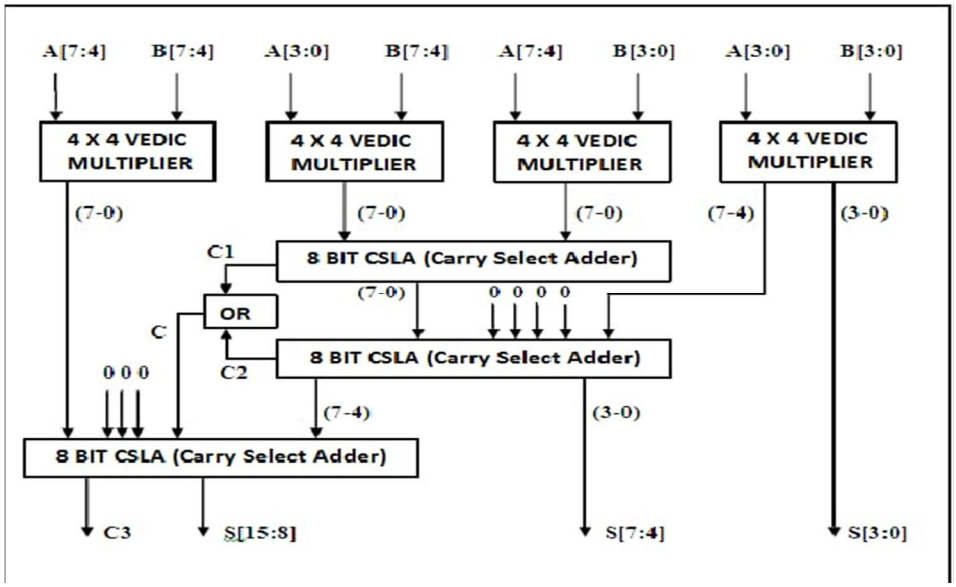

Fig4(c): 8*8 bit Vedic Multiplier Block Diagram

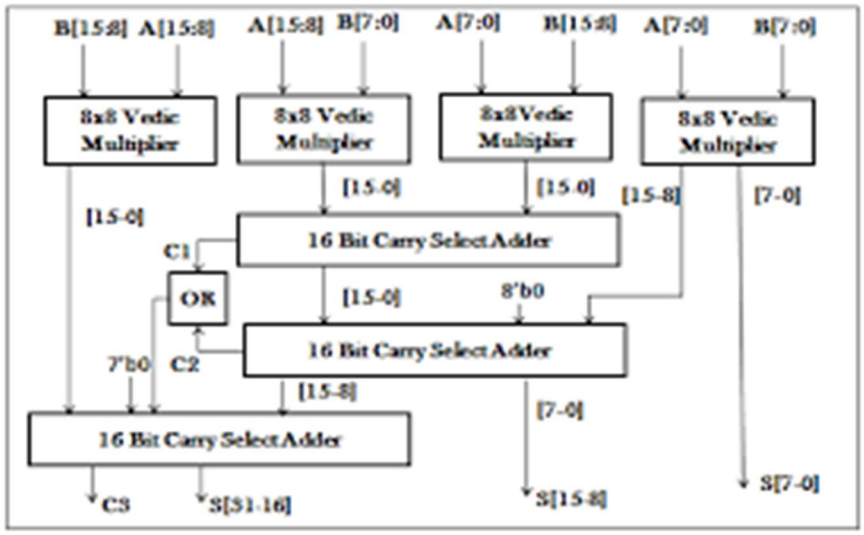

Fig4(d): 16*16 bit Vedic Multiplier Block Diagram

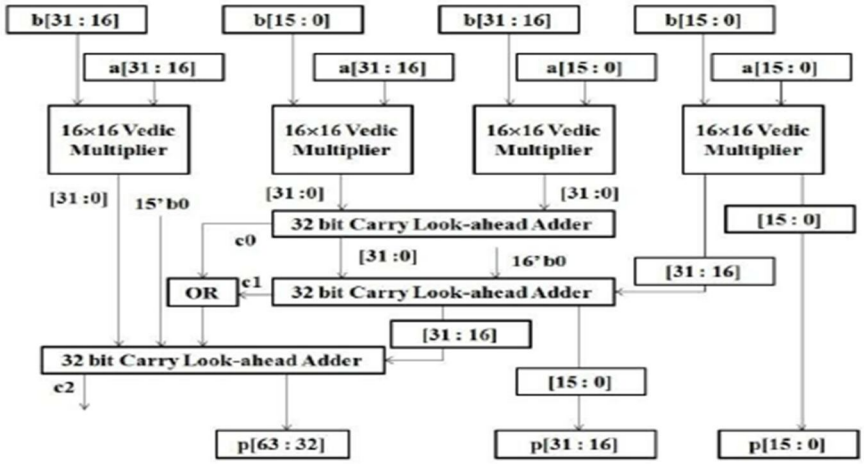

Fig4(e): 32*32 bit Vedic Multiplier Block Diagram

III. SYNTHESIS & SIMULATION

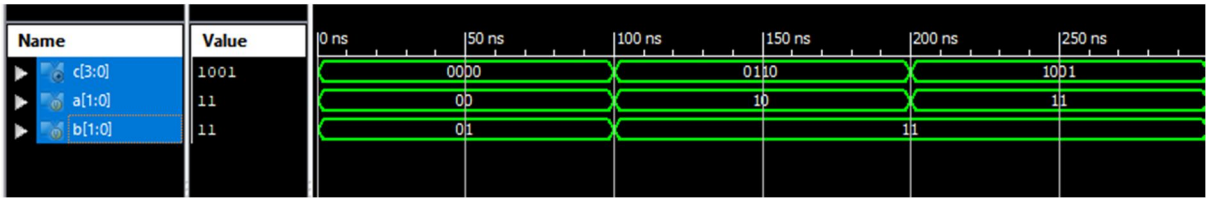

Fig. 5 Simulation Result of 2-bit Vedic Multiplier

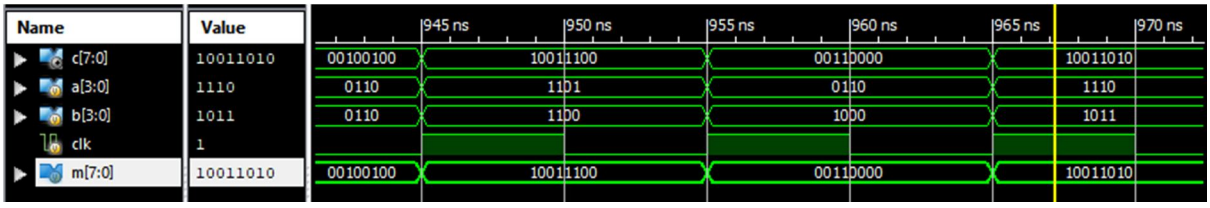

Fig. 6 Simulation Result of 4-bit Vedic Multiplier

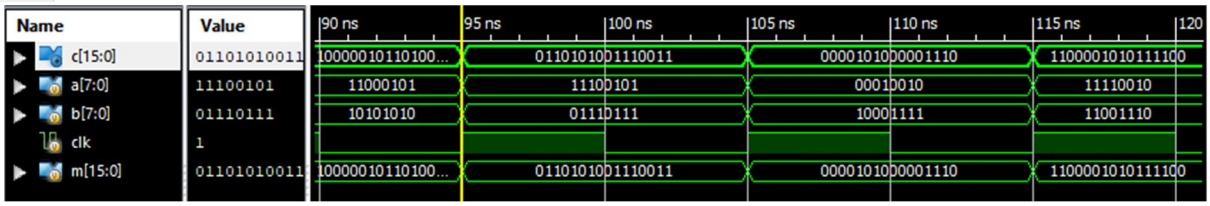

Fig. 7 Simulation Result of 8-bit Vedic Multiplier

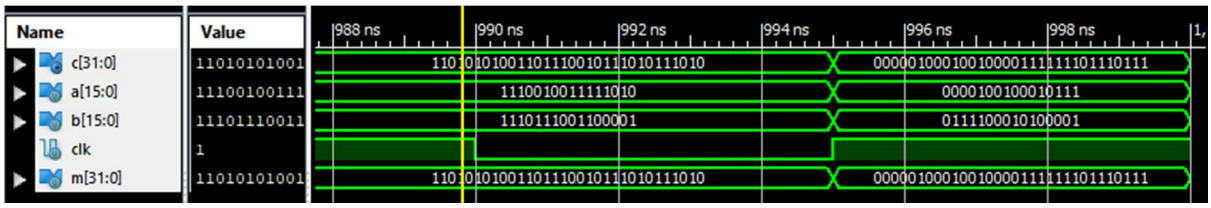

Fig. 8 Simulation Result of 16-bit Vedic Multiplier

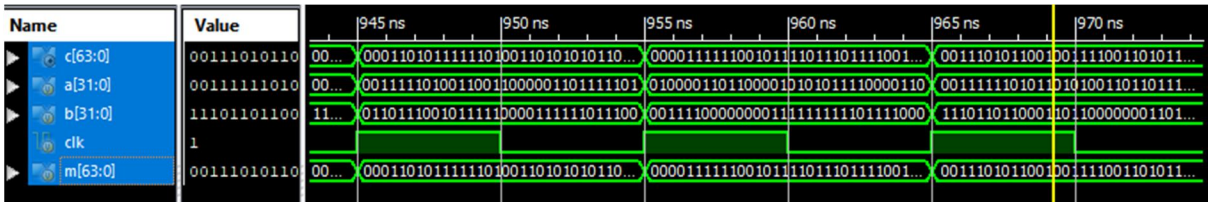

Fig. 9 Simulation Result of 32-bit Vedic Multiplier

IV. IMPLEMENTATION

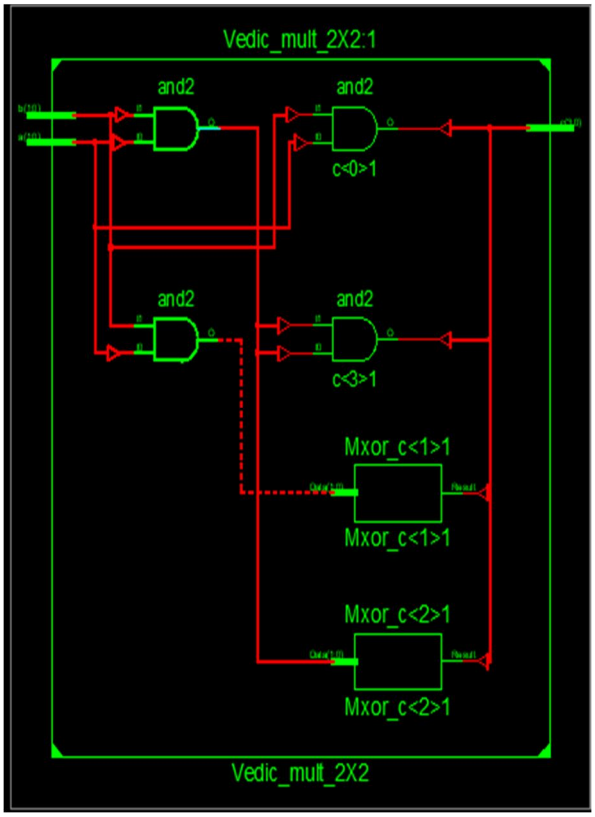

Fig.10 RTL Schematic for 2 bit Vedic multiplier

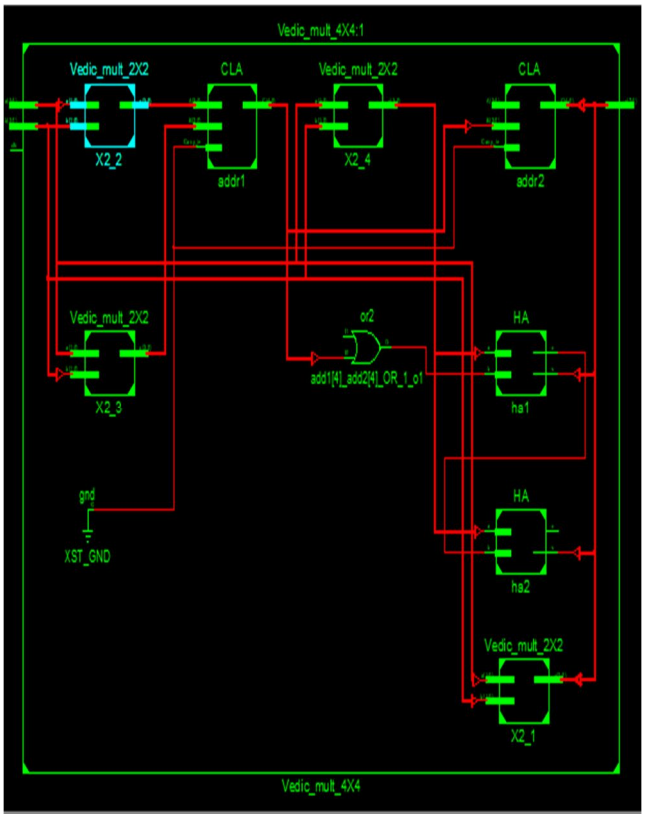

Fig.11 RTL Schematic for 4 bit Vedic multiplie

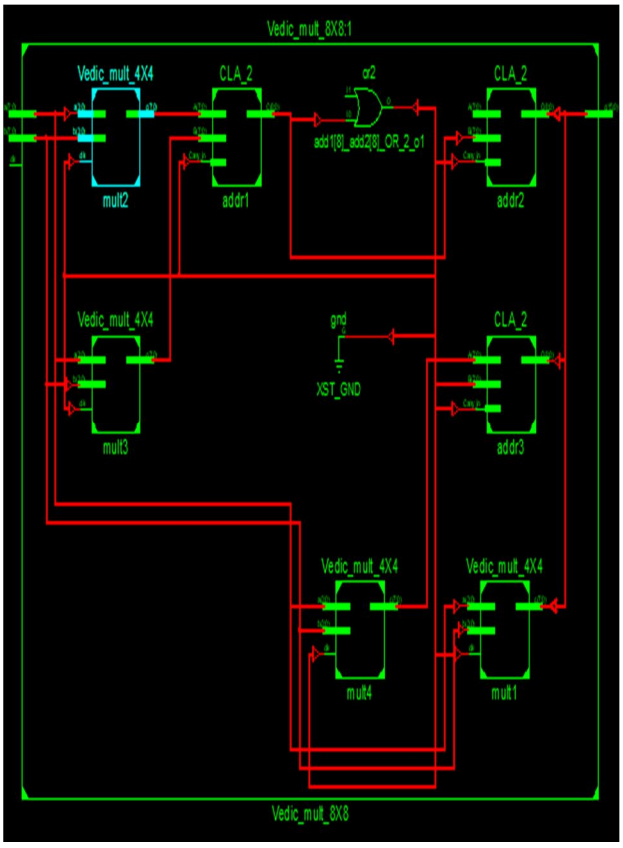

Fig.12RTL Schematic for 8 bit Vedic multiplier

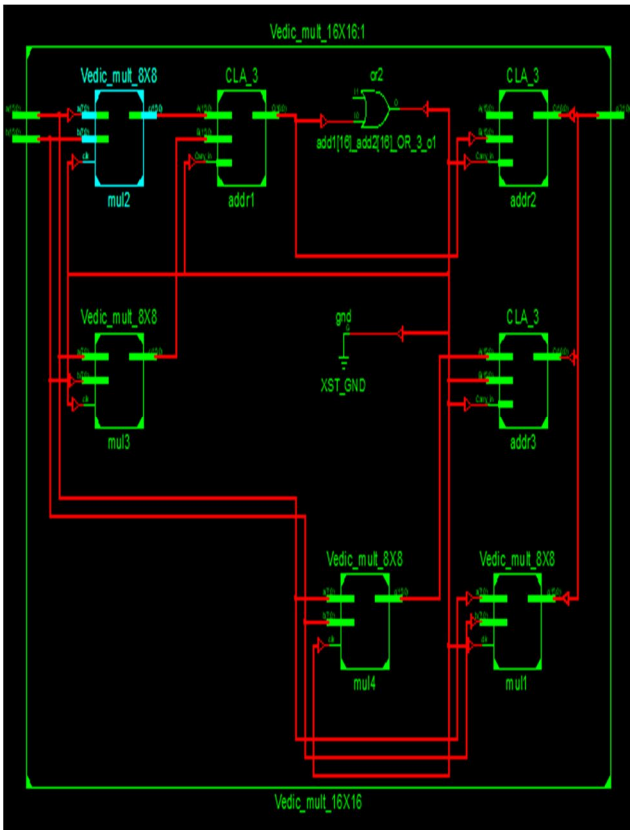

Fig.13 RTL Schematic for 16 bit Vedic multiplier

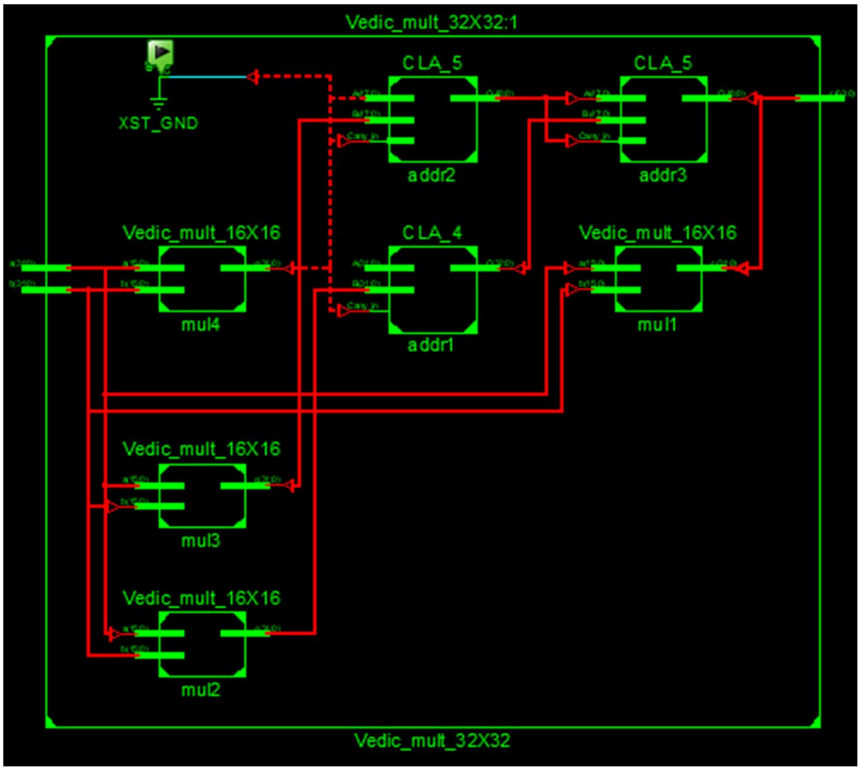

Fig.14 RTL Schematic for 32 bit Vedic multiplier

Device-Spartan6 XC6SLX45-CSG324				
Vedic Multiplier	Delay (ns)	Levels of Logics	No. of slice LUTs	Memory (KB)
2-Bit	0.948	3	4	4617500
4-Bit	3.976	8	25	4617456
8-Bit	7.965	14	129	4617516
16-Bit	17.752	32	603	4617444
32-Bit	44.652	88	2618	4618656

Table1. Using Look Ahead Carry Adder

V. CONCLUSION

This paper presents a highly efficient approach of multiplication– "Urdhva Tiryakbhyam Sutra" primarily based on Vedic mathematics. It offers us approach for modular multiplier design and certainly shows the computational advantages provided by means of Vedic methods. The computational route delay for proposed new Vedic multiplier is observed to be much less as contrast to different multiplier. Hence motivation to minimize delay is finely fulfilled. Therefore, the new Vedic multiplier is much more efficient than Array and traditional multiplier in phrases of execution time (speed).

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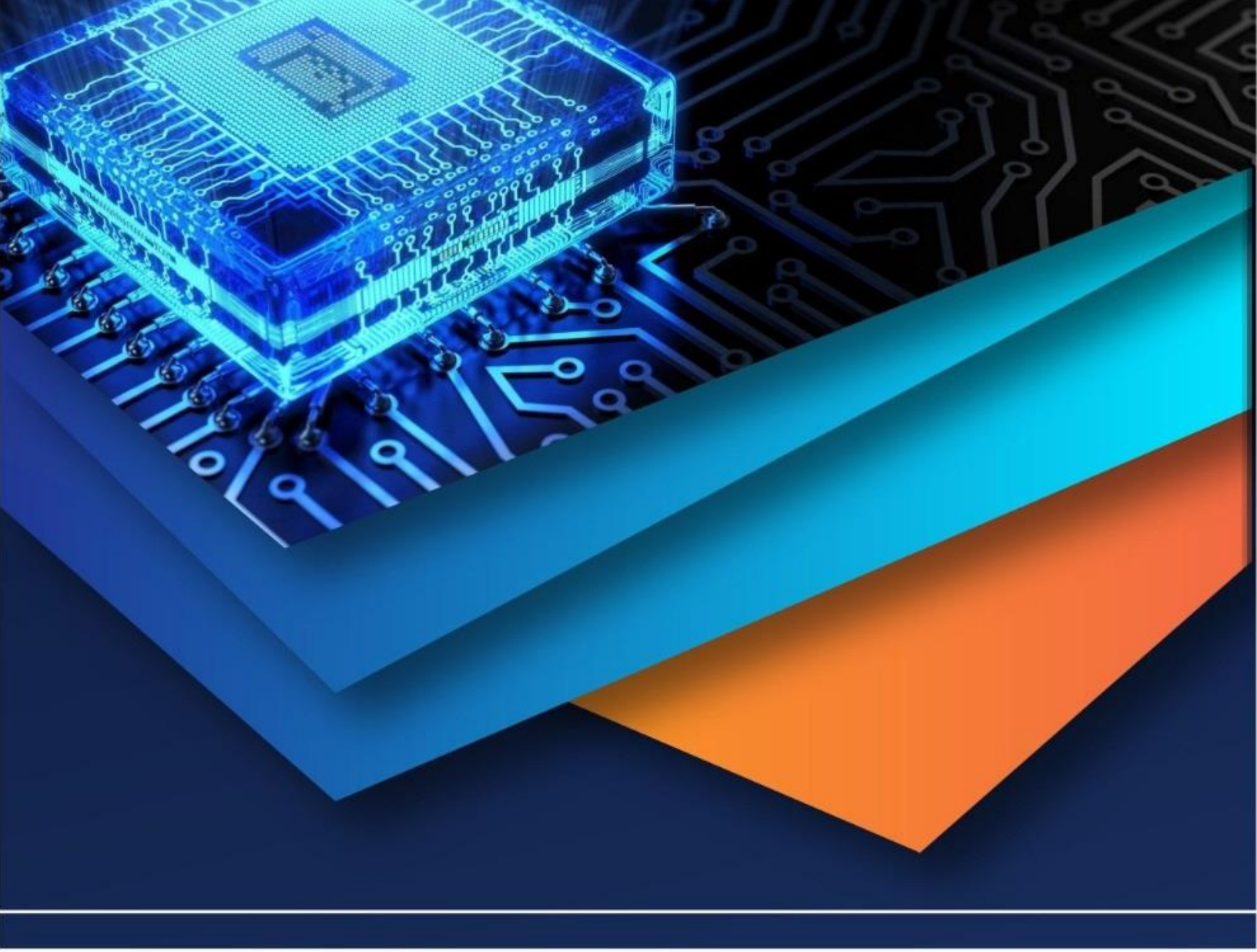

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