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Fast and Efficient VLSI Implementation of DWT for Image Compression

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Abstract: Image compression is an important technique in storage and transmission of digital images as it requires huge data. In this paper, fast and efficient FPGA based implementation of Discrete Wavelet Transform (DWT) for image compression is proposed. The proposed system is designed using Xilinx System Generator based Simulink model, simulated using MATLAB and synthesized using Xilinx ISE design suite 14.2. The design is implemented on Nexys4 DDR Board with Artix-7 FPGA. The synthesis result shows that this implementation utilizes only 120 slices at maximum operating frequency of 1102.536 MHz.
Keywords: DWT, FPGA, VLSI, image compression, System generator.

I. INTRODUCTION

Now a day, demand and progress of multimedia information is increasing speedily which then contributes to inadequate network bandwidth and memory storing capacity. Due to this, data compression becomes significant for decreasing data redundancy to save memory and transmission bandwidth. DWT based image compression offers major features such as high compression efficiency, processing error resilience and random code stream access. DWT is a kind of sub band coding where input spectrum is decomposed into set of band limited components known as sub bands. These sub bands are combined together to get the original spectrum without error. DWT has become one of the frequently used methods for signal analysis and image processing. DWT performs signal analysis that contains both frequency and time information. Due to its time and frequency domain characteristics, DWT is widely used for image compression. As convolution is based on filter bank structures in implementing DWT, more arithmetic computations and storage area is required. DWT is most commonly used DSP applications due to its computing efficiency and sufficient characteristics for non-stationary signal analysis. Fig. 1 shows general structure of DWT decomposition.

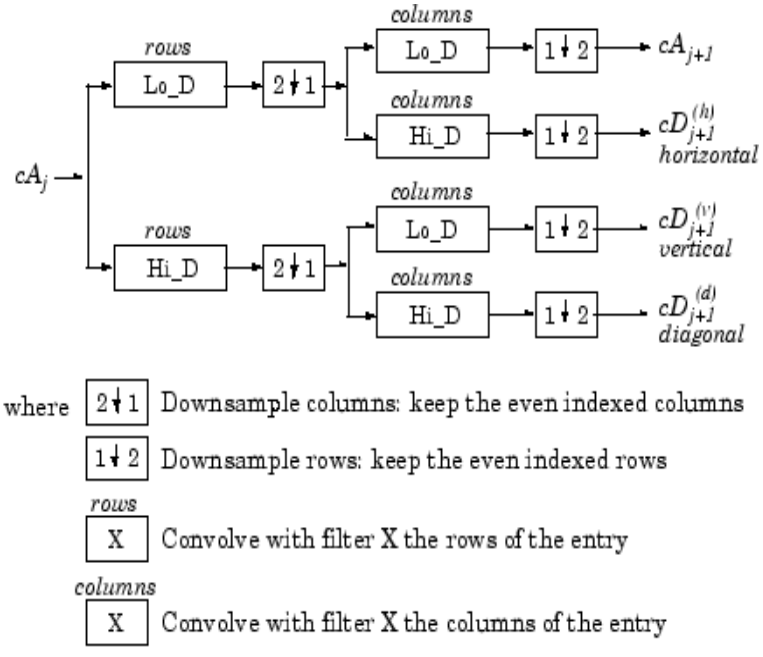


Fig. 1. DWT Decomposition structure

DWT decomposes a signal into different sub-bands so as to get the lower frequency sub-bands having finer frequency resolution and higher frequency sub-bands having coarser time resolution. Fig. 2. shows decomposition of an image at single level, two level or three level.

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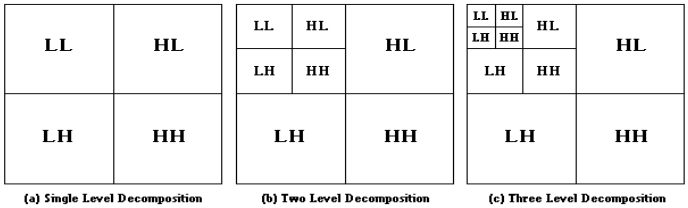


Fig. 2. Image Decomposition at single level, two-level and three-level

DWT is mainly useful for image compression as it supports features like easy manipulation of compressed image, progressive image transmission, region of interest coding, etc.

In single dimensional DWT, the signal is initially applied to low pass filters and high pass filters respectively. Then, an output of these filters, which are filtered coefficients, are down sampled to neglect an alternate coefficient. When the output of low pass filter is down sampled, it contains low frequency components of that signal which are known as approximate portion of the original signal whereas when the output of high pass filter is down sampled, it contains high frequency components which are known as detailed portion of the original signal. The filter pair low pass filter h(n) and high pass filter g(n) used for decomposition of the signal is known as analysis filter bank whereas filter pair used for reconstruction of the signal is known as synthesis filter bank. The output of low pass filter h(n) represents the approximate coefficients and is represented as:

$$y_h(n) = \sum_k x(k)h(2n-k)$$

The output of high pass filter g(n) represents the detailed coefficients and is represented as:

$$y_g(n) = \sum_k x(k)g(2n-k)$$

II. PREVIOUS WORK

Altaf O. Mulani et al [1] suggested FPGA implementation of watermarking based on DWT and AES algorithm which provides improved security. This system utilizes 2117 slices at maximum operating frequency of 228.064 MHz. Altaf O. Mulani et al [2] discussed FPGA based implementation of DWT which occupies 144 slice registers and its operating frequency is 43.630 MHz. Altaf O. Mulani et al [3] proposed a novel approach of DWT based watermarking which is consisting of AES algorithm also. Venkata Anjaneyulu et al [4] focused their interest on memory efficient FPGA or SPIHT (Set Partitioning in Hierarchical Trees) image compression technique. P.R.Kulkarni et al [5] suggested robust invisible watermarking for image authentication which is better to retain the original image. M. Nagabushanam et al [6] proposed a modified lifting scheme based 1D and 2D DWT FPGA architectures for computing the approximation and detailed coefficients of DWT. The system is implemented on Virtex -5 and it requires 1152 slices at 180 MHz. P.R.Kulkarni et al [8] proposed DWT based robust invisible digital image watermarking which does not affect the quality of original image. This method first combines information of low frequency DWT coefficients and watermark image and then the combination of this is used to extract the watermark. M. Puttaraju et al [9] proposed FPGA oriented (5/3) integer DWT for image compression. This architecture is based on lifting scheme and can be applied to 2D spatial images from payload instruments. Durga Sowjanya et al [10] proposed an area efficient and high speed VLSI architecture that utilizes 158 slices at 120 MHz. This implementation requires least computing time and also less area. It is applicable for fixed point 1-D DWT. M. Nagabushanam et al [11] suggested DWT architecture based on modified BZFAD multiplier that occupies 1152 slices at 256 MHz. According to the author, this implementation is 65 % faster and occupies 44 % less area. It also achieves 35 % power saving. Abdullah Al Muhit et al [15] proposed a DWT algorithm for image compression which supports JPEG 2000 standards.

From the literature survey, there are many researchers those have suggested different methods of implementing DWT on reconfigurable platform. Some of them have achieved better speed and some have optimized area. But there is no implementation in which both speed and area is optimized. In this paper, fast and area efficient implementation of DWT on FPGA is suggested.

III.EXPERIMENTAL RESULTS

In this implementation, Xilinx ISE Design Suite 14.2 and MATLAB 2012 tools are used. For hardware implementation, Nexys4 DDR Board having Artix-7 FPGA is used. The complete system is designed using Xilinx system generator so that implementation fulfils the requirements.

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Fig. 3. shows System generator based Simulink model for DWT implementation to get the simulation results.

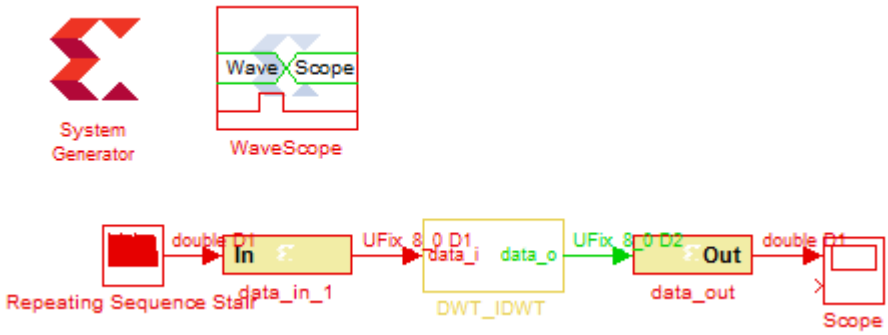


Fig. 3. System Generator based Simulink model for DWT implementation

Fig. 4. shows system generator based Simulink model for real time implementation of DWT.

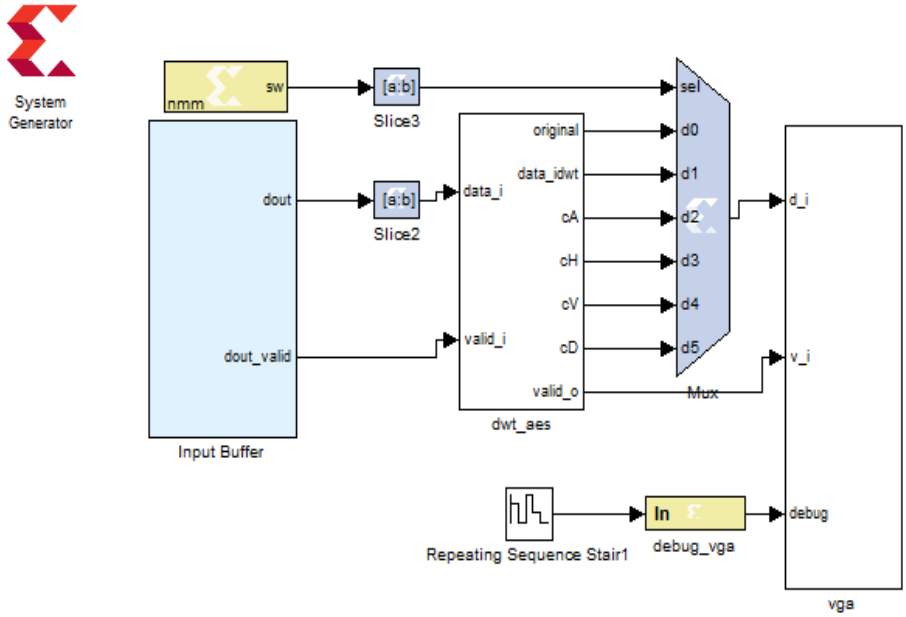


Fig. 4. System generator based simulink model for real time implementation of DWT

Fig. 5. shows system generator based test bench Simulink model for DWT implementation.

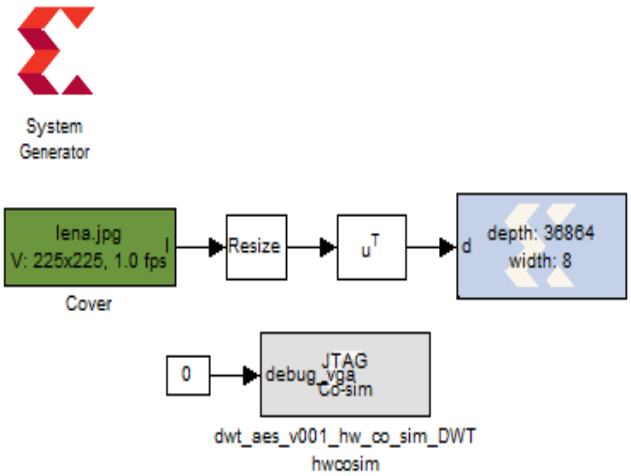


Fig. 5. Testbench model for DWT implementation

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Using system generator, the design is converted to VHDL code for getting the RTL schematic and synthesis report. Fig. 6. shows top level RTL schematic of the suggested implementation.

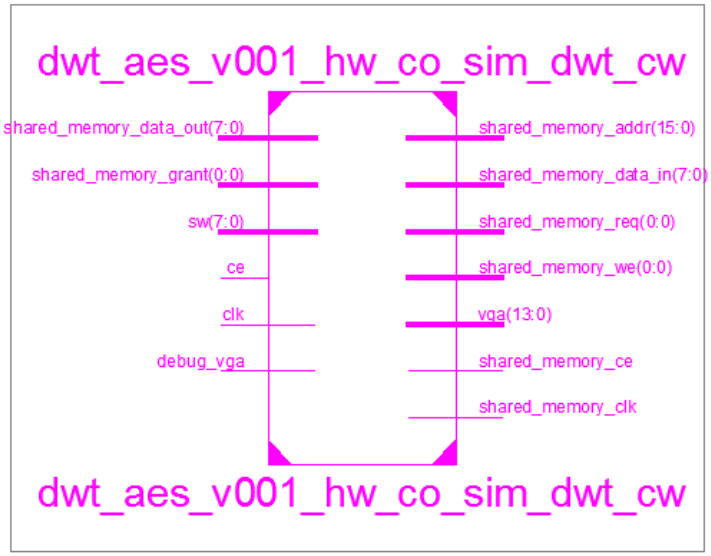


Fig. 6. Top level RTL schematic

Fig.7. shows detailed RTL schematic of this implementation.

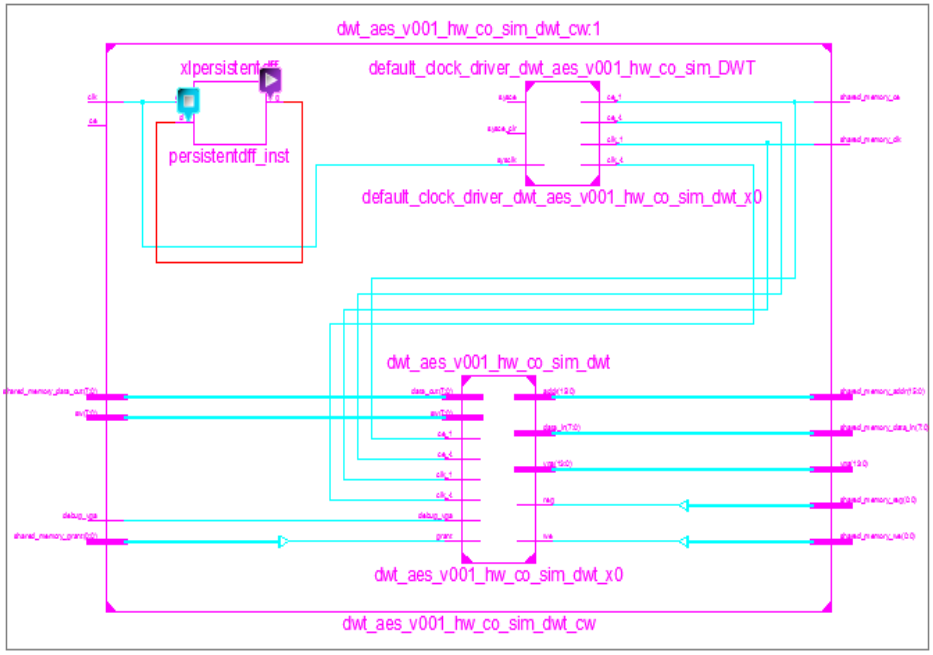


Fig.7. Detailed RTL schematic

Table 1 shows synthesis report of this implementation.

Table 1: Synthesis Report

Logic utilization	Utilized	Available
Number of slice registers	120	126800
Number of slice LUTs	2	63400
Number of fully used LUT-FF pairs	1	114
Number of bonded IOBs	65	210
Number of BUFG/BUFGCTRLs	1	32

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The maximum operating frequency achieved for this implementation is 1102.536 MHz.
Timing Summary:
Speed Grade: -1
Minimum period: 0.907ns (Maximum Frequency: 1102.536MHz)
Minimum input arrival time before clock: 0.435ns
Maximum output required time after clock: 0.883ns
Maximum combinational path delay: 1.391ns

Fig. 8. shows simulation result in terms of pixel values when an image is applied as input.

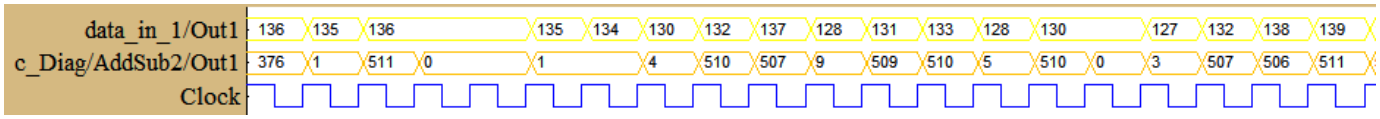
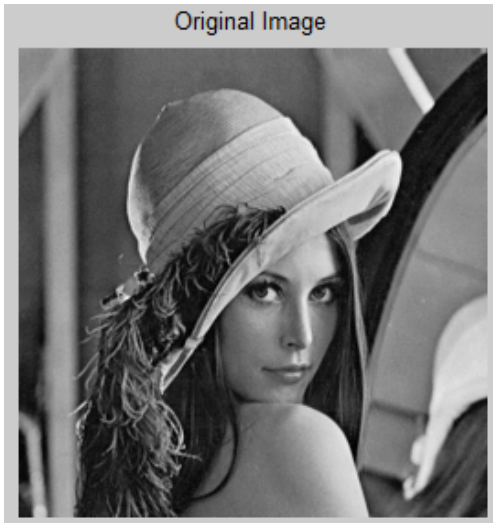
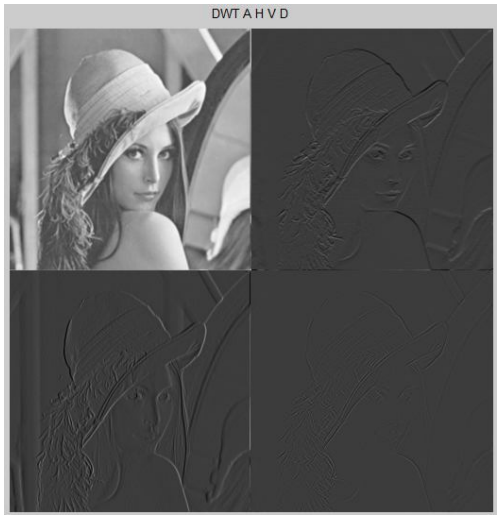


Fig. 8. Simulation result

Fig. 9. shows simulation result in terms of image.



a. Original Image



b. Single level decomposition



c. Recovered image

Fig.8. Simulation result of an input image

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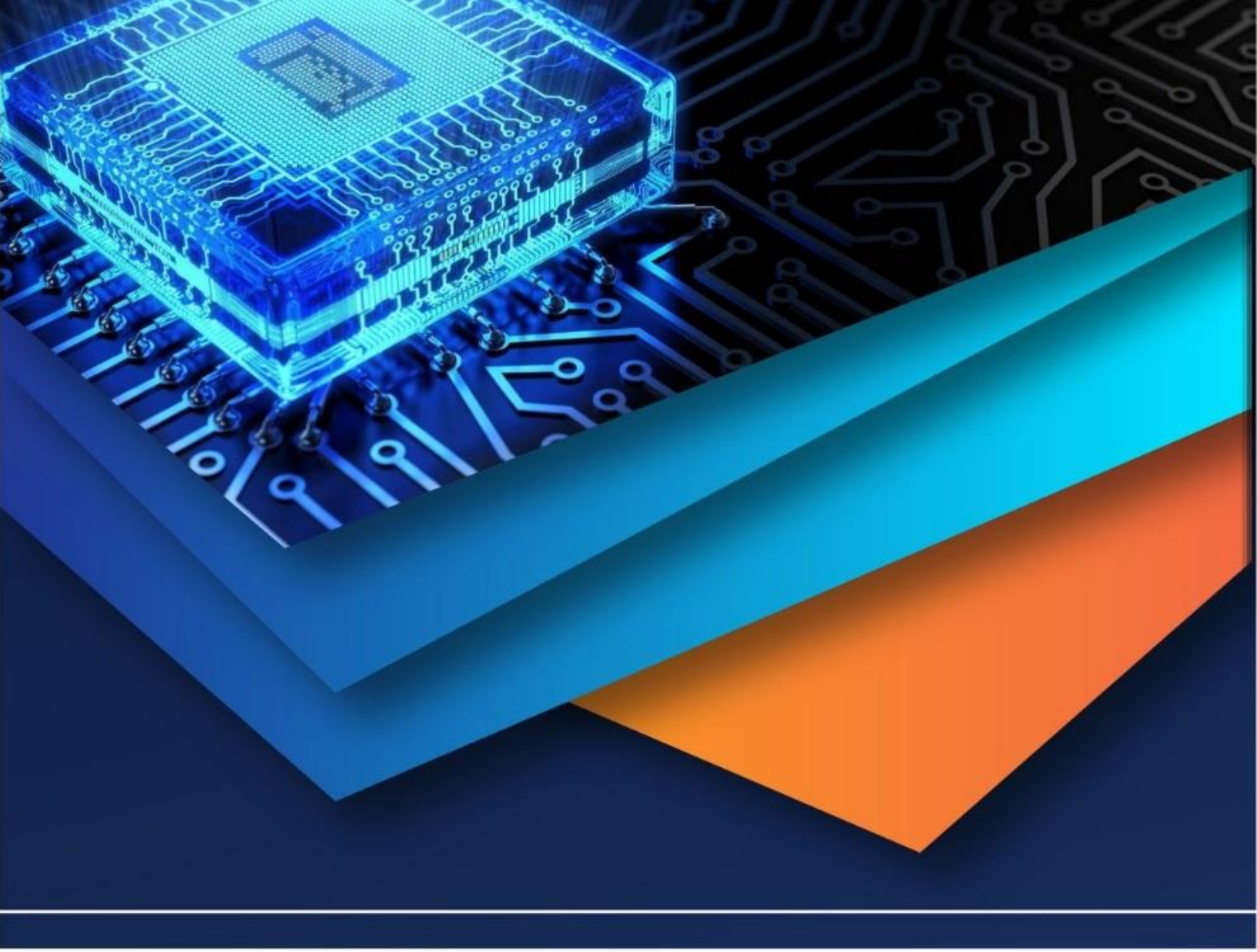
IV. CONCLUSIONS

In this paper, fast and efficient VLSI implementation of DWT algorithm is suggested. This implementation occupies very less area and achieves better speed of operation. The design utilizes only 120 slice registers at maximum operating frequency of 1102.536 MHz. As compared to the previous work done on FPGA based implementation of DWT algorithm done till date, this implementation is fast and efficient without compromising the area and quality. This implementation is suitable for image compression.

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