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A Review on Power MOSFET Device Structures

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Abstract*: The paper presents the comprehensive review on the various Power MOSFET structures that have been developed during the past decade. Various structures of Power MOSFET like LDMOS, VDMOS, V-Groove MOS, Trench Gate MOS, FLIMOS, SJ-MOS, and Strained Si MOS are studied and issues related to their performance are analyzed on the basis of following parameters: on-state resistance and breakdown voltage mainly, as trade-off should be maintained between them while designing the structure of Power MOSFET. The on-resistance should be low at high breakdown voltage for enhancing the performance of MOSFET device.

keywords: Power MOSFET, On-state resistance, Breakdown Voltage, VDMOS, SJ-MOS.

I. INTRODUCTION

The Power MOSFETs were evolved to develop the transistors that can be controlled using lower gate drive power levels. It is a three terminal device that are source, gate and drain as shown in Fig 1. It is also a voltage controlled device which is unipolar and requires very small gate current to turn on the device [1]. Electrical conductance is due to flow of single carrier, hence no issue of storage of minority carrier, therefore speed is high [2].

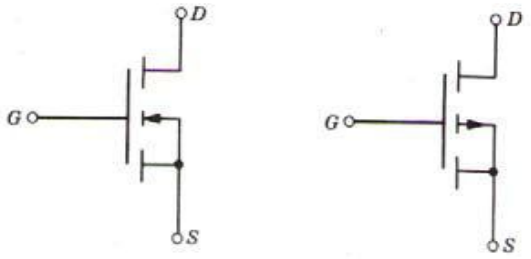

Fig. 1. Device symbol [1]

Due to its superior switching speed, it can be used as an ideal switch. The rate at which charge is supplied and removed from the MOSFET limits its switching speed [3]. It is advantageous to use power MOSFET than any other power semiconductor device due to its large Safe Operating Area (SOA), high switching speed, high input impedance [4], [5], ability to work in parallel [6] and scale devices. Other advantages are that it is a majority carrier device, it has operating frequency greater than 100 KHz and its on resistance (R_{on}) has positive temperature coefficient [1].

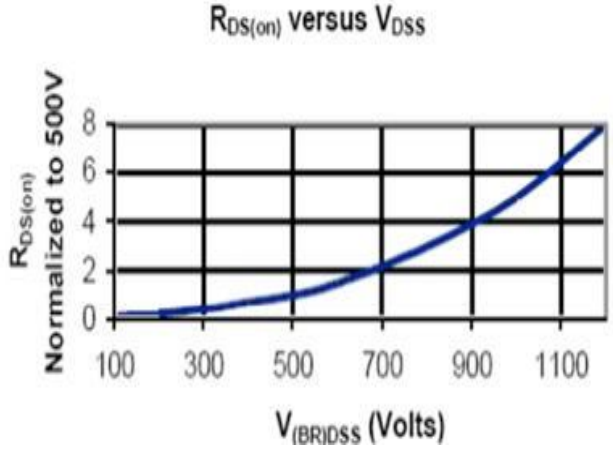

Fig. 2. Relationship b/w R_{on} and V_b [7]

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Two major characteristics associated with power devices are that they should have high breakdown voltage (V_b) in their off state and high current capacity in their on-state [7]. There is a need to maintain the trade-off between the on-state resistance (R_{on}) and breakdown voltage (V_b) while designing the Power MOSFET configuration [4]. Usually Power MOSFETs have high on state resistance (R_{on}). Relationship between R_{on} and V_b is shown in Fig 2.

II. PARAMETERS OF POWER MOSFET

A. On-state Resistance

R_{on} is the total resistance between the source and drain terminal in the on-condition and is expressed as the sum of channel resistance, spreading resistance, resistance of substrate, and bulk semiconductor resistance as shown in the Fig 3.

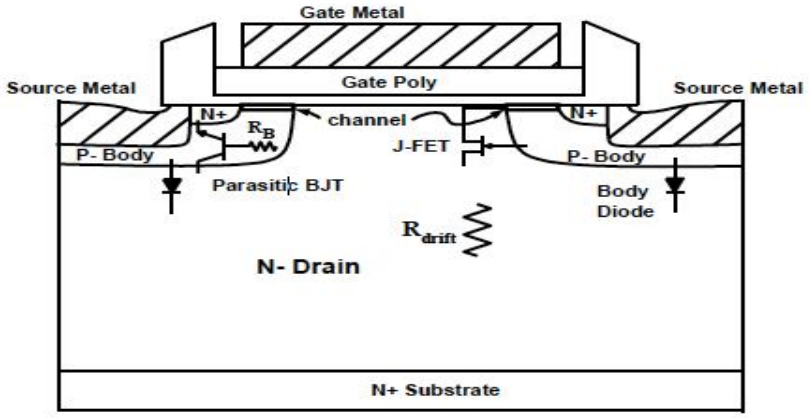

Fig. 3. N-channel Power MOSFET structure [3].

$$R_{on} = R_{ch} + R_a + R_{do} + R_{sub} . \quad (1)$$

$$R_{do} = R_{JFET} + R_d . \quad (2)$$

R_{ch} is the inverted channel resistance and it is inverse relation to the channel width, R_a is the spreading resistance of the accumulation region formed in the surface of the epitaxial layer, R_{do} is the resistance of the bulk semiconductor and the drain region, and R_{sub} is the resistance of the substrate. R_{do} is further divided into R_{JFET} and R_d, where R_{JFET} is the spreading resistance within the space between the p-body regions also called JFET region resistance, and R_d is the resistance occurring under the p-body to the top of the substrate [7]. The designed on-resistance of device should be low; if it is not, huge current will cause the huge power losses [8]. Repetitive avalanche cycles at very high temperature induces high stress in the power MOSFET, thus R_{on} can be decreased with number of avalanche cycles [9].

B. Breakdown Voltage

Breakdown voltage (V_b) is the maximum voltage between drain to source that a MOS can handle without causing avalanche breakdown. There are five driving factors that control breakdown: avalanche, reach-through, punch-through, zener, and dielectric breakdown. The value of R_{on} normally increases with increasing breakdown voltage while it is desired to have low R_{on} and high breakdown voltage values. This trade-off makes it difficult to specify the optimum doping and thickness of the n-epitaxial layer [7] because blocking voltage depends upon the doping concentration and thickness of epitaxial layer (t_{nepi}) of drift region [8], [10]. In [8] it is shown that below the t_{nepi} of 5 µm, V_b drops down, which indicate punch through. As V_b increases the half cell pitch decreases from 11 to 10 µm. But below 10 µm, V_b does not increase further, because gate is acting as a field plate which optimises the electric field distribution. V_b also increases by changing the material from Si to SiC as critical field of SiC is 8 times greater than Si as V_b is proportional to the square of critical field [8]. In [11] impact of different dopant distribution on breakdown voltage is studied by varying trench depth of device. V_b increases as trench depth gets deeper.

C. Threshold Voltage

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Threshold voltage (V_t) of a MOS transistor is defined as the gate voltage when an inversion layer is formed at the interface between the oxide layer and the substrate body of the MOSFET which gives a path for current to flow. A typical power MOSFET has V_t ranges from 2 to 4 V for high voltage devices having gate oxides thickness high and 1 to 2 V for low voltage devices with thin gate oxides [7]. The threshold voltage of device should not be so small so that suitable noise margin should be provided [8].

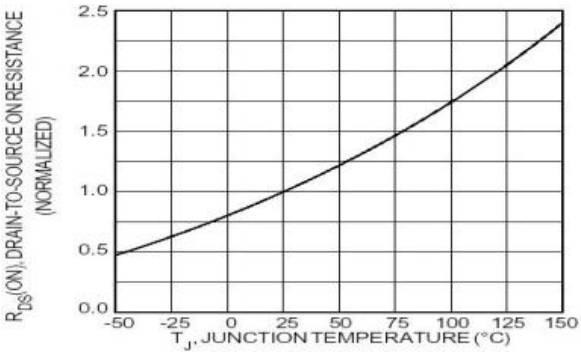

Fig. 4. On-resistance v/s Temperature [3]

D. Temperature effects

The temperature does not affect the switching speed and losses but the threshold voltage changes as it has a negative temperature coefficient, so threshold voltage decreases as temperature increases. The transfer characteristic of MOSFET depends on temperature and drain current both. Below 100 Amps current the voltage in gate source has a negative temperature coefficient and after 100 Amps, there is positive temperature coefficient. Breakdown voltage has a positive temperature coefficient and R_{on} also varies with change in temperature. As seen in Fig 4, on-resistance get almost doubles from 25ºC to 125ºC. The temperature coefficient of R_{on} is always positive because of majority carriers only. The positive R_{on} temperature coefficient ensures thermal stability while paralleling the power MOSFETs [3].

III. VARIOUS STRUCTURES OF POWER MOSFET

There are majorly two types of structures of Power MOSFETs viz. VDMOS (vertically diffused MOSFET) and LDMOS (Laterally diffused MOSFET) (also known as Planar MOSFET) on the basis of type of diffusion. VDMOS and LDMOS are derived from DDMOS (Double-diffused MOSFET) technology. Further improvements are made in these structures that are discussed below.

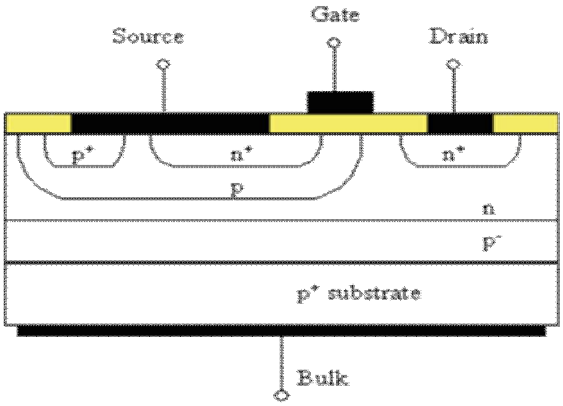

Fig. 5(a). Structure of LDMOS [7]

A. Laterally Diffused Metal Oxide Semiconductor (LDMOS)

In this structure, the current and breakdown voltage is the function of the width and length of channel respectively. Fig. 5(a) shows the basic structure of LDMOS. The main disadvantage of LDMOS is its high resistance channel; hence this structure is not used

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widely. The breakdown voltage of LDMOS ranges from 20V to 80V [7]. These devices are not suitable for power applications due to punch through breakdown [5]. In planar MOS, on-resistance can be decreased by 23% by changing half cell pitch from 10 to 6 micro-metre using gate width optimization method. Other methods include additionally doping the JFET region which decreases the on-resistance by 8.3% and by using SiC at place of Si to reduce on-resistance by 31% [8]

B. Vertically Diffused Metal Oxide Semiconductor (VDMOS)

In VDMOS the voltage rating depends upon epitaxial layer thickness and doping, while current rating depends on the width of the channel. Hence the MOSFET sustains with both high blocking voltage and high current.

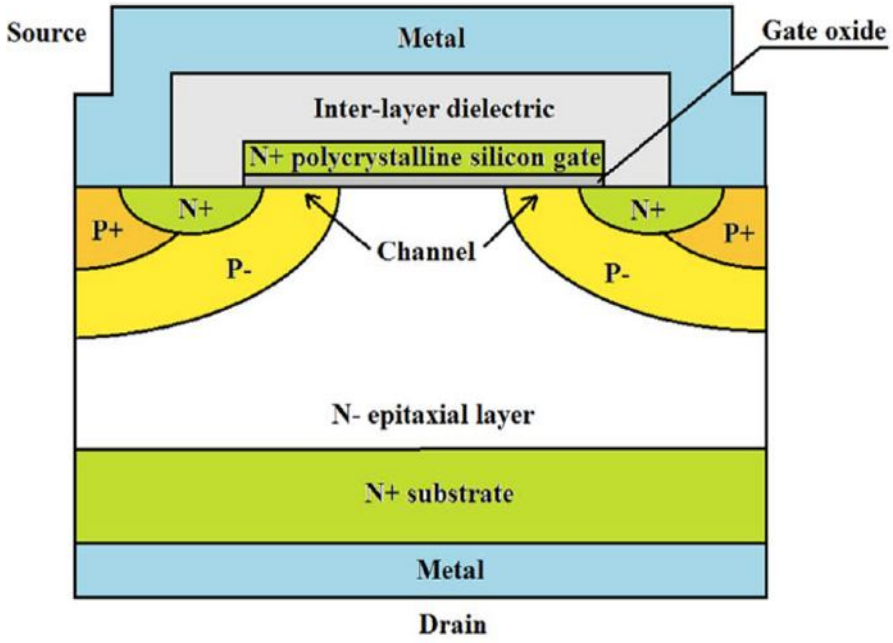

Fig. 5(b). Structure of VDMOS [13]

The vertical cross section of a VDMOS device is as shown in Fig 5(b). In this the source is over the drain, so current flows mainly in vertical direction when it is on [7]. Mostly devices are now fabricated with vertical structure because in these current carrying terminals are placed on opposite surface due to which uniform current is maintained [12]. In VDMOS there is drain to source leakage current which is due to dislocation of transistor cell in source area. This leakage can be eliminated during manufacturing of the device by reducing Plasma etching time [13]. In this structure JFET resistance is present which increases the overall on-resistance of the device [5]. This resistance can be reduced by varying the structure of VDMOS as discussed below.

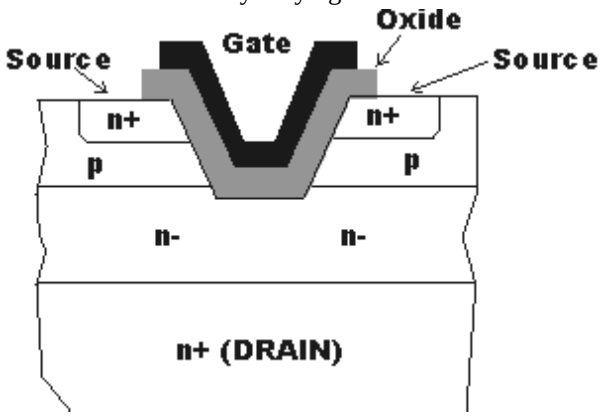

Fig. 5(c). Trench Gate MOSFET structure [7]

C. Trench Metal Oxide Semiconductor (Trench MOS)

From few years power MOSFET industry has shifted to trench-gate. These are also commonly known as U-MOSFET shown in Fig

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5(c). On-resistance decreases due to elimination of JFET region and small cell pitch [8]. In this channel is formed on the vertical sidewalls of the trench, thus current is directed along the vertical path, so JFET resistance is eliminated [4]. The specific on-resistance decreases by 60% of the planar MOS with same value of doping [8] in trench structure. It has disadvantage of switching delays due to gate charge. So gate charge has to be reduced without affecting the on-resistance and speed can be increased. The n+ - p junction is introduced in gate, which reduces the gate charge by 49.5% without changing the R_{on} [14]. An inverted L-shaped source trench power MOSFET reduces the 30% R_{on} [15]. A lateral power MOSFET in which the double extended trench gate is formed [16] gives 36% and 64% improvement in V_b and R_{on}. In this additional charges are introduced into the drift region and the substrate, which optimizes the distribution of electric field in the device. The U-trench structure has V_b ranges from 35 to 45 V with current handling capability of 1A and on resistance are 0.21 milli-ohms [7]. A novel trench power MOSFET having a buried-interface-drain is proposed in [17] which give ultralow on-resistance of 0.85 m-ohm/cm2 with a breakdown voltage of 133 V.

D. V-shaped Groove Metal Oxide Semiconductor (V-Groove MOS)

V-groove power vertical DMOSFET or VMOS consists of a vertical conduction majority carrier-based field whose channel length is determined by two diffusions [5].

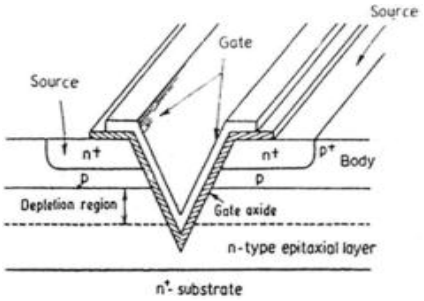

Fig. 5(d). V-groove MOS structure [7]

The V-groove structure has no JFET region, so the on-resistance of this structure is low. In this channel is formed along the sidewall of the trench structure at an angle and carrier mobility is improved by decreasing the on-resistance of device. This structure has drawback of the gate oxide breakdown due to the electric field crowding at the truncated apex of the V-groove. To avoid the oxide breakdown, P-layer is buried in N-epitaxial layer [18]. In the V-groove structure the presence of sharp edges affects the device breakdown, so it is used only for low-voltage and high current applications [4]. The breakdown voltage will be greater than or equal to 50V and on resistance is nearly 3 ohm [7]. Fig 5(d) shows the structure V-groove MOS.

E. Super-Junction Metal Oxide Semiconductor (SJ-MOS)

SJ-MOS structure increases the speed and V_b of device. In this structure drift layer is replaced by p and n pillars which share vertical boundaries, due to this modification the electric field changes that result in the large breakdown voltage.

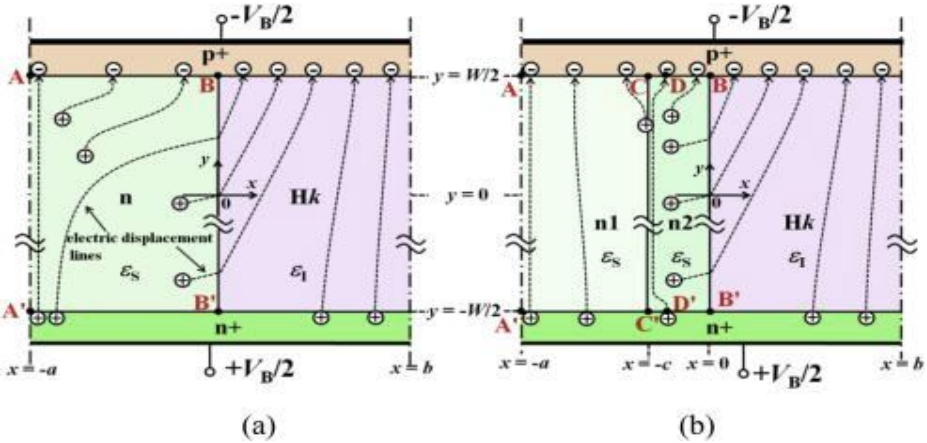

Fig. 6. Structure of (a) Conventional Hk-MOSFET and (b) Improve Hk-MOSFET [19]

This structure is based on the principle of charge compensation. The low on-resistance in this structure can be achieved by

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increasing the aspect ratio of the n and p pillars [4]. The main drawback of SJ is that V_b is sensitive to imbalance condition of charge which can be controlled by doping concentration [19]. This charge imbalance is induced by the negative charges of the current, which leads to generation of impact ionization. This drawback has been overcome by the Hk-MOSFET which attains high breakdown voltage and low on-resistance. In vertical power Hk-MOS of Hexagonal layout R_{on} decreases by 20% [20]. Further improved vertical power MOS using Hk insulator in Fig 6 [19] reduces R_{on} to 30% and 50% as compared to Hk-MOS and SJ-structure. For the same value on V_b the R_{on} is decreased to 10.1 milliohm for improved Hk structure. This structure helped in attaining the better trade-off between the R_{on} and V_b as compared to VDMOS and LDMOS [19].

F. Floating Island Metal Oxide Semiconductor (FLI-MOS)

The device with vertical floating island in the conventional power MOSFET is known as FLI-MOSFET [4].

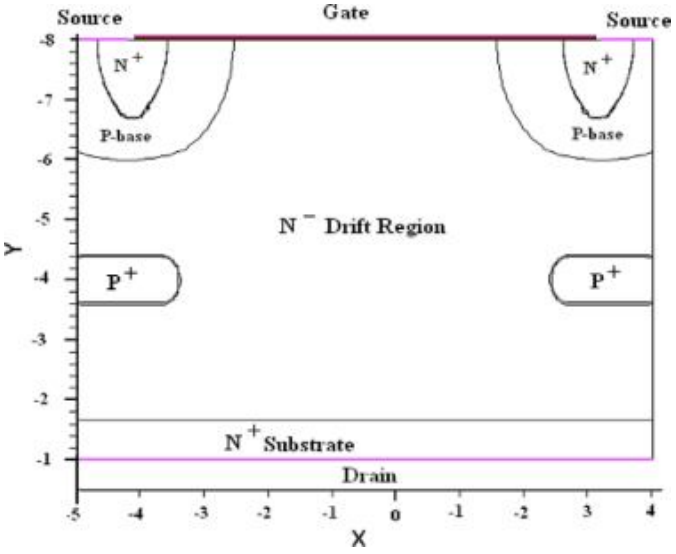

Fig. 7(a). Conventional FLIMOS structure [20]

In this structure the triangular electric field distribution in the body is divided into different sections so that the magnitude of peak electric field can be decreased by inserting P+ buried layers in the N- drift region [21] as shown in Fig 7(a). The development of depletion layer increases with the P+ floating rings, due to this the doping concentration of the N- drift region enhances such that maximum electric field is less than breakdown field and on- resistance decreases [4] with decrease in access resistance and drift resistance [20]. The conventional structure has low on resistance in the low range of voltages but there is quasi-saturation effect, so in [20] FLIMOS concept and Trench gate MOS is combined to overcome the limitations of conventional FLIMOS. This structure (in Fig 7(b)) reduces the 30% peak electric current which improves R_{on} and V_b. This device breaks the limit set for one P+ floating island and has low on-resistance that is 10 times lower [5], [20].

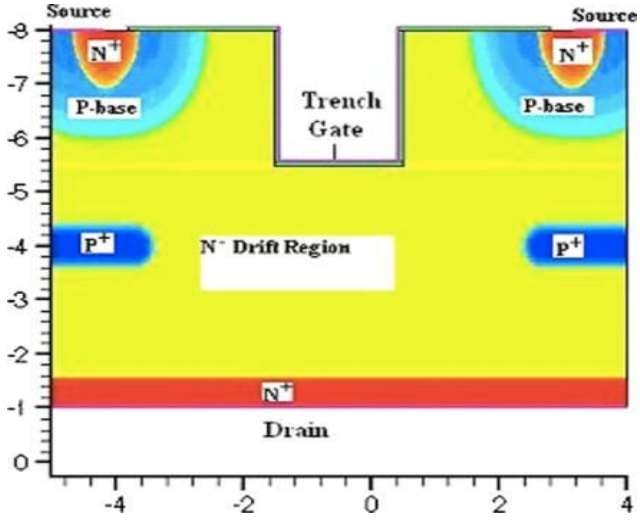

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Fig. 7(b). Trench gate FLIMOS structure [20]

Table 1 shows the comparison of various Power Metal Oxide Semiconductor Field-Effect Transistor (Power MOSFET) structures based on the On-state resistance and Breakdown voltage for different types of device structure. It can be seen from the table that by applying different types of methodology, device structures and semiconductor materials, a trade-off can be maintained between On-state resistance and Breakdown voltage, which is the desirable characteristics for a power MOSFET.

TABLE I
COMPARISON OF VARIOUS POWER MOSFET STRUCTURES

Device structure	Year	Author	Methodology	Results
LDMOS	2015	Tianhong YE	Gate width optimization	R_{on} reduces by 23% [8]
LDMOS	2015	Tianhong YE	JFET region additional doping	R_{on} reduces by 8.3% [8]
LDMOS	2015	Tianhong YE	Substituting Si with SiC	R_{on} reduces by 31% [8]
VDMOS	2014	Mihir Mudholkar	Substituting Si with SiC	High speed, R_{on} reduces by 100 times from Si [22]
VDMOS	2013	B Jayant Baliga	Substituting Si with GaN	R_{on} reduces by 1.78times and 2130times from Si, SiC [12]
Trench MOS	2015	Tianhong YE	U-Trench Gate in planar structure	R_{on} reduces by 60% with same doping [8]
Trench MOS	2015	Ying Wang	Gate charge reduced by 49.5%	Switching delay decreases without changing R_{on} [14]
Trench MOS	2010	] Jacky C. W. Ng	Inverted L-shaped source region	R_{on} reduces by 30% [15]
Trench MOS	2012	Lei Yue	Double extended Trench Gate MOS (Planar structure)	R_{on} improves by 34% and V_b improves by 36% [16]
Trench MOS	2015	Shengdong Hu	Buried Interface Drain (BID) MOS	R_{on} decreases [17]
V-Groove MOS	2016	Surbhi Sharma	Channel is formed at angle along groove	No JFET resistance, R_{on} decreases [7]
V-Groove MOS	2016	Michihiro Shintani	V-Groove with buried P-layer	Avoid oxide breakdown and V_b increases [18]
SJ MOS	2015	M. Huang	Doping Concentration is controlled	Improvement in Charge Imbalance [19]
SJ MOS	2013	Xinjiang Lyu	Conventional Hk-MOS	R_{on} reduces by 20% [20]
SJ MOS	2016	M. Huang	Improve Hk-MOS structure	R_{on} reduces by 30 % and 50% from HK-MOS and SJ-MOS [19]
FLIMOS	2005	Rakesh Vaid	P+ floating rings in drift region	Peak electric field magnitude decreases [4]
FLIMOS	2011	Rakesh Vaid	Buried P+ layer in Trench gate	Peak electric current reduced by 30%; V_b and R_{on} improves [21]
Strained Si MOS	2008	Saxena	Strain is introduced in channel using SiGe	R_{on} reduces by 28% and V_b reduces by 12% [23]
Strained Si MOS	2011	Shan Sun	Strain is introduced in channel using SiGe	R_{on} reduces by 12% with same V_b [24]

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IV. EFFECT OF OTHER SEMI-CONDUCTOR MATERIAL

Si power MOS are limited to the V_b lower than 200V [22] because of its high on-resistance at high blocking voltage. In 1980, analysis is done for the performance of power devices to the different basic material of semiconductor, in which BFOM (Baliga's figure of merit) was proposed to evaluate performance of device by replacing basic material silicon with other semiconductor materials. This analysis reports the 13.7 and 1000 times improvement in device performance when Si was substituted with GaAs and SiC respectively [12]. The comparison of different types of materials is shown in table 2.

TABLE II
COMPARISON OF GaN, SiC AND SI-SJ DEVICE [25]

Device	Rating (V)	Ron(m-ohm)
Si-SJ	600	56
GaN E-Mode	650	50
SiC DMOS	900	65
SiC TMOS	650	60

A. Silicon Carbide Metal Oxide Semiconductor (SiC-MOS)

SiC material is favored than other Wide Band Gap (WBG) material due to presence of its stable native oxide SiO_2 [6], high breakdown field strength, wide band gap, saturation velocity and thermal conductivity [22].V-Groove SiC MOS having buried P-layers model is proposed (in Fig 8) and its bias dependence of on-resistance and parasitic capacitances are represented in [18]. This structure has advantage of high electron mobility, low on-resistance and high breakdown voltage over Si device structures. SiC power MOS provide us high speed, low on-resistance (reduced 100 times as compared to Si) and better trade off [22]. But it has some limitations due to presence of interface traps, low concentration of intrinsic carrier and tunneling effects [10].

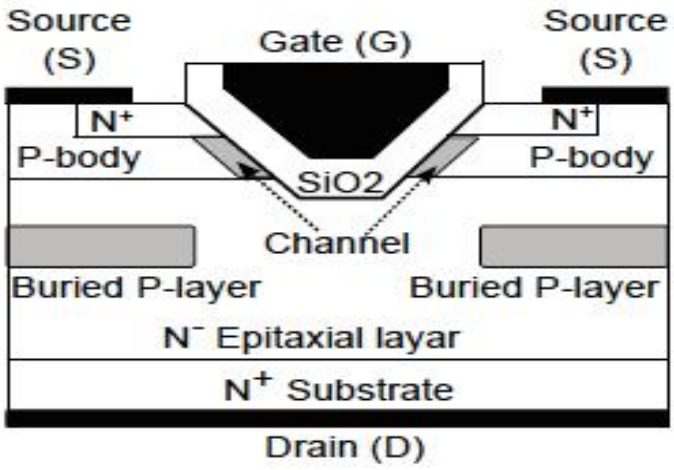

Fig8. Structure V-groove SiC MOS with buried P-layer [18]

B. Strained Silicon Metal Oxide Semiconductor (SS-MOS)

Strain engineering like tensile-strained silicon on silicon germanium is mostly used in MOSFETs to provide better carrier mobility and it also reduce the on-resistance of trench MOSFETs.

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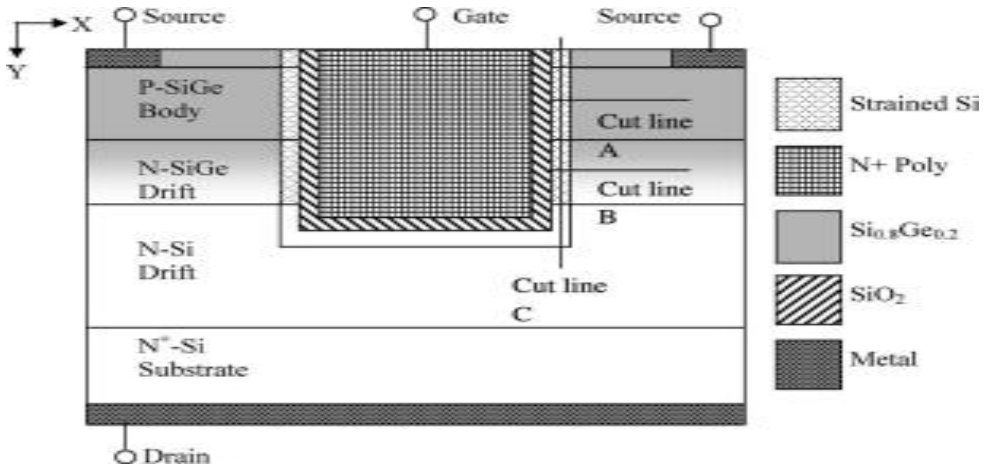

Fig. 9(a). Proposed Trench gate MOSFET with strained-Si [23]

A trench MOSFET with strained-Si channel [23] is proposed that provides better trade of between R_{on} and V_b than conventional trench structure. For producing strain in the channel SiGe is used. This proposed structure gives 28% reduction in on-resistance with very less decrease of just 12% in breakdown voltage while it also provides improvement in drive current and trans-conductance. This MOSFET uses P-type $Si_{0.8}$ $Ge_{0.2}$ in the body and N-type SiGe that is compositionally graded buffer layer to produce strain as shown in Fig 9(a). The fig 9(b) shows the structure of a new trench power MOSFET that is proposed in [24] with strained p-type Si/SiGe multilayer channel that reduce the R_{on} by 12% which maintains the same breakdown voltage and gate charge as that of conventional Si trench MOSFET structure.

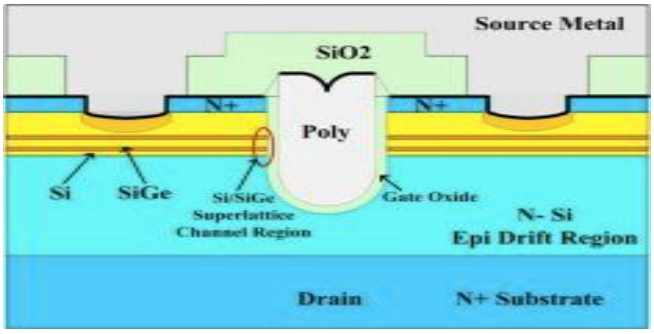

Fig. 9(b). Trench Power MOSFET with Strained silicon super-lattice like channel [24]

C. Gallium Nitride (GaN)

Gallium nitride (GaN) is WBG material whose power electronic devices are evolving as promising candidates for next generation due to better material properties such as high-electric breakdown field, high-electron saturation velocity, and high mobility. GaN has larger critical electric field strength; hence larger breakdown voltage can be achieved using this material. The ideal R_{on} of vertical GaN device is 1.78 times smaller as that of SiC device and 2130 times smaller than of Si [12]. The GaN on Si show better performance in R_{on}, switching speed, thermal performance, chip size and cost [25]. Fig 10 shows the comparison of V_b with R_{on} and Critical field strength of GaN, SiC and Si material.

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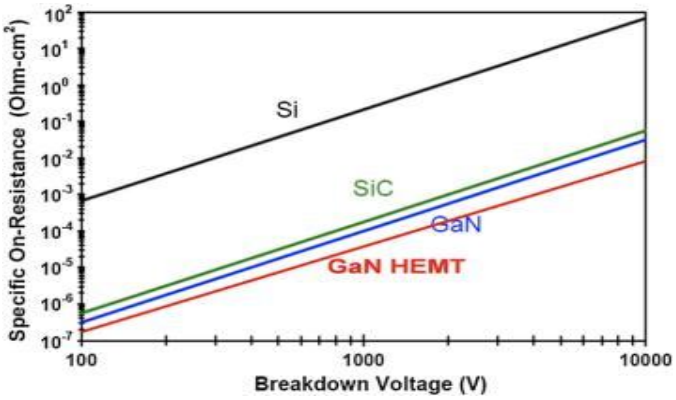

Fig. 10(a). Comparison of breakdown voltage and on-resistance [12]

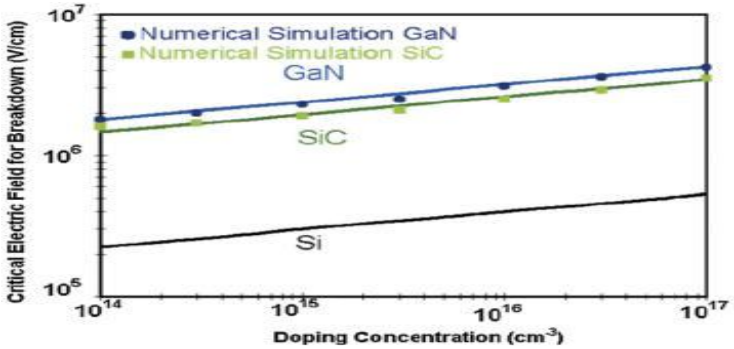

Fig. 10(b). Critical electric field strength for doping concentration [12]

V. CONCLUSION

This paper provides the study of different Power MOSFET structures and various modifications made in these structures to maintain a trade-off between R_{on} and V_b. Si-SJ structure gives ultra low on-resistance at high breakdown voltage as compared to other structure with Si as their basic material, while performance of other structures gets improved by using GaN and SiC material. In recent years, many modifications have been done in the LDMOS, VDMOS, and Trench gate MOS, FLIMOS, and SJ-Si structures for improving the performance of device by reducing the On-state resistance. The performance of these systems could be increased by using a hybrid combination of the above structures and by the use of other semiconductor materials as discussed earlier in this paper.

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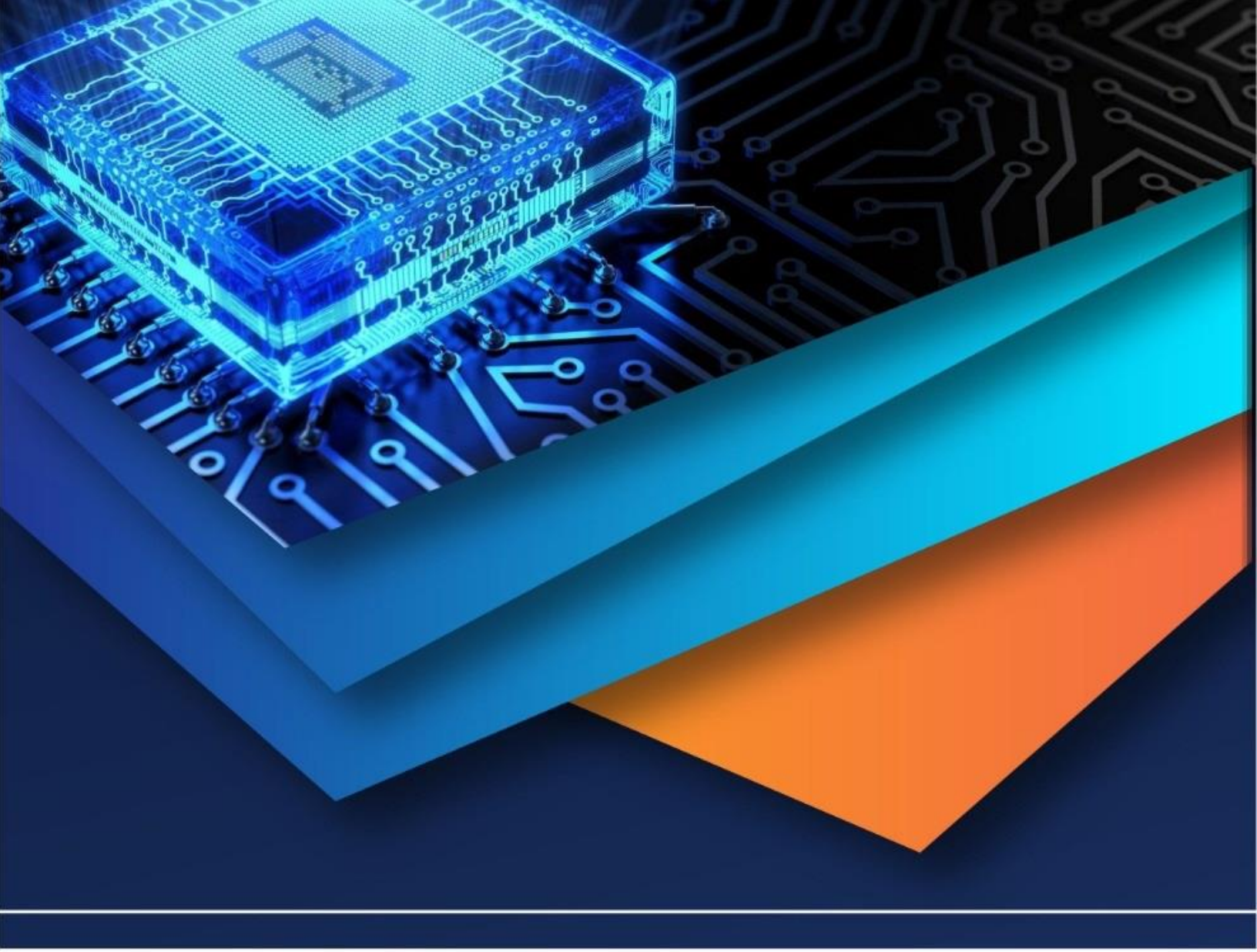

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