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Crosstalk Analysis In Carbon Nanotube Bundle Interconnects

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Abstract: ***With the advanced technology nodes, huge number of functionalities is integrated in a Very Large Scale Integration (VLSI) chip. Thus, the density of long interconnects is increased exponentially that connect millions of active devices on a chip, is posing a serious bottleneck in terms of substantial capacitive and inductive couplings. Hence there appears a dire need to search a potential material for future generation of VLSI interconnects that will be capable of exhibiting minimized propagation delay, power dissipation and crosstalk effects. Many researchers show that carbon nanotubes are the best promising candidates for next generation of VLSI interconnect. Carbon nanotubes are preferred over copper interconnect due to their high current carrying capacity and high thermal conductivity. The present work explores the possibilities of alternative interconnect material for future VLSI interconnects. The most promising alternative for copper interconnects turns out to be Carbon Nanotube (CNT). An investigation of the control of crosstalk induced noise voltage (functional crosstalk noise) in capacitively coupled interconnects of SWCNT bundle, at the far-end of victim line, for fixed pitch and varying interconnect dimensions at 22nm technology node, have been carried out. A similar analysis is performed for copper interconnects. Result reveals that, compared to SWCNT bundle interconnects, copper interconnects has higher coupled noise voltage levels.***
Keywords: Carbon nanotube, Very large scale integration, Copper, Single wall carbon nano tube, Crosstalk.

I. INTRODUCTION

Interconnects are the metal wire that is accustomed connect element on a VLSI chip, to attach multiple structures on a system board. It controls noise, reliability, timing, design, functionality and power.

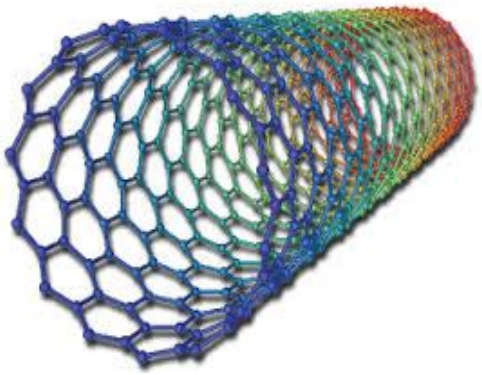

Fig.1 Carbon nanotube

Carbon nanotubes (CNTs) are carbon molecules with cylindrical shape having properties such as great mechanical, thermal, chemical, and electrical properties. They are best field emission emitters, 100 times stronger than steel and can withstand a current density of more than 10^{10} A/cm^2.[4]

Carbon nanotubes are of two types: single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs). SWCNTs were discovered in 1993, having a diameter nearly 1 nm and length thousand times larger and of the order of centimeters. The structure of SWCNT can be anticipated by bundling a thick layer of graphite into a consistent cylinder. The way the graphene sheets wrap can be

denoted by a duo of indices (n, m) named as chiral vector. The relationship between n and m defines the three categories of CNTs namely, zigzag, chiral, and arm chair.

MWCNTs consist of several layers of graphite rolled in to form a tube with an interlayer spacing of 3.4 Å. The outlying diameter of MWCNTs ranges from 1 to 50 nm while the inner diameter is of few nanometers.

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II. EQUIVALENT CIRCUIT MODEL FOR AN ISOLATED SINGLE WALLED CARBON NANOTUBE (SWCNT)

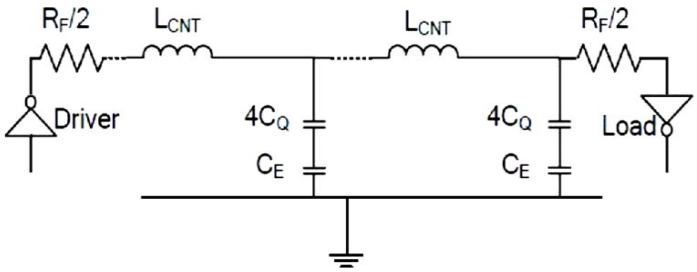

Fig.2 Equivalent circuit model for an isolated SWCNT

A. The equivalent circuit model for an isolated single-walled
CNT is shown schematically in Figure 2

1) R_F is the fundamental resistance,
2) L_{CNT} is the total inductance,
3) C_E is electrostatic capacitance
4) C_Q is quantum capacitance

The fundamental resistance R_F, is equally divided among the two contacts on both side of the nanotube. It can be given as

$$R_F = \frac{h}{4e^2}$$

B. The total capacitance of a nanotube consists of two component
1) Electrostatic capacitance (C_E)
2) Quantum capacitance (C_Q)
Electrostatic capacitance is the intrinsic plate capacitance of an isolated carbon nanotube, whereas the quantum capacitance accounts for the electrostatic energy stored in the CNT when it carries current.

$$C_E = \frac{2\pi \in}{\ln \frac{y}{d}}$$

$$C_Q = \frac{2e^2}{hV_f}$$

Here y is distance of CNT from ground plane, V_F is Fermi velocity in graphite (8×10^5 m/s), ε is dielectric permittivity, and d is CNT diameter.

C. The total inductance of a CNT consists of two components
1) Magnetic inductance (L_M)
2) Kinetic inductance (L_K)

The magnetic inductance per unit length is given by:

$$L_M = \frac{\mu}{2\pi} \ln \frac{y}{d}$$

Apart from magnetic inductance, another inductive component exists due to the kinetic energy of the electrons. The kinetic inductance per unit length can be give as [4]

$$L_K = \frac{h}{2eV_f}$$

III. EQUIVALENT CIRCUIT MODEL OF COPPER INTERCONNECT

The resistance of the copper interconnects of length L is given by following equation

$$R = \frac{\rho l}{wt}$$

Where, ρ is the resistivity of material (in Ω-m), l is the length of interconnect w is the width of interconnect and t is the thickness of interconnect. The total effective capacitance of the copper interconnect is given by

$$C_g = \varepsilon\left[\frac{w}{h} + \left\{2.22\left(\frac{s}{s+0.7h}\right)^{3.19}\right\} + \left\{1.17\left(\frac{s}{s+1.51h}\right)^{0.76}\left(\frac{t}{t+4.53h}\right)^{0.12}\right\}\right]$$

Where Ɛ is the dielectric permittivity, s is the inter wire spacing of copper. Inductance associated with copper interconnect is given by

$$L_s = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{w+t} + \frac{1}{2} + \frac{0.22(w+t)}{l}\right]$$

Where μ_0 is the permeability.

IV. CROSSTALK ANALYSIS

Crosstalk effect between coupled interconnects becomes increasingly valuable in a VLSI chip as technology advances to Giga Scale Integration (GSI) level. This is due to the fact that the interconnect density has grown and dimensions have shrunk, as the chip size increases in scaled Deep submicron (DSM) CMOS technologies. These wires do not scale in length with technology scaling and parasitic impedance parameters of these wires increase with the length of interconnects. The parasitic impedance parameters of interconnect and device depend on materials, geometry and technology. Hence, the long interconnects pose severe challenges viz. crosstalk , delay and power dissipation for high performance VLSI design.

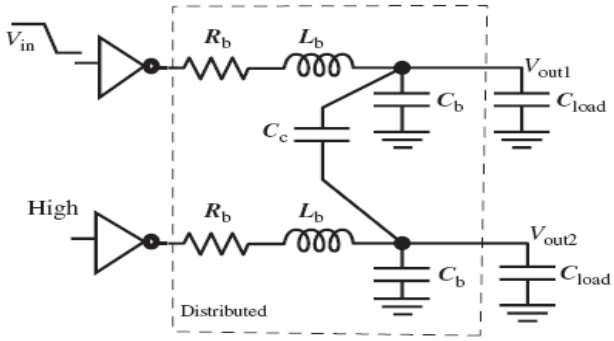

Fig.3 CMOS gate driven capacitive coupled interconnects

The above circuit parameters and coupling capacitance of coupled interconnect of copper are calculated by appropriate use of the expressions from Equations and data obtained from Table1. For overshoot analysis, the victim net (i.e. the crosstalk affected net) is kept fixed at logic 1 and the aggressor net (i.e. the net that cause crosstalk on victim) is switched from logic 1→0. The aggressor line CMOS driver has pMOS width (W_p) double than nMOS width (W_n) while the victim line is grounded at the input through a linear region equivalent driver resistance and the size of CMOS driver nMOS is set to the minimum size of transistor. In this analysis, the width (w) and thickness (H) of interconnect are assumed to be 32nm and 96nm respectively, and space(s) between two interconnect is assumed to be 32nm.

The simulation for interconnects are carried out on Tanner EDA tool at 22nm technology at 1GHz frequency. We analyzes how crosstalk noise voltage (functional crosstalk noise) in capacitively coupled Single Walled Carbon Nanotube (SWCNT) bundle interconnects, at the far end of victim line, is controlled under the influence of interconnect dimensions such as space(s) and width(w) for fixed pitch, using proposed inter coupling capacitive model. A similar analysis is performed for copper based interconnect and comparison is made with result obtained for CNT based interconnect at 22nm technology. The SPICE simulation results reveal that the crosstalk noise voltage level at the far end of victim line in CNT bundles is significantly low compared to that in conventional metal(copper) conductors in three different cases to keep the pitch (s+w) fixed but varying the value of interconnect spacing and width.

Case-1: Space (s) between two interconnect equals to s + w/2 = (3w)/2=48nm and Width (w) = w - w /2=w/2=16nm.

Case-2: Space (s) between two interconnect equals to 32nm and Width (w)=32nm.
Case-3: Space (s) between two interconnect equals to s - (w /2) = w /2=16nm and Width (w) =w + (w/2) = 3w/2 = 48nm.
In all three cases pitch (s + w) is kept fixed at 64nm but interconnect dimensions are varied. Data given in Table1 are used for the calculations of Resistance, Induction, Capacitance and coupling capacitance for CNT and Cu.

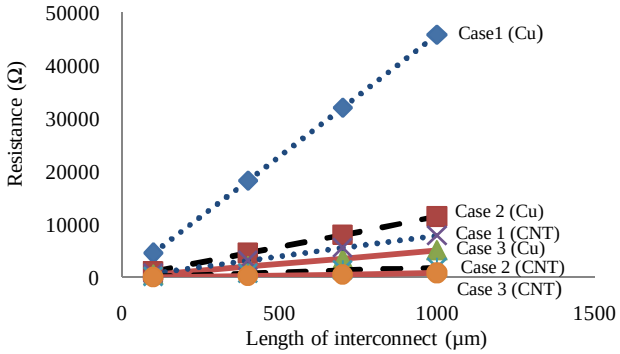

Fig.4 Variation of resistance as a function of interconnect length at different dimension between adjacent interconnects for 22nm technology.

The above fig.4 shows how the resistance varies with interconnect length for three different dimensions. It can be seen that interconnect of larger width in case 3, when used as interconnect will have smaller line resistance for both CNT and copper. It shows that in various length and width of interconnects the resistance of bundle SWCNT is several times lower than that of copper based interconnects.

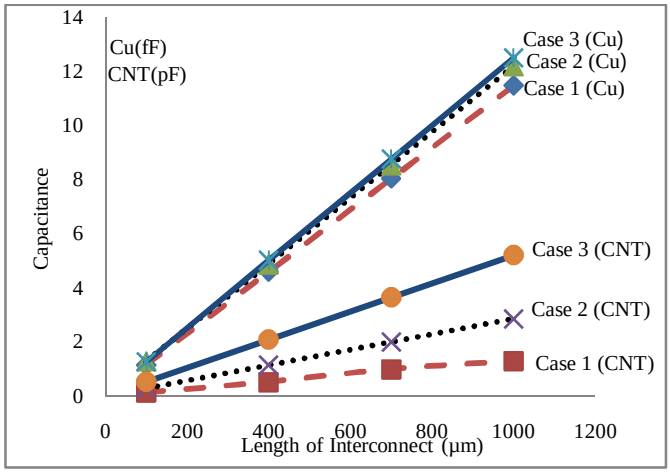

Fig.5 Variation of capacitance as a function of interconnect length at different dimension between adjacent interconnects for 22nm technology.

Fig.5 shows the variation of total interconnect effective capacitance (equivalent ground capacitance) as a function of interconnect length for different adjacent interconnects dimension. Interconnect capacitance increases with decrease in space between adjacent interconnects and decreases with scaled down dimensions.
It is observed that a bundle composed of tubes has larger effective capacitance in all three cases compared to the copper based interconnect. Since, the cylindrical surface area of the CNTs at the edge of a bundle exposed to the surrounding interconnects is larger than the corresponding surface area for a copper (Cu) interconnect with straight edges. Therefore SWCNT bundle has larger effective capacitance as compared to copper of equivalent dimension.
Fig.6 illustrates the dependence of inductance on interconnect length. Inductance increases with increase in space between interconnects and decreases with increase in width of interconnects in all three cases. It has been observed that a bundle composed of tubes has smaller inductance in all three cases as compared to copper .

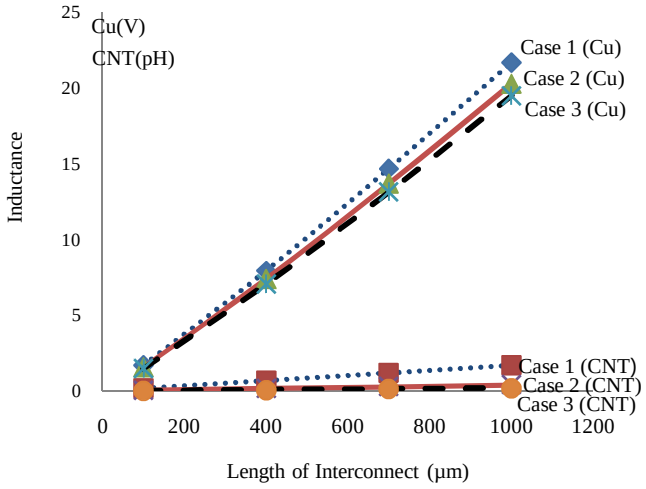

Fig.6 Variation of Inductance as a function of interconnect length at different dimension between adjacent interconnects for 22nm technology.

Results are obtained in Fig.4, 5 and 6 indicate that a densely packed interconnects have larger capacitance but reverse is true for inductance and resistance.

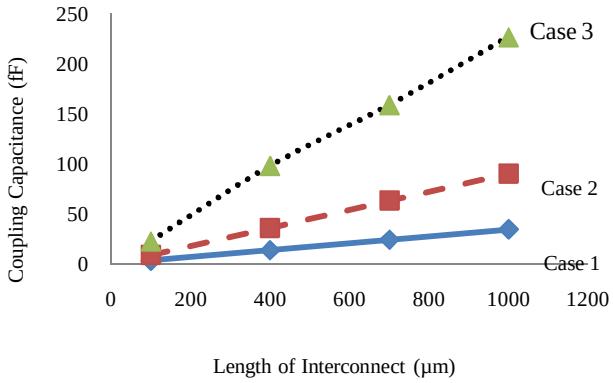

Fig.7 Variation of coupling capacitance as a function of interconnect length at different dimension between adjacent interconnects.
Fig.7 shows how inter coupling capacitance between adjacent interconnects vary as a function of interconnect length for three different dimensions. Coupling capacitance increases with decrease in space between adjacent interconnects and decreases with scaled down the width of interconnects. Coupling capacitance increases significantly with increase in length of interconnect. Results also reveal that copper based interconnect has higher value of coupling capacitance than a CNT bundle counterpart in three different cases.

Table 6.5 Comparison between the crosstalk noise of Cu and CNT. Length of interconnect=1mm,C_{Load}=0.14fF, Technology:22nm

Interconnect Dimensions	Coupling Capacitor	COPPER (mV)	CNT (mV)
Case 1	0.034pF	80.76	0.205
Case 2	0.0903pF	166.37	0.219
Case 3	0.227pF	190.99	0.191

The table 2 also provides an account of crosstalk noise voltage corresponding to three different cases of copper coupled interconnects.
As compared to SWCNT bundle interconnect for all three cases, copper has higher coupled noise voltage levels due to larger value of coupling capacitance as shown in Fig.7.

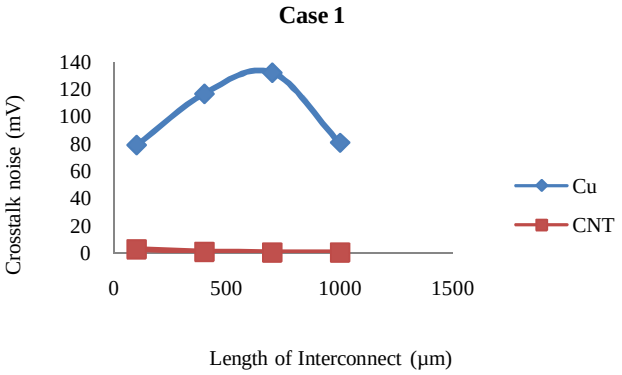

Fig. 8 Crosstalk noise voltage as a function of length for different interconnect

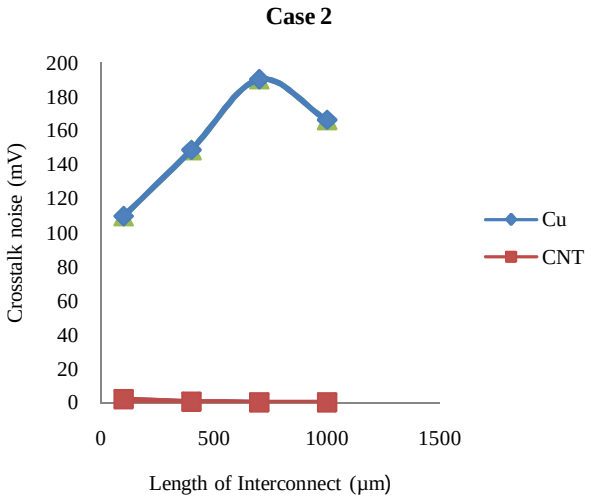

Fig. 9 Crosstalk noise voltage as a function of length for different interconnect

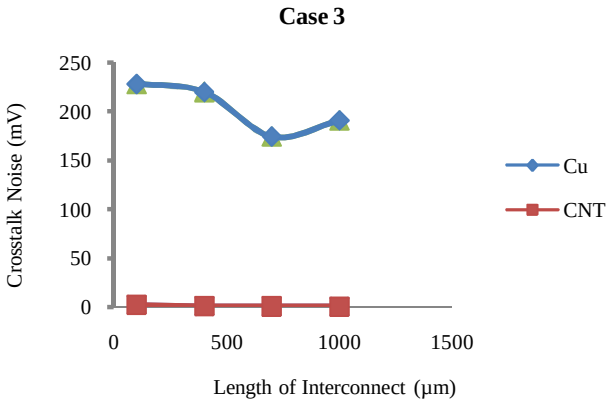

Fig. 10 Crosstalk noise voltage as a function of length for different interconnect

Fig. 8, 9 and 10 shows the comparison of crosstalk noise for copper and CNT bundle interconnect for L segment RLC. It reveals that crosstalk noise in the case of CNT bundle interconnect is much less than the copper interconnect which means that CNT bundle introduces less noise than copper interconnect and gives better performance.

V. CONCLUSION

The control of crosstalk induced noise voltage (functional crosstalk noise) in capacitively coupled interconnects of SWCNT bundle, at the far-end of victim line, for fixed pitch and varying interconnect dimensions under three different cases, for the proposed inter coupling capacitance model and the conventional model, at 22nm technology node, have been analyzed. It has been observed that the proposed model of coupling capacitance provides better reduction in crosstalk noise voltage compared to conventional counterpart in all three different cases. A similar analysis performed for copper interconnects showed that, compared to coupled interconnects of SWCNT bundle, copper interconnects has higher coupled noise voltage levels due to larger coupling capacitanceFurthermore, a comparative analysis of the effect of interconnect resistance, self inductance and ground capacitance of interconnect on positive coupled peaks at the far end of victim line in capacitively coupled interconnects of SWCNT bundle and copper has been studied. It is observed that, with increase in line resistance or ground capacitance, while the noise voltage peak reduces for both CNT and copper, there are more noise voltage peaks in the copper.

VI. FUTURE SCOPE

This work can continue in many different directions, Crosstalk and variation effects must be considered in designing the circuitry. New novel device and advanced circuit technologies enhance the performance while reducing power. The system's impact of these devices should be investigated. Resistivity of copper increases due to effect of electro migration and surface scattering in deep submicron technologies. To overcome these problems various alternative are used, but carbon nanotubes are found to be better alternative than copper interconnect. It is believed that CNT shall outperform copper interconnects in near future.

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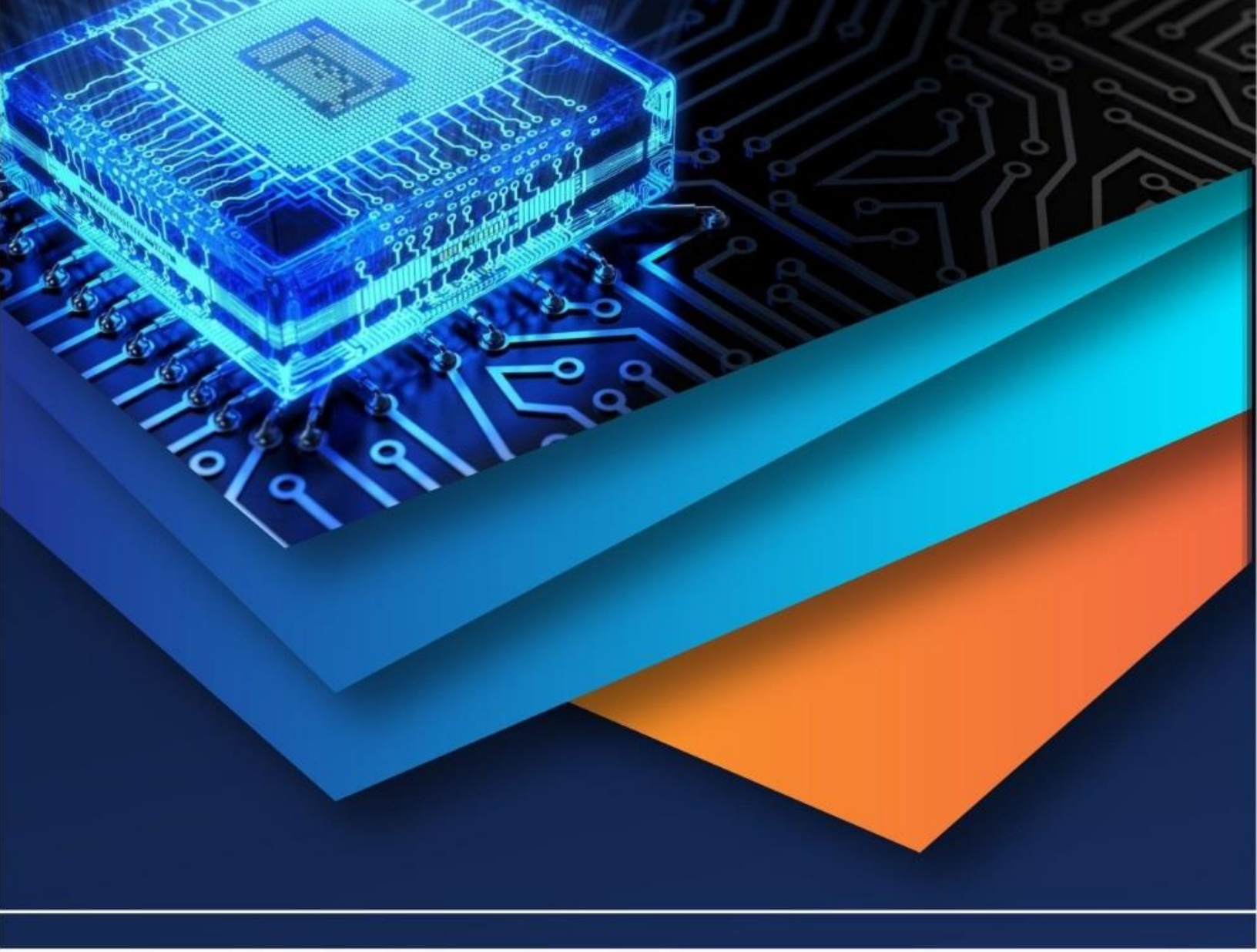

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