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Multi-Core Processors - Making the Move to Quad-Core and Beyond

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Abstract:** One constant in computing is that the world's hunger for faster performance isnever satisfied for which we have ever evolving processor which is what the best gift by digital electronics. Today these performance demands are not just for speed, but also for smaller, more powerfulmobile devices, longer battery life, quieter desktop PCs, and in the enterprisebetterprice/performance per watt and lower cooling costs. People want improvements inproductivity, security, multitasking (running multiple applications simultaneously onyour computer), data protection, game performance, many other capabilities and convenience being the last factor. Microprocessors are complex in many ways, not least in the complicated interrelationships between the chip, software, operating systems, development tools, available talent, and third-party support. Any one of these without the others is only a partial solution. All of them taken together provide a thriving ecosystem where innovation, engineering, and product design can flourish. But the ceaseless efforts by people in digital electronics have brought humanity in an era where multitasks are are efficiently carried out in a blink of eye. This paper deals with the description of basic operation and functions of three classes of hardware platforms, advantages, challenges of multi-core processing along with futuristic quad-core processors, increased processor performance, energy efficiency and capabilities. An attempt to combine the two best qualities of two processors has been made in this paper: Intel Core i7 processor's high-performance and the Intel Atom processor's low-power implementations.

***Keywords:** Multitasking, microprocessors, softwares, operating systems, hardwares, multi-core, quad-core.*

I. INTRODUCTION

Multi-core processors are the future of computing. As the and complexity of the data around us grows, multi-core processors has become increasingly important for helping run businesses, governments, our homes, and our entertainment. Multi-core processors are empowering the development of new usage models that enable wide-ranging advances in everything from medicine to IT, as wellas revolutionize the digital office, digital home, computing on the go, and computer gaming. The term architecture encompasses a combination of microprocessors and supporting hardware that creates the building blocks for a variety of computing systems. These devices are used in virtually every field of electronics, including automotive, industrial, automation, robotics, consumer electronics, image processing, networking, encryption, military, construction, medical, energy, and other industries.

From early 8-bit beginnings to 32-bit and 64-bit microprocessors that address a range of applications, performance requirements and power levels, processors have grown a lot and are still growing.

Some abbreviations used in the diagrams below:

BIOS : Basic Input/Output System; a boot ROM

DDR3 : Double Data-Rate v3; a popular DRAM interface standard

DMI : Direct Memory Interface; a video graphics standard

FIVR : Fully Integrated VoltageRegulator

LPC : Low Pin Count; a simple interface to slower I/O devices

PCH : Platform Controller Hub; a companion chip

PCI : Peripheral Component Interconnect; a popular expansion bus

PCIe : PCI Express; an upgraded PCI standard

SATA : Serial ATA; a popular disk-interface standard

SPI : Serial Peripheral Interface; simple interface to slower devices

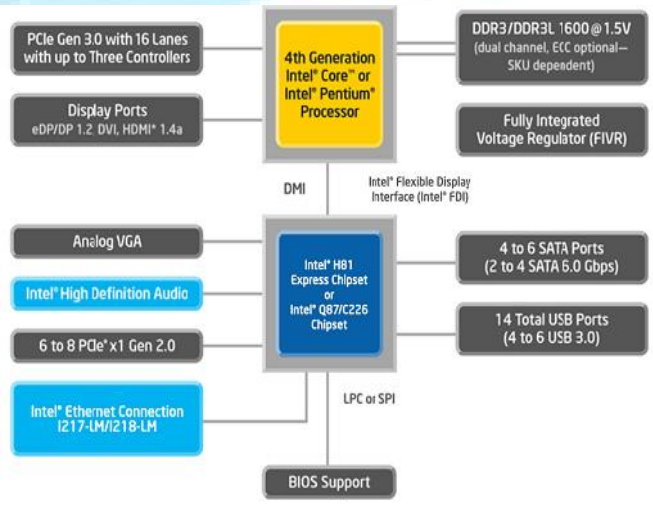


Fig.1 Typical system based on the Intel Core i7 processor.

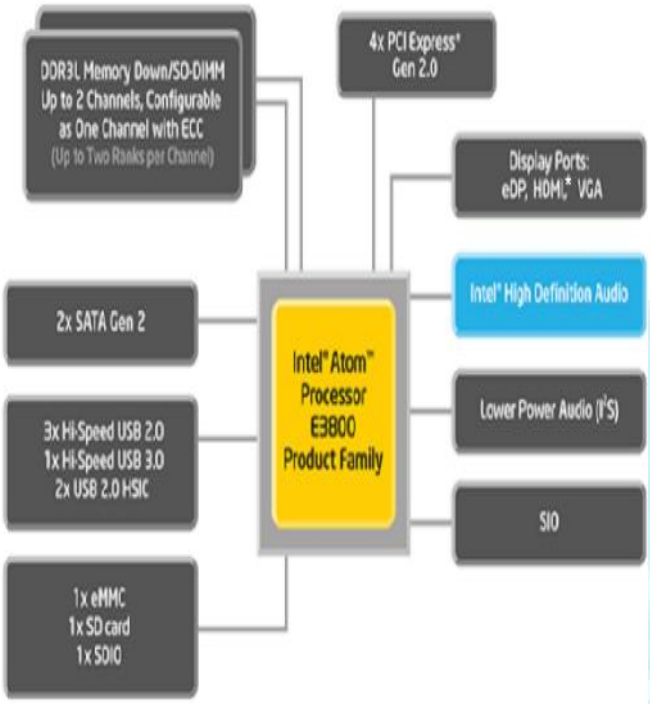


Fig.2 Typical system with Intel Atom processor (SoC).

II. BASICS OF PROCESSOR ARCHITECTURE

The hardware requirements for each application will be different, of course, but some basics apply to all. The processor chip itself is just the beginning. With few exceptions, the processor does not stand alone, but works in concert with compatible support chips. Different processors work with different support chips, and this paper outlines two representative examples. The first example describes a typical hardware platform based on the high-performance Intel Core i7 processor combined with similarly high-performance support logic (see Figure 1). The second example focuses on a small, low-cost Intel Atom processor–based system (see Figure 2). Generally speaking, every hardware platform will include two major components: the microprocessor chip, and a companion chip known as the platform controller hub (PCH). In earlier times, processors were paired with two companion chips, often called the "north bridge" and the "south bridge," or the MCH and the ICH. Nowadays, the functions of the north bridge are usually included in the processor itself, while the south bridge has been replaced by the much more capable PCH. In single-chip (SoC) configurations, there is no PCH; its functions are included in the processor itself. Surrounding these two components (i.e., processor and PCH) will be other components including DRAM, a boot ROM, a power supply, and the peripheral interfaces appropriate for the system, such as a network or sensor connection. Most systems will also include some nonvolatile memory (e.g. flash or E2PROM), and perhaps some "glue logic" that is specific to the application.

As these diagrams show, one of the example systems is based on a two-chip set (processor and PCH), while the second example uses only a single chip (the processor) with integrated controllers. The former is designed for higher performance and more expansion capability, while latter is optimized for small size and low cost. These examples highlight just two of the many options available to designers of Intel architecture systems.

A. Intel Core i7 Processor–Based System:The example in Figure 1 illustrates a high-performance system based on the quad-core Intel Core i7 processor, the Intel® Q87 chipset (Intel® DH82Q87 PCH), two banks of external DDR3 DRAM, and several peripheral devices and interfaces. This configuration represents a high-end system with maximum performance with maximum capability and expandability.

B. The Intel® Core™ i7 Processor: The heart of this system design is the Intel® Core™ i7-4770S processor, a high-end 64-bit implementation of the Intel architecture. The particular 4th generation, or "Haswell," Intel Core i7 processor shown in the diagram has several notable features, including:

- Four independent CPU cores
- Two-way multithreading per CPU core
- A built-in two-channel DDR3 DRAM controller
- Integrated L1, L2, and L3 caches
- Direct Media Interface (DMI) connection between the processor and the PCH

The Intel Core i7 processor achieves its high performance through its multiple CPU cores and its Simultaneous Multithreading (SMT) feature. Between the four cores (in this example) and the two-way multithreading per core, the Intel Core i7 processor appears to software as eight independent 64-bit CPUs. Figure 3 shows a representation of the silicon die for Intel Core i7 processor, with its four independent CPU cores and other features highlighted. Figure 4 shows a conceptual diagram of the same processor, illustrating how the four CPUs each has its own L1 and L2 caches, and the shared L3 cache.

The processor's on-chip DRAM controller is responsible for cache coherence. If data at the address requested is not in one of the processor's caches, or if the data in external memory is newer than the cached copy, the memory controller is told to retrieve the data at the requested address. Data transfers between the processor and memory are always 64 bits wide, the full width of the L2 cache on the processor. If only a byte of data is requested, the full 64 bits are retrieved but the processor may use only 8 of those bits. The memory controller is configurable via the BIOS to support multiple speeds and/or sizes of memory. DRAM refresh is also handled by the memory controller, after it's initially configured. The specific type, size, and speed of memory supported varies by processor.

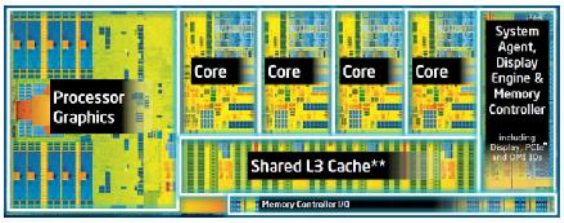


Fig.3 Intel Core i7 processor internal die photograph.

The PCI Express (PCIe) interface is the highest bandwidth I/O interface in the Intel architecture system. The number of PCIe lanes can vary depending on the processor used, but will usually be in multiples of four.

III. DIRECT MEDIA INTERFACE (DMI)

DMI is the name given to the link between the Intel Core i7 processor and its companion chip, the Intel Q87 chipset (Intel DH82Q87 PCH). The same DMI interface is used by several different processor and PCH implementations, including the Intel Core i7-4770S, Intel Core i5-4570S, Intel Core i3-4330 processors, Intel Pentium processor G3420, Intel Q87 chipset, Intel H81 Express chipset, and Intel C226 chipset.

IV. PLATFORM CONTROLLER HUB (PCH)

The Platform Controller Hub (PCH) chip is a highly integrated device intended to prove all the high-value features and interfaces required for a midrange to high-end system. Depending on the particular model of PCH chip, it may provide a controller for multiple banks of DRAM, a controller for multiple graphics displays (an accelerator for which may be present on the processor itself), several USB interfaces, SATA controller for disk drives and other storage media, an Ethernet LAN port, High Definition Audio , and more.

A. Modern I/O Interfaces:

The PCH acts a bridge or controller for a variety of industry-standard interfaces allowing the system designer to choose from a wide range of peripherals, including:

• PCIinterface operates at 33 MHz and allows for a number of external bus masters. The PCH acts as the central arbiter and root of the PCI bus.

• PCI Expressroot port controllers. The number of ports varies with the specific PCH component but is generally in the range of 1 to 4. Link widths of ×1 ×4 are support at speeds of 2.5 GT/sec.

• Serial ATA (SATA)controllers supporting both legacy operation using I/O space and the Advanced Host Controller Interface (AHCI) using memory-mapped I/O, as well as allowing advanced features such has hot-plug and native command queuing. SATA II supports data rates of 1.5 Gb/sec and 3 Gb/sec.

• Integrated Drive Electronics (IDE) controllers are also used to control hard disc drives and CD/DVD drives. They have been replaced in some platforms by the newer SATA interface since SATA offers better performance over a smaller interface.

• Universal Serial Bus (USB)supporting High Speed USB 2.0 (480 Mb/sec) operation as well as full-speed (12 Mb/sec) and low-speed signaling.

• General Purpose I/O (GPIO)pins for system customization. Many pins can also be configured to cause interrupts or wake events.

• System Management Bus (SMBus 2 .0)The SMBus Host interface allows the processor to communicate with SMBus slaves. This interface is also compatible with most I2C devices. Slave functionality, including the Host Notify protocol is implemented.

• Serial Peripheral Interface (SPI)is used to interface to BIOS flash devices that contain boot firmware and initialization code. Up to two SPI flash devices operating at 33 MHz can be connected. Note that the flash devices connected to the LPC interface are quickly becoming obsolete and SPI is expected to be standard interface for BIOS flash in the future. The PCH is always a master on the SPI interface.

• Low Pin Count Interface (LPC)This interface replaces the ISA bus originally developed by IBM in the early 1980s, but uses only 7 signals plus a clock. It can be used to connect to a variety low speed devices that don't require the bandwidth of PCI or PCI Express. This interface is typically used to interface with Super I/O devices which contain many interfaces such as floppy driver controller, PS2 keyboard/mouse controls and serial ports.

• JTAG Boundary Scanallows testing of PCB board after assembly.Support PeripheralsThe PCH integrates numerous support peripherals that replace many external components.

• Real Time Clock (RTC): The RTC is compatible with the popular MC146818A. It contains 256 bytes of RAM that can be maintained with a 3V battery. Of that space, 242 bytes are available for programmer use, while the remaining are dedicated to the clock function. The RTC can generate wake events up to 30 days in the future. An external 32.768-KHz crystal is required for operation.

• High Precision Event Timers These are high-resolution timers that can be used to generate periodic or one-shot interrupts. There are eight comparators, which share a common counter that is clocked from a 14.31818-MHz source.

• Advanced Programmable Interrupt Controller (APIC)is a more modern interrupt controller than the earlier 82C59 (see below). It supports multiprocessor/multicore interrupt management by allowing interrupts to be directed to a specific processor. The I/O APIC in the PCH can support up to 24 interrupt vectors and works in conjunction with I/O APICs in other devices to help eliminate the need for share interrupts among multiple devices.Compatibility PeripheralsThe PCH

contains peripherals compatible with those dating back to the earliest IBM PCs with an ISA bus. Modern systems replace the ISA bus with the Low Pin-Count (LPC) bus, but the peripherals that were once discrete components are now integrated into the PCH. One key strength of Intel architecture is its combination of backward compatibility and continuing innovation.The PCH contains two 82C37 DMA controllers, two ISA-compatible 82C59 interrupt controllers, and three 82C54 programmable interval timer equivalents.

B. Introduction to Intel Atom:

Intel Atom processor is a fairly recent addition to the family of 32-bit processors. It is intended for embedded systems where small size, modest power consumption, and low cost are important.The 82C37 DMA controllers should not be confused with the DMA engines found in some earlier MCH (Memory ControllerHub) components. These DMA controllers are tied to the ISA/LPC bus and used mostly for transfers to/from slow devices such as floppy disk controllers.The ISA-compatible 82C59 interrupt controllers have been largely supplanted by the Advanced Programmable Interrupt Controller (APIC, see above) since the letter offers support for more than 15 interrupt sources and supports multicore/multiprocessor systems. However, the 82C59 controllers are still used by some older operating systems that run only on single-processor (single CPU) systems.The BIOSLike any computer, an Intel architecture system requires a boot ROM to bootstrap the processor and, optionally, load an operating system and configure components. In an Intel architecture system, this boot ROM has typically been known as the BIOS: the basic input/output system.

The BIOS controls the activity of the Intel architecture hardware until the operating system takes over. One job of the BIOS is to configure registers and components and set up the devices to the particulars of the system hardware into which the Intel architecture is designed. In a typical PC design, some of the hardware is dedicated by the design based on the motherboard design, but other hardware aspects vary based on what the end user may plug into the motherboard. As the BIOS executes, after the initial configuration is done, it will determine the type and amount of memory, then it goes through a discovery phase. Once all the devices and hardware are configured the BIOS will turn over control of the system to an operating system. Many Intel architecture platforms come with the necessary boot firmware already installed. To create a boot ROM for a custom or updated system, Boot Loader Development Kit (Intel BLDK), which can be used to create a UEFI-compliant (Unified Extensible Firmware interface) boot loader compatible with many operating systems.

Intel Atom Processor–Based System Compared to the Intel Core i7 processor–based system described above, an Intel Atom processor based system is almost trivially simple. This example is based on an Intel Atom processor E3800 product family, which has all the necessary controllers and peripherals already integrated into it, doing away with the need for a companion chip. Refer back to Figure 2 for an overview of this system configuration. The Intel Atom ProcessorIntel Atom processor is a fairly recent addition to the Intel architecture family of 32-bit processors. It is intended for embedded systems where small size, modest power consumption, and low cost are important. For that reason, Atom processor includes its own on-chip DRAM controller, PCI Express interface, optional display controller, USB controllers, real-time clock, timers, interfaces to system-management functions. The overall system thus enjoys small size with high integration.

With no DMI (nor any need for one), Atom processor uses PCI Express as its primary means of expansion. PCIe has sufficient bandwidth for extensive expansion capability, and its standardized interface is compatible with many devices from multiple vendors. Like the Intel Core i7 processor, Intel Atom processor E3800 has its own on-chip DRAM controller, able to handle two channels of DDR3 DRAM. One channel can optionally support ECC (error correction), further enhancing system reliability.

C. A Fundamental Theorem of Multi-Core Processors (Advantages):

Multi-core processors take advantage of a fundamental relationship between power and frequency. By incorporatingmultiple cores, each core is able to run at a lower frequency,dividing among them the power normally given to a singlecore. The result is a big performance increase over a singlecore processor. The following illustration—based on our labexperiments with commonly used workloads—illustrates this key advantage.

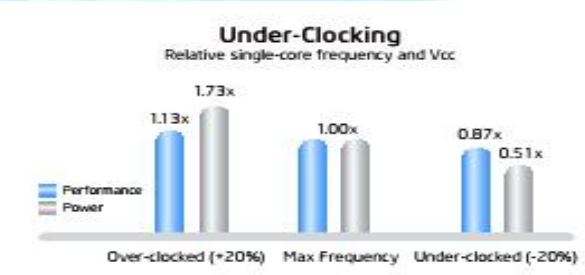


Figure 1. Increasing clock frequency by 20 percent to a single core delivers a 13 percent performance gain, but requires 73 percent greater power. Conversely, decreasing clock frequency by 20 percent reduces power usage by 49 percent, but results in just a 13 percent performance loss.

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This fundamental relationship between power and frequencycan be effectively used to multiply the number of cores fromtwo to four, and then eightand more, to deliver continuousincreases in performance without increasing power usage.

A. Cache Utilization:

Cache is multi-core optimization that improves performance and efficiency by increasing the probability that each core of a multi-core processor can access data from a higher performance, more-efficient cache subsystem. Cache works

by sharing the Level2 (L2) cache among cores so that data is stored in one place that each core can access. Sharing L2 cache enables each core to dynamically use up to 100 percent of available L2 cache, thus optimizing cache resources.

B. Quad-Cored:

This quad-core desktop processor will be the ultimate gaming machine and multimedia processing engine for today's growing list of threaded applications. In additionto being excellent for intensive multitasking, the Intel Core 2 Extremequad-core processor will provide impressive gaming performance,offering plenty of headroom for tomorrow's thread-intensive games. Gamers can expect a smoother, more exciting gaming experience through the distribution of artificial intelligence (AI),physics and rendering across four hardware threads. Ideal forprocessor-intensive, highly threaded applications, the Intel Core2 Extreme quad-core processor will be the top choice for multimedia enthusiasts, gamers, and workers in demanding multitasking environments. It will feature 2.66 GHz core speed and 1066 MHz front side bus speed.

C. Beyond Quad-Core: Tera-Scale Computing:

Spurred by increasing globalization, growing device intelligence,and the explosion of digital data, next decade's applications will be much more computationally intensive thananything we've seen to date. This will be the "tera era"—an age when people need teraflops (a trillion floating point operations persecond) of computing power, terabits (a trillion bits per second of communications bandwidth), and terabytes (1,024 gigabytes) of data storage to handle the information all around them.

D. Transitioning the Industry to Multi-Core Processing (Benefits):

One immediate benefit of multi-core processors is how they improve an operating system's ability to multitask applications. For instance, say you have a virus scan running in the background while you're working on your word-processing application. This often degrades responsiveness so much that when you strike a key, there can be a delay before the letter actually appears on the screen. On multi-core processors, the operating system can schedule the tasks in different cores so that each task runs at full performance.

Another major multi-core benefit comes from individual applications optimized for multi-core processors. These applications, when properly programmed, can split a task into multiple smaller tasks and run themin separate threads. For instance, a word processor can have "find and replace" run as a separate thread so doing a "find and replace" on a big document doesn't have to keep you from continuing to write or edit. In a game, a graphics algorithm needing extensive processing power could be one thread, rendering the next scene on the fly, while another thread responds to your commands for a character's movements.

The critical element in multi-core computing is the software. The throughput, energy efficiency, and multitasking performance of multi-core processors will all be more fully realized when application code is threaded and multi-core ready.

There are several vendors that provide us with multicore processors such as Intel, AMD, VIA etc.

Let's see where does the next decade take us to! From multi-processors to virtul processors and so on many more.

V. CONCLUSIONS

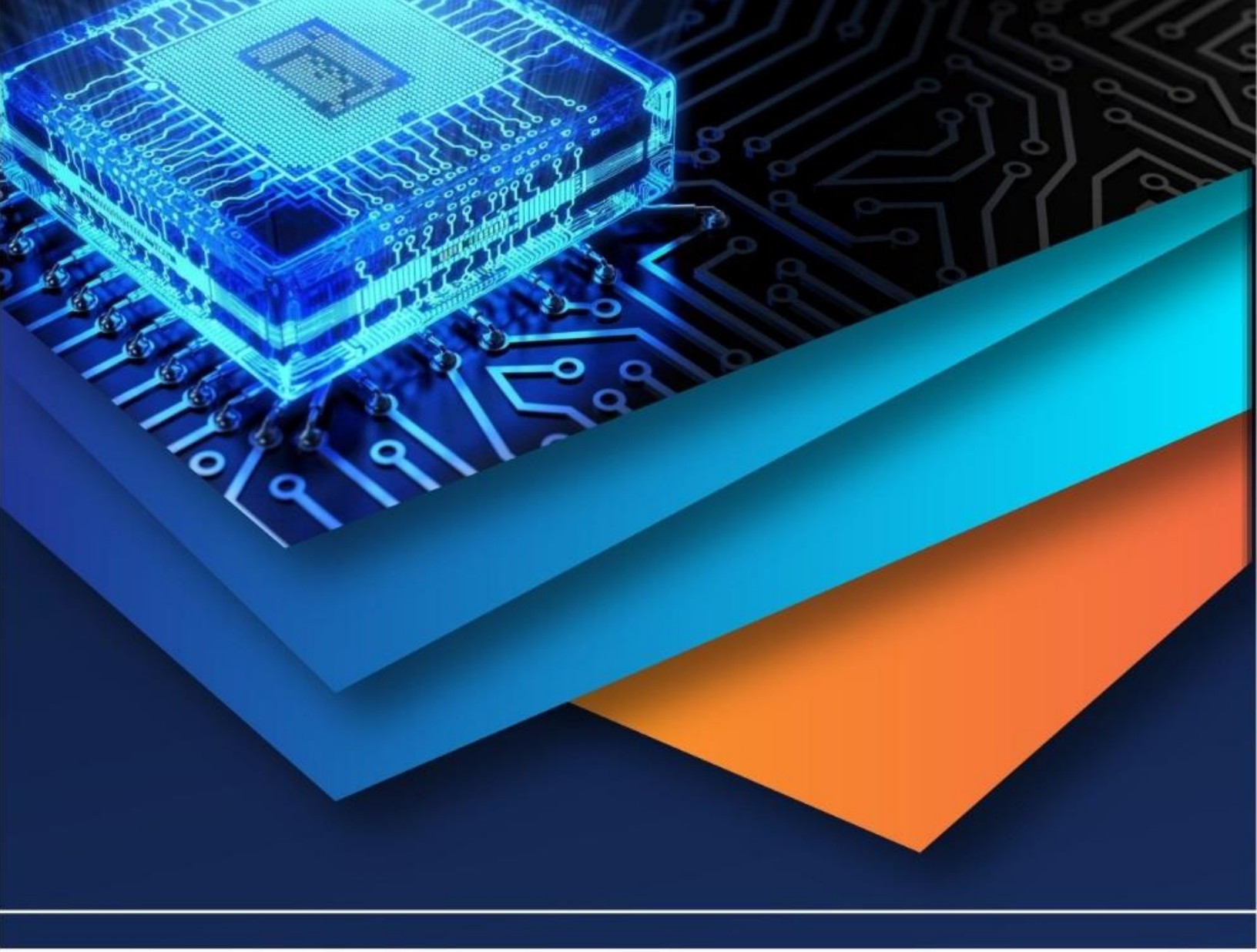
Multi-core processors are the future of computing. As the wealth and complexity of the data around us grows, multi-core processors will become increasingly important for helping run businesses, governments, our homes, and our entertainment. Multi-core processors will empower the development of new usage models that will enable wide-ranging advances in everything from medicine to IT, as well as revolutionize the digital office, digital home, computing on the go, and computer gaming. Think of a time a decade or so from now when the full power of high performance computing and parallel processing is available to computer users everywhere and it might be possible to hold the power of a computer with hundreds of execution cores in the palm of your hand. Chances are, we'll look back and wonder how people ever managed with computers having just a single execution core in their processor. Intel® quad-core processors are the next step in this process.

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