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A Simplified Spam Algorithm for Three Level Diode Clamped Inverter

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Abstract: ***To solve the problem of computational complexity in The Multi-Level Inverter (MLI) SVPWM algorithm due to large number of switching vectors and redundant switching sequence. In this paper Simplified SVPWM algorithm has been implemented based on geometrical symmetry of six sectors, as well as relationships between on time calculations and on time allocation for the switches. The advantages of above proposed algorithm, is to reduce computations of the three-level SVPWM in one sector. Consequently in this paper the simplified algorithm compared with the conventional algorithm. The proposed algorithm is verified through MATLAB simulation and compared the performance of three-level SVPWM algorithms against the Total Harmonic Distortion (THD).***

Keywords: Multi-level inverter, Pulse Width Modulation (PWM), Space Vector Pulse Width Modulation (SVPWM), Sine Pulse Width Modulation (SPWM) and Total Harmonic Distortion (THD).

I. INTRODUCTION

An inverter converts DC voltage source to AC output voltage. The two level inverter produces a square wave output voltage with high harmonic. To minimize the THD with improved fundamental voltage, the multi-level inverter concept has been implemented. The neutral-point clamped (NPC) three-level topologies are recently showing great popularity in MLIs[1]-[2]. An advantage of this multilevel inverter includes good power quality by increasing waveform steps and reduces the voltage stress across switches. Low voltage stress results in the low dv/dt, which causes less EMI problems.

There are several PWM techniques to control the inverter, where SPWM techniques are commonly used [8]. In three-level SVPWM technique has an advantage over SPWM technique such as, it gives us 15% higher DC-BUS Utilization and very well used for digital implementation [1]-[5].

Conventional three-level SVPWM is complex than two-level SVPWM because of more number of switching vectors and on time calculations of the switches[1]-[4].

II. THREE LEVEL SVPWM DIODE CLAMPED INVERTER

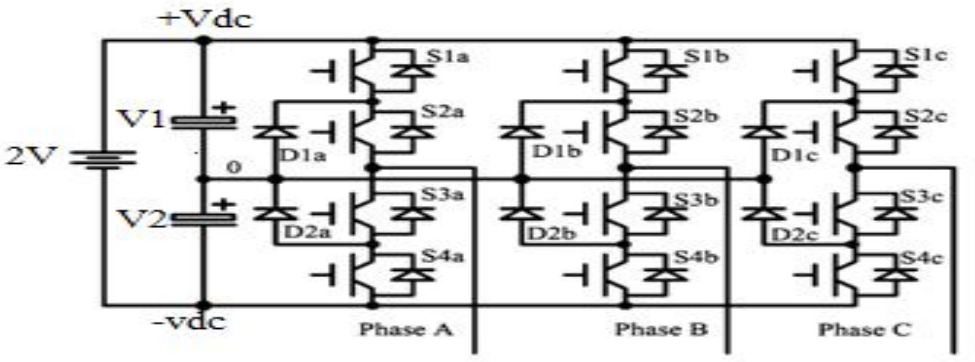


Fig. 1Three level Diode clamped voltage source inverter

Circuit shown of the three-level converter. Now a days, three-level neutral clamped voltage source inverters (3LVSIs) are mostly used for dc–ac power conversion. One of the advantages is the improved output waveform quality or reduction in total harmonic distortion (THD) in the line voltage. With devices of the same voltage rating, a 3LVSI can handle a dc bus voltage twice that of a 2LVSI. Hence, this topology is popular in medium-voltage applications [1]-[5]. It also provides better performance in terms of semiconductor losses than a two-level converter in low-voltage applications with medium to high switching frequencies.

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III. THREE LEVEL SPACE VECTOR PULSE WIDTH MODULATION

It is a naturally accepted view that three-level SVPWM is an extension of the conventional two-level SVPWM.

A. Basic Principle of Operation

Each phase leg of inverter composed of four switches, has three kinds of switching states, which can be represented by P, O, N listed Table I.

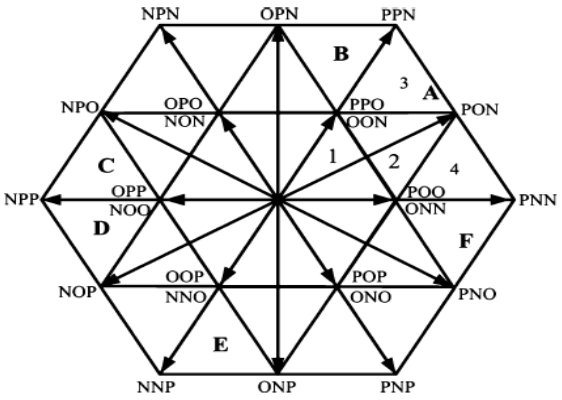
TABLE I
SWITCHING STATES AND THEIR REPRESENTATION

Symbol	S_{1x}	S_{2x}	S_{3x}	S_{4x}	Voltage
P	ON	ON	OFF	OFF	+V
O	OFF	ON	ON	OFF	0
N	OFF	OFF	ON	ON	-V

So 27 switching states exist in three-phase three-level converter, each of which can be represented in vector form using following expression

$$V_{ref} = \frac{2}{3}(V_a + V_b * e^{j\frac{2}{3}\Pi} + V_c * e^{-j\frac{2}{3}\Pi}) \quad (1)$$

Space-vector diagram of a three level converter, shown as Fig. 2.



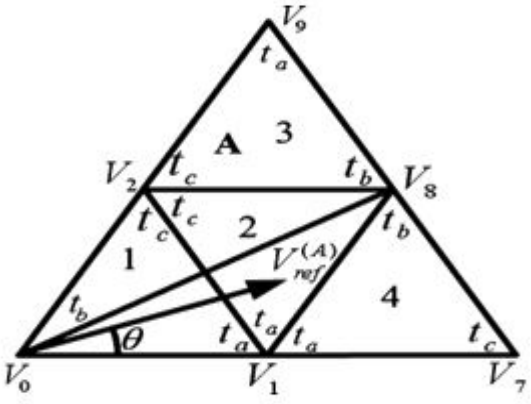


Fig. 2 Three level SVPWMFig.3 Vector combination in sector A.

After calculated Vα, Vβ, Vref and angle, the first step is taken. The next step is to calculate the duration ON time for each vector [7].

By using sector A as an example, the calculation flow of the three-level SVPWM algorithm can be clearly demonstrated.

Considering the reference voltage vector V_{ref}^{A} staying in the region2 [1]-[6], it can be composed by voltage vectors v_1, v_2 and v_8 as shown in Fig.3. During a switchingperiod (T_s), the average output voltage combined by three consecutive voltage vectors should match with the reference voltage. Therefore, the (volt-sec) balance equation is given by

$$V_{ref}^{A} T_s = V_1 T_a + V_8 T_b + V_2 T_c \quad (2)$$

$$T_s = T_a + T_b + T_c \quad (3)$$

The on time of voltage vectors can be calculated as follows:

$$T_a = T_s - 2k\sin(\theta) \quad (4)$$

$$T_a = 2k\sin\left(\frac{\Pi}{3} + \theta\right) - T_s \quad (5)$$

$$T_c = T_s - 2k\sin\left(\frac{\Pi}{3} - \theta\right) \quad (6)$$

Where k= $(\frac{\sqrt[4]{3}}{3})(\frac{V_{ref}}{V_{dc}})T_s$

Using the same procedure, the dwelling time in other regions in sector A can be obtained as shown in Table II.

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TABLE III
ON TIMES IN SECTOR A

On time& Region	T_a	T_b	T_c
1	$2k\sin\left(\frac{\Pi}{3}-\theta\right)$	$T_s_2k\sin\left(\frac{\Pi}{3}+\theta\right)$	$2k\sin(\theta)$
2	$T_s-2k\sin(\theta)$	$2k\sin\left(\frac{\Pi}{3}+\theta\right)-T_s$	$T_s_2k\sin\left(\frac{\Pi}{3}-\theta\right)$
3	$2k\sin(\theta)-T_s$	$2k\sin\left(\frac{\Pi}{3}-\theta\right)$	$2T_s_2k\sin\left(\frac{\Pi}{3}+\theta\right)$
4	$2T_s_2k\sin\left(\frac{\Pi}{3}+\theta\right)$	$2k\sin(\theta)$	$2k\sin\left(\frac{\Pi}{3}-\theta\right)-T_s$

B. Three level SVPWM Switching Sequence Arrangement

The converter has some redundant switching states, so there are several options to determine the switching sequence. Switching sequence can be arranged according to certain optimal objective. In this paper, in order to achieve low THD, all relevant switching states are arranged to form the switching sequence [1].

The switching sequences in the regions of sector A are arranged as follows:

Region 1: PPO-POO-OOO-OON-ONN and return

Region 2: PPO-POO-PON-OON-ONN and return

Region 3: PPO-PPN-PON-OON and return

Region 4: POO-PON-PNN-ONN and return

C. Three Level SVPWM Symmetrical PWM Generating

As indicated in the name of the topology, each phase has three voltage levels, which require two PWM generators to produce [1]-[6].

Wave form can be decomposed into two two-level waveforms, which can be produced easily using two PWM generators as shown in Fig.4.

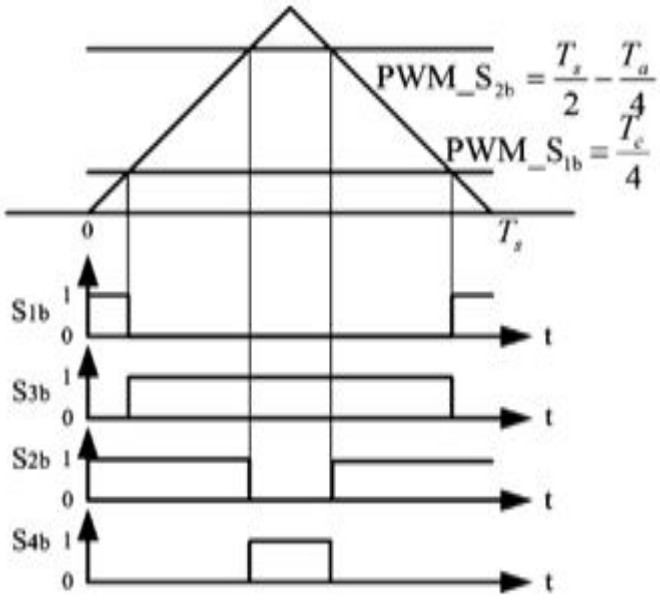


Fig.4 Firing Time Settings for Four Switches Using Two PWM Pulses in Phase B.

According to switching sequences arranged in symmetrical pattern, the PWM firing time setting for each switch in sector A can be achieved as given in Table III.

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TABLE IIIII
PWM FIRING TIME FOR EACH SWITCH OF UPPER ARMS IN SECTOR A

Region& Time	1	2	3	4
PWM_S1a	$\frac{T_c}{4}+\frac{T_a}{4}$	$\frac{T_c}{4}+\frac{T_a}{4}+\frac{T_b}{2}$	$\frac{T_s}{4}-\frac{T_c}{4}$	$\frac{T_s}{2}-\frac{T_a}{4}$
PWM_S2a	$\frac{T_s}{2}$	$\frac{T_s}{2}$	$\frac{T_s}{2}$	$\frac{T_s}{2}$
PWM_S1b	$\frac{T_c}{4}$	$\frac{T_c}{4}$	$\frac{T_c}{4}+\frac{T_a}{2}$	0
PWM_S2b	$\frac{T_s}{2}-\frac{T_a}{4}$	$\frac{T_s}{2}-\frac{T_a}{4}$	$\frac{T_s}{2}$	$\frac{T_a}{4}+\frac{T_b}{2}$
PWM_S1c	0	0	0	0
PWM_S2C	$\frac{T_s}{2}+\frac{T_a}{4}-\frac{T_c}{4}$	$\frac{T_c}{4}+\frac{T_a}{4}$	$\frac{T_c}{4}$	$\frac{T_a}{4}$

IV. THREE LEVEL SIMPLIFIED SVPWM ALGORITHM

The main idea for simplified algorithm comes from the fact that the shape of 6 sectors is identically same as seen from Fig. 2. So there should exist some close relationships in on time calculations and arrangement for switches in each phase between them. We can calculate the on times for switches in certain sector and then map the on times in other specific sectors corresponding on time through the relationships between them. The following is the explanation of the relationships between them

A. The Relationship of On Times between sectors

Suppose reference vector V_{ref}^{A} stays in region 2 of sector A, while reference vector V_{ref}^{B} in sector B is obtained by rotating V_{ref}^{A} vector counter clock wise by 60^0 degree as demonstrated in Fig. 5.

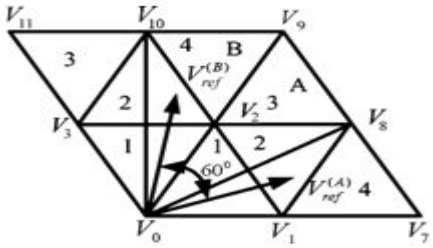


Fig. 5 Two Vectors with 60◦Shifting in the Sector A and B.

Therefore, vector V_{ref}^{A} and vector V_{ref}^{B} with the same length lie in the region 2 of sector A and B respectively. As explained in the Section II, the reference vector V_{ref}^{A} can be composed of by vector V1, V2 andV8. Whose on times can be calculated using expression (2). While the reference vector V_{ref}^{B} can be composed by vector V2, V10 and V3, whose on times can also be given as

$$V_{ref}^{(B)}T_s = V_2T_a + V_{10}T_b + V_3T_c \qquad (7)$$

$$T_a + T_b + T_c = T_s \qquad (8)$$

The expression can be transformed V_{ref}^{A} by multiplying the rotating factor $e^{-j\frac{\Pi}{3}}$ as illustrated as follows:

$$V_{ref}^{(B)}T_s = V_2T_a + V_{10}T_b + V_3T_c \xrightarrow{e^{-j\frac{\Pi}{3}}} V_{ref}^{(A)}T_s = V_1T_a + V_8T_b + V_2T_c \qquad (9)$$

It is clearly shown that the on times of the corresponding voltage vectors are totally same. This relationship in other regions of any other sectors is also validated. Therefore, when the reference vector in other sectors is rotated to sector A by $n\pi/3$ (n=1, 2, 3, 4, 5), the on times calculated out in sector A equal to those in other sectors.

B. Relationship of Switching Sequences Between Sectors

If the relationship between the switching sequences in sector A and those in other sectors can be found out, the switching sequences can be arranged in sector A and then mapped to the other sectors through the corresponding relationship. By this means, all the

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calculation procedures can be carried out in sector A, which will definitely reduce computation resources in hardware implementation.

Considering that the reference vector V_{ref}^{A} is expressed as a combination of phase voltageV_a, $V_b$and V_c in vector form as:

$$V_{ref}^{A} = \frac{2}{3}(V_a + V_b * e^{j\frac{2}{3}\Pi} + V_c * e^{-j\frac{2}{3}\Pi}) \qquad (23)$$

So the reference vector V_{ref}^{B}can be expressed in the following form

$$V_{ref}^{B} = V_{ref}^{A} * e^{j\frac{1}{3}\Pi} = \left(-V_b - V_c * e^{j\frac{2}{3}\Pi} - V_a * e^{-j\frac{2}{3}\Pi}\right) \quad (24)$$

Indicates that vector V_{ref}^{B} also can be combination of Phase voltageV_a, $V_b$and V_c by shifting and reversing phase voltages [1]-[2]-[4]. Using the same way, the corresponding reference vector in other sectors can be constructed as given in Table IV.

TABLE IV
RELATIONSHIPS OF PHASE VOLTAGES CONSTRUCTING THE REFERENCE VECTORS IN SIX SECTORS

Sector	Phase voltage A	Phase voltage B	Phase voltage C
A	V_a	V_b	V_c
B	$-V_b$	$-V_c$	$-V_a$
C	V_c	V_a	
D	–	–	–
E			
F	–	–	–

Phase voltage shifting is easy to be accomplished by exchanging the PWM signals between two corresponding phases. While phase voltage reversing can be achieved by mirroring the PWM signals of switches of upper arm with those of lower arm as illustrated in table V.

Suppose the switching state is P, which means the switches s1 and s2 are on and switches s3 and s4 are off. By mirroring the PWM signals, the switches s1 and s2 are off and switches s3 and s4 are on, in doing so, the phase voltage reversing can be obtained. The relationship of on times of s1 and s2 before and after mirroring can be easily deduced as given in Table V.

TABLE V
RELATIONSHIP OF ON TIMES OF S1 AND S2 BEFORE AND AFTER MIRRORING

Phase voltage	S1 On time	S2 On time
V	PWM_S1b	PWM_S2b
-V	$/2$ −PWM_S2b	$/2$ −PWM_S2b

Through the simplified algorithm, the calculation flow forsix sectors can be mapped into sector A, as demonstrated [1]-[5] in Fig. 6.

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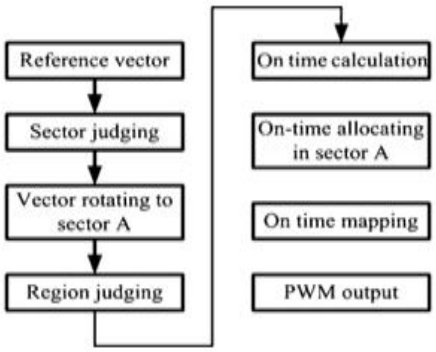


Fig. 6 Simplified Calculation Flow Chart for the Three-Level SVPWM

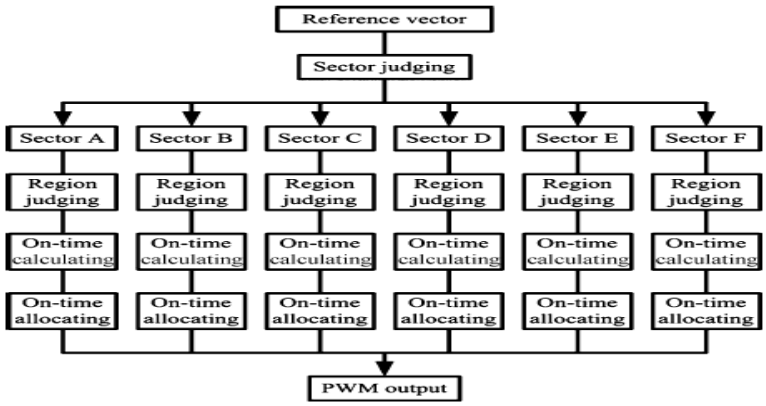
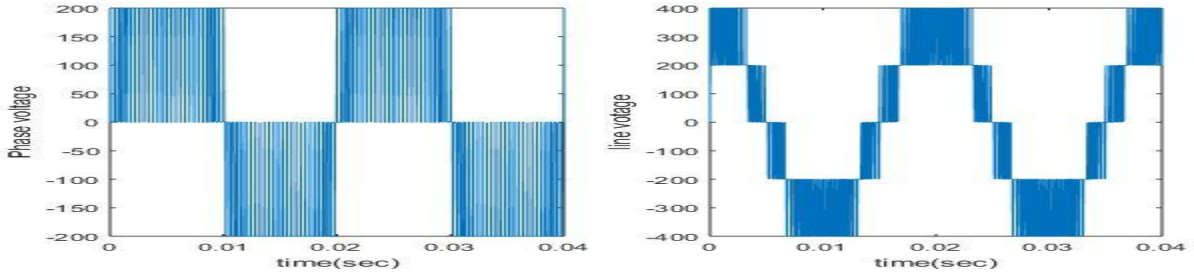


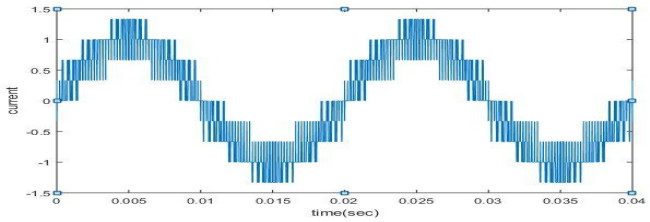
Fig. 7 conventional calculation flow

Compared with the conventional calculation flow as shown in fig.7, the simplified calculation flow can significantly reduce calculation complexity.

V. MATLAB SIMULATION/OUTPUT WAVE FORMS AND THD ANALYSIS

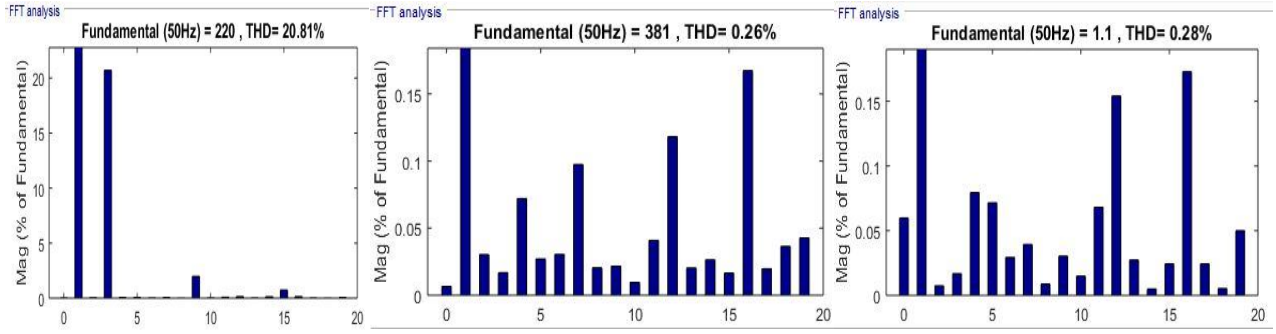


(a) (b)



(c)

Fig.7Three-Level SVPWM (a).Phase Voltage, (b).Line Voltage and(c). Phase Current.



(a) (b) (c)

Fig.8. THDAnalysis of Three-Level SVPWM (a) Phase Voltage,(b) Line voltage and (c)Phase Current.

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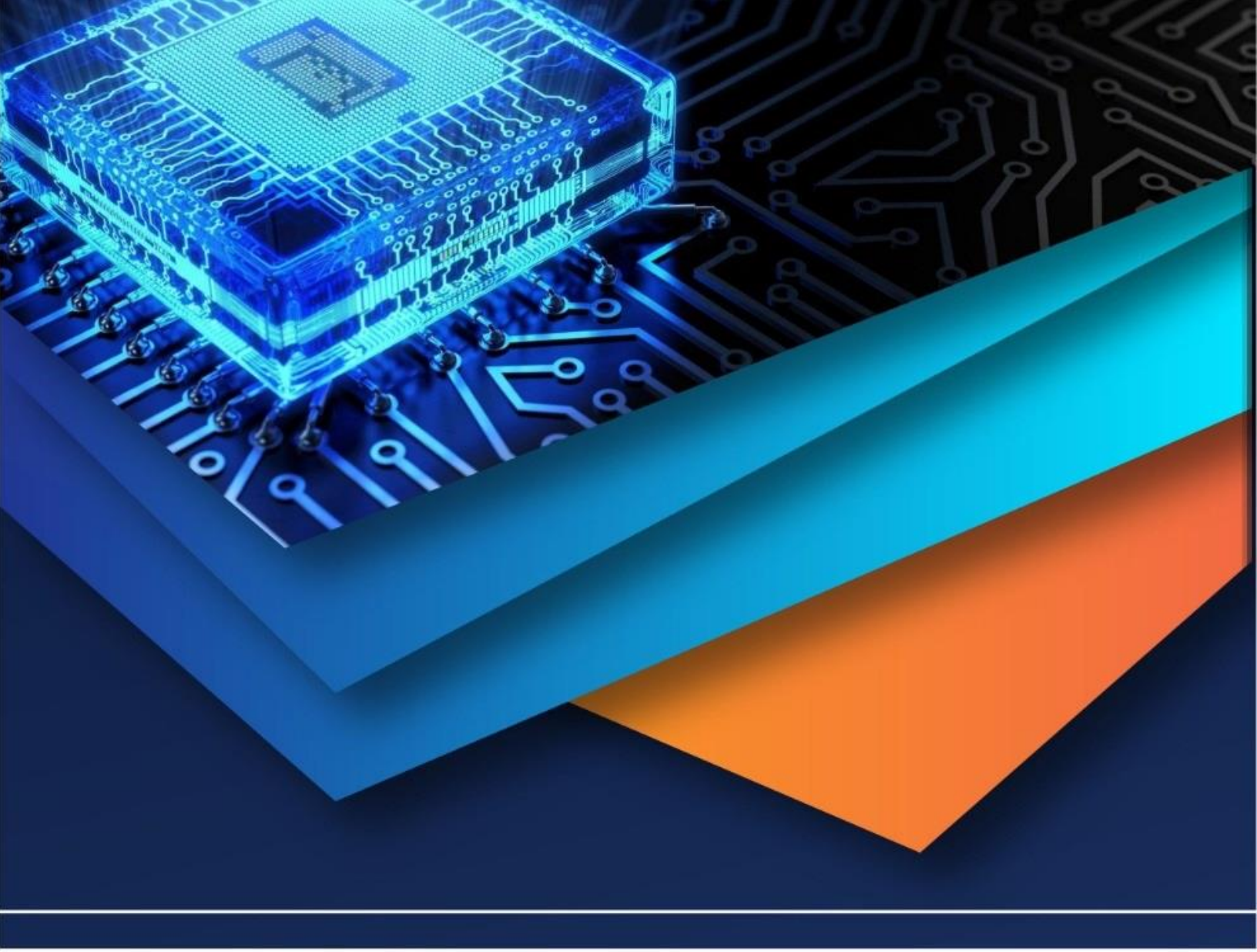
VI. CONCLUSION

This paper presents a simplified space vector PWM algorithm. The proposed algorithm significantly reduces and simplifies the calculation of space vectors and their corresponding dwell times. This simplified algorithm is implemented to three level diode clamped multilevel inverter. This simplified algorithmfeatures easy implementation and more importantly minimum harmonic content in the inverter output voltage. These algorithms are verified through computer simulations and results are validated.

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