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Review and Analysis of Glitch Reduction for Low Power VLSI Circuits

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***Abstract:** Due to miniaturization of circuit's mobility degradation, velocity saturation and power dissipation issues are critical in the design of VLSI circuits. In this paper various techniques to minimize power dissipation due to glitches are discussed. Total power consumption consists of two major parts like static power consumption and dynamic power consumption. In the total power, the static power is 30% and dynamic power is 70 %. The power due to glitches is 70% of the dynamic power and 30 % of the total power. Various methods are developed by researchers to minimize the power due to glitches.*
***Keywords:** Glitch, CMOS, Static & Dynamic Power, Switching Activity, Propagation delay, Resistive Feed through Cell.*

I. INTRODUCTION

One of the major factors which contribute to the power consumption in CMOS combinational logic circuits is the switching activities in the circuits. Many of such switching activities are due to spurious pulses, called glitches. A glitch is a fast spike which is unwanted. A hazard is a circuit which may produce a glitch. A glitch is called to an invalid and unpredicted output of a digital circuit that can be read by the next stage and result in a wrong action. Glitches happen mostly due to propagtion delays in a digital circuit. For example assume a circuit as below:

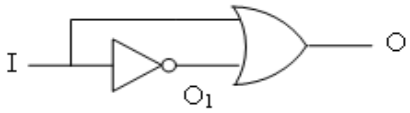

Figure 1: Glitch

When input I=1, the output is 1 as one of the inputs to the OR gate is one. When I=0 also the output is 1 as the output of the inverter will be 1 going to the OR gate. So for both these cases the output should remain as 1.

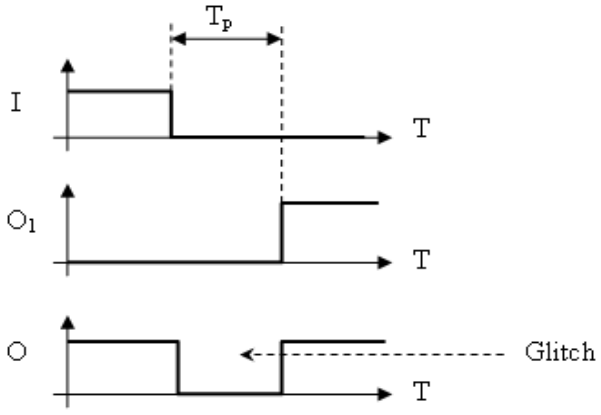

Figure 2: Timing Diagram

When the input change from 1 to 0, it takes a short time for the inverter to provide a 1 at its output due to its propagation delay. Therefore for that short period of time both inputs to the OR gate are zero, resulting in a zero at the output of the OR gate. Then finally after the inverter output changes to 1, the OR gates output changes to one too. This example shows happening of an

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unexpected zero at the circuit. This is a glitch and can cause problem for the rest of the circuit as it will propagate into the next circuits and result in more and more glitches.

Low power circuit design is one of the major topics of research in design automation. The power consumed in CMOS combinational logic circuits is heavily dependent on the switching activities in a circuit. Such switching activities are largely determined by the input switching patterns and the structure of the circuit. Many researchers have studied how switching activities are to be modeled and the determination of optimal circuit structure for power reduction. Signal switching in combinational circuits occurs for different reasons. Input signal transitions take place at different times in a clock cycle. Different logic gates are sensitive to different types of transitions in the inputs. Also propagation delays of the gates may differ. These entire mean that a signal might go through several state changes before it reaches its steady state within a clock cycle. These spurious transitions are often called glitches. For low power design, glitching should be minimized because it causes power dissipation.

To estimate the power consumption of a circuit, we need to determine the number and locations of the glitches in order to minimize the power dissipation due to glitches. In a combinational circuit the power dissipation due to glitches could be as high as 20% of the total power consumption, and can be much more in some circuits such as combinational adders. The dynamic power dissipation, which is the dominant source of power dissipation, is directly related to the number of signal transitions in a circuit. A signal transition can be classified into two categories; a functional transition (steady-state transition) and a spurious transition (glitch). It is well known that glitches occupy a considerable amount in the signal transitions of a circuit. Glitches are extremely sensitive to signal propagation characteristics (delay). If we properly optimize timing characteristics such that the number of glitches is minimized, and if the area (power) cost for the optimization is small, we can expect that the power cost is well overcompensated and overall power dissipation is reduced by the glitch education. In static CMOS circuits, due to the imbalance

of delays among the different combinational paths ending at the output of a gate, the output signal might switch more than one within a clock period before it stabilizes. These extra transitions are called glitches. Various techniques are developed by the researchers to minimize the glitches like gate sizing, gate freezing, balancing algorithm, buffer insertion, edge alignment and various statistical approaches.

II. MOTIVATION

The continuing decrease in the feature size and corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design. Excessive power dissipation in integrated circuits discourages their use in portable systems. It also causes overheating, which degrades the performance and reduces chip lifetime. The growing need for portable communication devices and computing systems has increased the need for optimization of power consumption in a chip. The low power design is a critical technology needed in the semiconductor industry.

III. POWER DISSIPATION BASICS

Un-necessary signal transitions that do not have any functionality are known as glitches [3]. Nowadays, power dissipation is a very burning topic, everybody in search of how to minimize power dissipation in daily use devices like laptops, mobile phones, mp3 players etc, particularly for handy devices because most of the gadgets today are battery operated that requires low power consumption. Total power dissipation consists of mainly dynamic power dissipation and static power dissipation, further these dynamic and static power dissipation divided in to others like leakage power dissipation, switching power dissipation and short circuit power dissipation as shown in equation (1) and (2).

$P_{total} = P_{static} + P_{dynamic}$ ..... (1)

$P_{total} = P_{Switching} + P_{Short\text{-}Circuit} + P\ leakage$..... (2)

Dynamic power dissipation is a major source of leakage power, that is directly proportional to the number of signal transitions (0 – 1 and 1 – 0) in a digital circuit. Signal transitions are of two types: functional transition and a glitch. According to reference glitch power dissipation is 20 % to 70 % of total power dissipation. By varying gate delays and path delays in the circuit glitches can be reduced to some extent. Glitches are the source of un-necessary power dissipation, misalignment of signal transitions and gate delays are the major sources for glitches in digital circuits. Switching power dissipation ($P_{Switching}$) is directly proportional to switching activity (α), load capacitance (C_{load}), supply voltage (V_{dd}) and clock frequency (f_{clk}) as shown in equation (3).

$P_{Switching} = \alpha \cdot C_{load} \cdot V_{dd}^2 \cdot f_{clk}$ .....(3)

Switching activity means charging and discharging of load capacitor also we can say transition from low to high level (0 – 1) and high to low level (1 – 0). As glitches are dependent on signal transitions so more switching activity will result in more glitches in a

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digital circuit and more power dissipation will be there. According to equation (3) switching power dissipation can be controlled by controlling switching factor, voltage scaling etc.

IV.TECHNIQUES

When transitions are applied at inputs of a gate, the output may have multiple transitions before reaching a steady state. Among these, at most one is an essential transition, and all others are unnecessary transitions often called glitches or hazards. Because switching power consumed by the gate is directly proportional to the number of output transitions, glitches reportedly account for 20%–70% dynamic power. A combinational circuit is minimum transient energy design, i.e., there is no glitch at the output of any gate, if the difference of the signal arrival times at every gate's inputs remains smaller than the inertial delay of the gate. This condition is expressed by the following inequality:

$$t_n - t_1 < d_i$$

where we assume t1 is the earliest arrival time at inputs,tn is the most delayed arrival time at another input, and diis gate's inertial delay, as illustrated in Figure 4.The intervaltn−t1 is referred to as the gate output timing window. To satisfy inequality, either increase the inertial delay di (hazard filtering) or decrease the path delay differencetn−t1 (path balancing)[2].

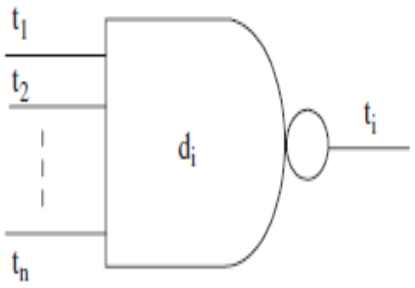

Figure4. n-input NAND gate

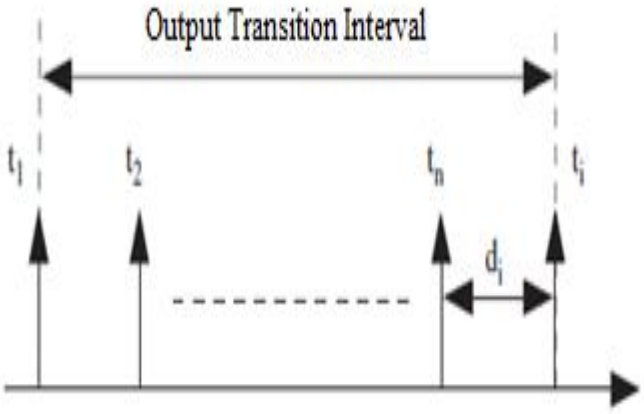

Figure5. Transition timing for the inputs and output of NAND gate

A. Resistive Feedback Power Optimization

The formulation might become non-linear, since changing the W/L ratio of a MOSFET changes the channel resistance as well as the associated parasitic capacitances Thus, an n-diffusion capacitor and a resistor wire with a blocking mask is developed. The blocking mask increases the resistivity of the polysilicon resistor. To simulate a realistic situation, each delay element is driven by an inverter gate and is also loaded with an inverter. The circuit set up is shown in Figure 6.The inverter and the transmission gate cells are made of transistors with minimum sizes. Figure6. Circuit setup for resistive load placement.

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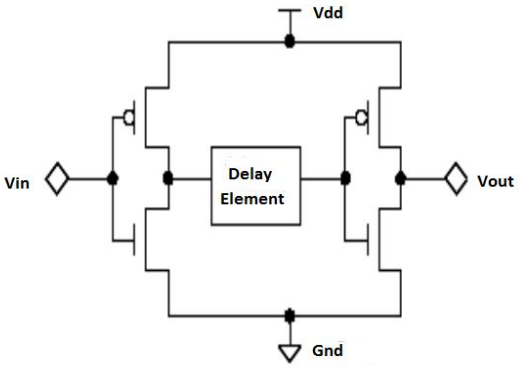

Figure6. Circuit setup for resistive load placement

he delay elements are implemented as standard cells with fixed height, the area is measured in terms of the number of grid units along the width. This delay element is called as resistive feedthrough logic. The resistance of a rectangular slab of length L, width W and thickness t can be calculated in terms of a material specific constant called resistivity ρ, as R=ρL/(Wt).

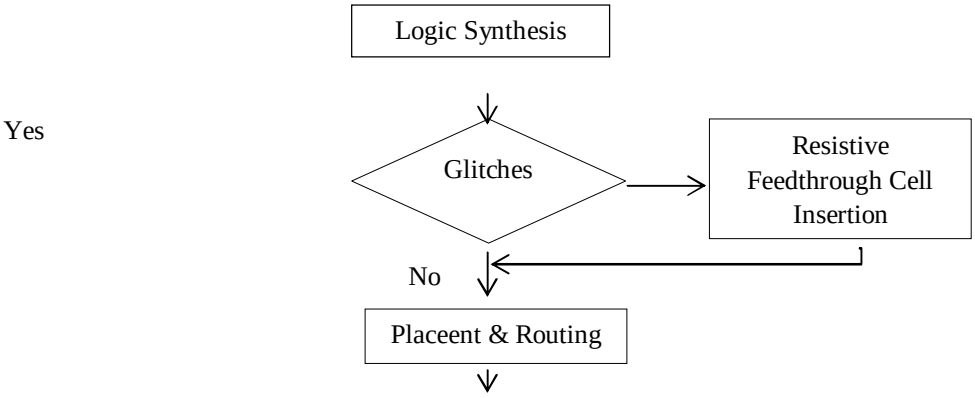

Figure 7. The new Low Power driven design flow

B. Reducing Switching Voltage

The dynamic power of digital chips expressed by Equation (3) is generally the largest portion of power dissipation. It consists of three terms voltage, capacitance and frequency. Due to the quadratic effect of the voltage term reducing the switching voltage can achieve dramatic savings. The easiest method is to reduce the operating voltage of the CMOS circuit. There are many trade-offs to be considered in voltage reduction. Performance is lost because MOS transistors become slower at lower operating voltages. The main reason is that the threshold voltages of the transistors do not scale accordingly with the operating voltage to avoid excessive leakage current.

V. CONCLUSION

Discussed different concepts of techniques for glitch reduction in VLSI circuits. Here some conclusions were made according to the references.The need for lower power systems is being driven by many market segments. Unfortunately designing for low power adds another dimension to the already complex design problem and the design has to be optimized for power as well as Performance and Area. Glitches can be minimize by reducing switching Activity and inserting resistive feed through cell.

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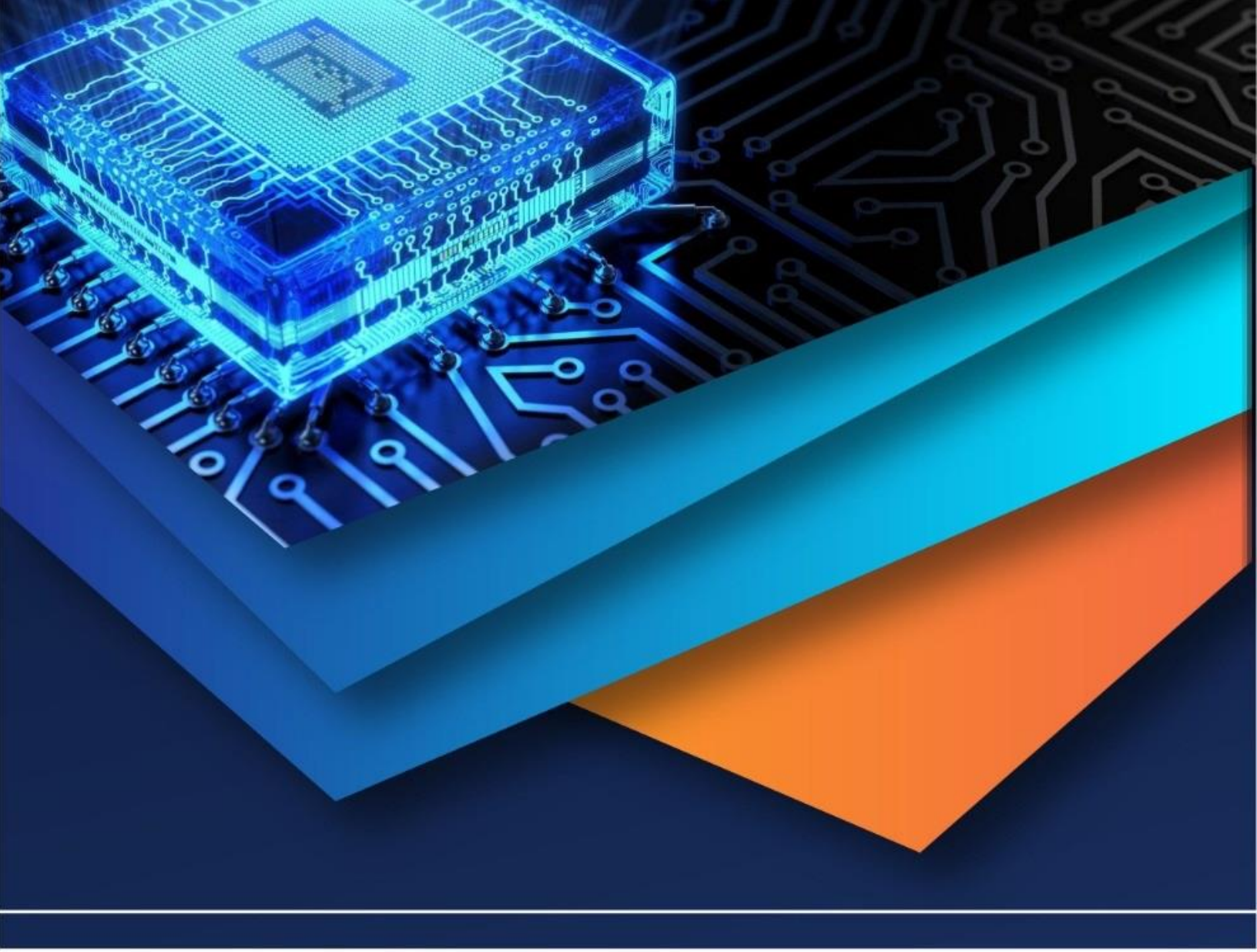

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