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Area Efficient Thermal Aware Testing Using Scan Chain Architecture

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Abstract: Increasing chip temperature is a major reliability concern since various failure mechanisms are accelerated at high chip temperature, which require thermal-aware testing to detect them. External devices like thermal chambers are usually used to heat up the chip to a desired temperature in order to apply the test. However, there are many limitations for these external devices, which make the thermal-aware testing of the FPGA a challenging process. In this paper, a self-heating approach for thermal-aware testing of FPGAs is presented, in which the internal resources of FPGA are used to build controlled self heating elements (SHEs). These controlled SHEs are distributed across the FPGA and integrated with the built-in self-test (BIST) scheme to generate the required temperature profile for testing. Thus, no external devices for heating up the FPGA are needed. The experimental results show that a wide range of maximum chip temperatures can be achieved (from 50◦C up to 125◦C onVirtex-5 FPGA) with a high accuracy (/ 1◦C).
Keywords: SHEs, BIST, FPGA

I. INTRODUCTION

A Built – In Self-Test or Built – In Test is a mechanism that Permits a machine to test itself. Engineer Design BIST tomeet requirements such as

A. High reliability
*B.*Lower repair Cycle Times

The main Purpose of BIST is to reduce the complexity, and thereby decrease the cost and reduce reliance upon external (pattern – Programmed) test equipment. BIST Reduces cost in two ways.

1) Reduce test – Cycle Duration.
2) Reduce the complexity of the test/probe setup, by reducing the number of I/O signals that must be driven /examined under test control. The BIST name and concept originated with the idea of including a Pseudo random number generator (PRNG) and a cyclic Redundancy Check (CRC) on the IC. If all the register that hold state in an IC are IC are on one or more Internal Scan Chains. Then the function of the register and the Combinational logic between them will generate a unique CRC Signature over a large enough sample of the random inputs.
3) *The complexity issue*. As the complexity of VLSl systems increases, we ask if the testing problem can be partitioned. The answer, unfortunately, is no. For example, consider two devices connected in a cascade. There is often no simple way to derive tests for the cascade from the given tests for its individual parts. Another possibility is the use of a hierarchical approach. The complex design automation problems of synthesis and physical design are often solved through hierarchical procedures. The testing problem, however, is not easy to solve with traditional hierarchical techniques. For example, no simple method exists for deriving a board test from tests for chips on the board. BET, however, does offer a hierarchical solution to the testing problem. Consider the testing of a chip embedded in a board that is a part of a system. The top down hierarchy consists of system, boards, and chips. Suppose all levels of the hierarchy use BIST. To test the chip, the system sends a control signal to the board, which in turn activates self-test on the chip and passes the result back to the system. Thus, BIST provides efficient testing of the embedded components and interconnections, reducing the burden on system-level test, which need only verify the components' functional synergy.
4) *The quality issue.*A product's quality depends on the tenacity of its tests. Test tenacity or ability is most frequently measured as coverage of single stuck at faults. Thus, we calibrate tests according to their ability to detect single lines that appear as if shorted to ground (stuck-at4) or to the power supply (stuck-at-1). Since the kind and number of faults that occur depends on the type of device (chip, board, and so on) and the technology (CMOS, bipolar, GaAs), evaluating test quality can be a complicated task.3 In general, quality requirements such as 95% fault coverage for complex VISI chips or 100% coverage of all interconnect

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faults on a printed circuit board (PCB) are based on practical considerations. The test engineer tries to achieve a low *reject ratio* (percentage of faulty parts in the number passing the test)-for example, 1 in 10,00&while controlling the cost of test generation and application. For very large systems, such requirements are achievable only through DIT. Our discussion will show that BIST is the preferred form of DIT.

5) *Test generation problem***.:**pointed out earlier, the problem of generating tests is difficult to solve by using hierarchy. The difficulty lies in carrying the test stimulus through many layers of circuitry to the element under test and then conveying the result again through many layers of circuitry to an observable point. BIST simplifies this problem by localizing testing.

6) *Test application problem.*For almost a decade, incircuit testing (ICT) has dominated the PCB testing scene.4 In this method, a bed of-nails fixture customized for the board under test enables the tester to access the pins of the chips mounted on the board. ICT effectively applies chip tests for diagnosis and also effectively tests board wiring. The method, however, presents several problems. First, ICT is effective only after a board is removed from the system; therefore, it is no help in system-level diagnosis. Second, in surface mount technology (SMT), components are often mounted densely on both sides of the board. Bed of- nails fixtures for such boards are either too expensive or impossible to build. BET offers a superior solution to the test application problem. First, built-in test circuitry can test chips, boards, and the entire system without expensive, external automatic test equipment. Second, for off-line testing of boards and chips and for production testing, we can use the same tests and test circuitry that we use at the system level.

II. LITERATURE OF SELF – HEATING BIST FOR FPGA'S

In order to meet performance, cost, and power demands, Field Programmable Gate Arrays (FPGAs) are designed and fabricated using the most advanced nano-scale technology nodes. State-of the- art FPGAs are built using 28 nm high-κ/metal gate materials [1], which enable them to reach an integration density of up to 6.8 billion transistors per chip .

FPGAs based on 20 nm and 14 nm technologies were recently announced. This excessive downscaling and the very high integration densities are faced with many manufacturing and reliability challenges such as process variation, sub-threshold leakage, thermal dissipation, increased circuit noise sensitivity, and reliability concerns due to transient and permanent failures.

Testing of FPGA chips therefore, is of great importance not only at the manufacturing phase, but also during the in-field operation to ensure the correct functionality throughout the system lifetime. As many failure mechanisms are accelerated with high chip temperatures, thermal-aware methods of testing are usually used to detect such failures, and also to ensure the quality of the devices for a required thermal specification. In this type of testing, the chip is first heated to a certain temperature and then the test is applied. External devices such as thermal chambers and

ovens are used for the purpose of heating up the chip. Burn-in testing is another type of testing in which the chip is exposed to high temperatures and/or voltages for certain periods in order to accelerate the aging and stress the chip before applying the test.

Again, in this type of testing external devices are used for heating up the chip. However, the use of these devices for thermal-aware testing has various limitations. For instance, they cannot provide on-chip thermal gradient for thermal testing; they are large and expensive, and have limited usability for in-field test; there is a possibility of heating up unwanted components on the board; and the number of chips that can be simultaneously tested is limited.

III. PROPOSED PAPER SELF – HEATING BIST FOR FPGA'S:

The Proposed Self – Heating approach can be combined with various BIST Schemes for FPGA Testing to Create a thermal – aware BIST.

The Main steps for integrating the proposed self – Heating for FPGA devices with BIST Structures.

A. BIST Integration

1) FPGA Devices Consists of 3 main Sets of Components

*a)*Test Pattern Generators (TPG's)

*b)*Block Under Test or Circuit Under Test (B/CUT)

*c)*Output Response Analyzer (ORA's)

*2)*TPG is used for generating the required input patterns for testing targeted Circuits.

*3)*Block/ Circuit under Test which represents the blocks of the FPGA to be tested.

*4)*Output Response Analyzers(ORA's) which determine whether the output of the BUT are Valid.

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To Test all resources of the FPGA and achieve 100 % Coverage, Several test Configuration are generated in a such way that each resource appears in at least one test configuration as B/CUT.

B. There are two ways of self-heating with BIST structure can be done

*1)*Sequential Method :

*2)*Concurrent Method:

C. Sequential Methods

1) In this method, the self-heating and the self-testing are done in two consecutive steps. First the FPGA is loaded with the SHEs (heat configuration) for heating up the chip to the desired temperature.

*2)*Afterwards, the BIST test configuration is loaded on the FPGA for testing. In case the test requires multiple reconfigurations, this process of consecutive heating and testing is repeated before the application of each test configuration.

*3)*The main advantage of this method is that there is no need to modify the original BIST structure. Additionally, the whole FPGA resources are available to the SHEs during the heating step.

*4)*The controlling of the temperature can be done only during the execution of the heating step.

*5)*During the testing step, the temperature will vary.

Thus, depending on both the configuration time and execution time of each test configuration on the FPGA, the precision of the thermal control may decrease. Although, the FPGA can be heated above the desired temperature during the heating step to compensate the cool down that may happen, this still does not allow accurate temperature control during the test steps.

D. Concurrent Method

1) In this method, the SHEs are integrated with the BIST structure into a single Heat&Test configuration. This is done by adding a fourth set of components to the BIST structure representing the SHEs as shown in Figure.

*2)*The main advantage of this method is the accurate control of the test temperature. Furthermore, the total number of required Heat&Test configurations, and hence the total test time, is less compared to the sequential method.

3) However, this integration requires additional design efforts depending on the original BIST structure.

*4)*The original BIST structure has to be modified in order to free up enough logic resources for the SHEs.

This can be done in several ways, again depending on the targeted BIST structure:

By reducing the number of BUTs that are tested at the same time and scaling down the other BIST components accordingly. This will also result in an increase to the total number of configurations, compared to those in the original BIST method,

by decreasing the size of the ORAs in such a way that the fault detection coverage is preserved but the diagnosis resolution is diminished. Because of the main advantages of this method over the sequential method, the concurrent method is adopted in the rest of this paper.

IV. METHODOLOGY

In this paper, we present an approach for self-heating the FPGA chips for the purpose of thermal-aware testing. Thus, no external devices are needed. In our approach, the internal logic resources of FPGA are used to build controlled Self-Heating Elements (SHEs). These SHEs are very flexible in both size and quantity, they can be either distributed across the FPGA to heat up all the FPGA at once, or they can be concentrated in a certain part of the FPGA to generate the required thermal gradient across the chip. Furthermore, we developed a simple programmable controlling scheme to tune the amount of generated heat according to the test requirements.

The SHEs are integrated with the Built-In Self-Test (BIST) scheme

for FPGAs, which allows any specific thermal profile during test by specific placement of SHEs throughout the chip as well as programming SHEs for particular heat generation. In that way, the required testing temperature is maintained throughout the test. The proposed approach has many advantages. First, it eliminates the need for any external devices for heating, and thus reducing the testing cost and assuring heating only the FPGA chip and not any other components on board. Unlike the external heating devices, it can generate uniform temperature or particular thermal gradient on the chip for specific test plans. Furthermore, it can be used for in-field thermal-aware testing by end users.

Additionally, there is no limitation on the number of FPGA chips to be heated in parallel and hence reducing the test time. Moreover, this technique can primarily be used for thermal-aware testing as a part of manufacturing and production test flow. Also,

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it can be used as a part of acceptance test by the user in the field. The presented approach is demonstrated on a Spartan-3E FPGA and integrated with a particular FPGA BIST scheme. The experimental results show that a wide range of maximum chip temperatures can be achieved (from 50◦C up to 125◦C) with a high accuracy (1◦C).

A. The concept of self-heating:

The idea of self-heating is to make the FPGA able to generate heat by increasing the power consumption of its elements. This can be achieved in several ways e.g., creating intentional short circuits, forcing high toggling rates at the inputs/outputs of the FPGA resources, etc. The approach that includes forcing of high toggling rates is safer and straightforward to implement and control, and thus it is preferred. Forcing high toggling rates can be applied to most FPGA resource types such as Block-RAMs or Digital Signal Processing (DSP) elements. However, most of these resources are concentrated in a few locations on the FPGA die and may not be available at all in different FPGA chips. Therefore, if an even temperature distribution across the FPGA is desired, these types of resources are unsuitable to implement self-heating. On the other hand, logic resources are well distributed across the FPGA, which makes them a good candidate for being used for the implementation of self-heating modules. Usually the logic resources consist of a set of look-up tables (LUTs) and flip-flops (FFs) as well asswitching/ routing resources and multiplexers.

B. Self-Heating Elements (SHE's) :

In this paper, the main components to implement the proposed SHEs are LUTs and FFs. As these resources are available in a large number and evenly distributed across the FPGA, the SHEs can be freely placed in any desired location on the FPGA and thereby their density and quantity can be controlled, which determines the amount of heat generated in order to achieve the desired final on die temperature distribution.

C. Basic Toggle Logic:

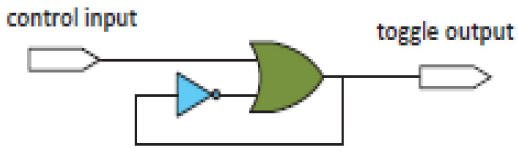
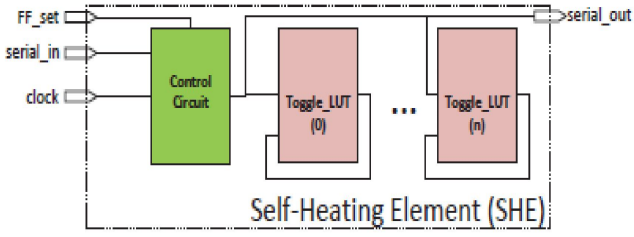


Fig : Basic Toggle Logic Circuit

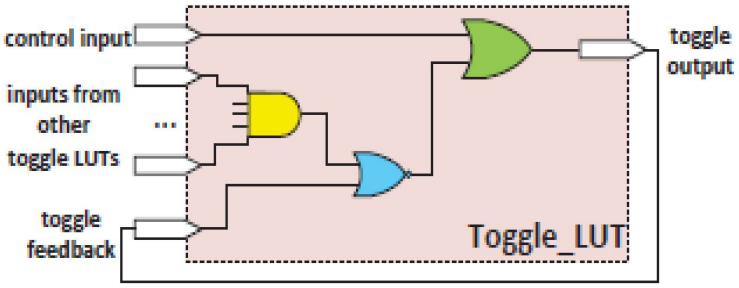
The basic circuit for controlling input/output toggling is depicted in Figure 1. It consists of a basic ring oscillator with an additional signal to control the toggling rate. This circuit can be realized using an LUT with at least two inputs. Usually, the feedback signal from the LUT output to its input goes through switching resources, which cause these resources to toggle as well and hence their dynamic power consumption will increase in turn, enabling more heat to be generated.

D. Toggle Logic With additional Inputs :

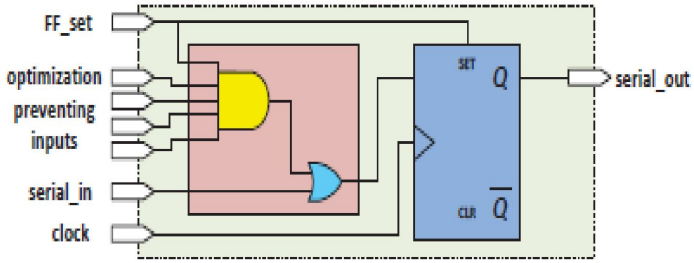


For larger LUTs (e.g. with 6- inputs), it is preferable to toggle all the inputs in order to maximize the power consumption. This can be achieved by connecting the feedback signal to all inputs. To maximize the power consumption, each of the proposed SHEs consists of several toggling LUTs. Figure 2 shows an overview of a single SHE. It consists of a set of toggling LUTs in addition to a control circuit. The logic function implemented by each toggling LUT is depicted in Figure 3. Basically, this is an extension to the circuit in Figure 1 to achieve toggling on the rest of LUT inputs by connecting them to feedback signals from other LUTs.

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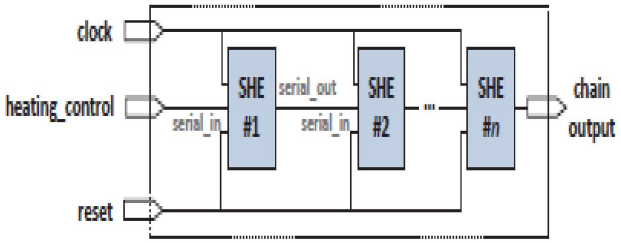


The control circuit depicted in Figure 4 sends the (serial out) signal to all (control input) ports of toggling LUTs inside the SHE. The circuit consists of a FF working as a shift register to store the toggling control signal (serial in) for one clock cycle. The (FF_set) signal is used to stop the toggling asynchronously by forcing the output of the FF to '1'. The "optimization preventing inputs" are inputs from toggle LUTs inside the SHE to prevent any possible deletion of their signal by the FPGA tools.



E. Chain of SHEs

A single SHE can have as many toggling LUTs as possible. However, the larger the SHE the more routing complexity it poses, which can restrict its placement on the FPGA. Furthermore, in a single SHE, all of the toggling LUTs can be either in toggling mode or stopped, all at the same time. Thus, if an SHE contains too many LUTs, a fine control of the generated temperature cannot be achieved.

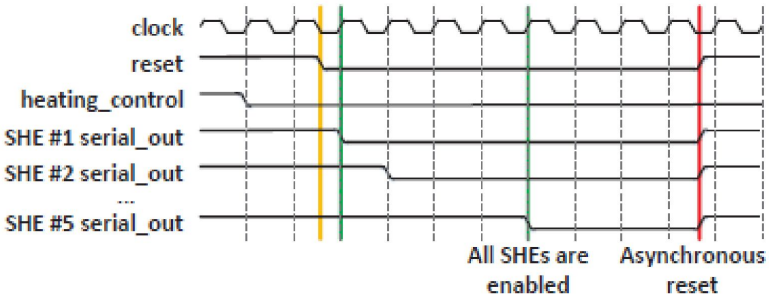


Based on the above statement, small SHEs (e.g., each with up to 10 toggling LUTs) are more preferable. Moreover, local routing can be used instead of global routing resources, and the serial out signal has less routing overhead. Consequently, the footprint of each SHE is less and more space is left for any BIST circuitry to be implemented concurrently with the SHEs. Furthermore, it is easier to distribute small SHEs across the FPGA than the larger ones for better heat distribution and control.

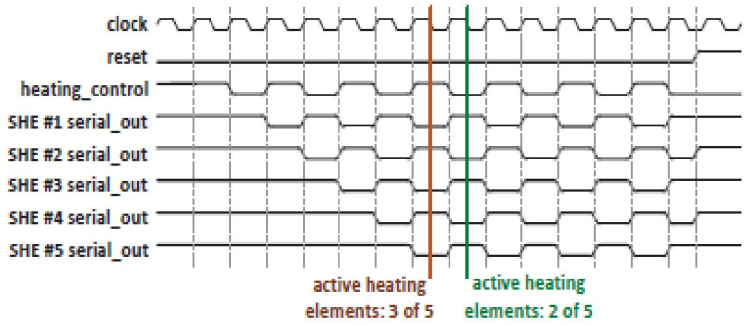
In order to have a simple control for the SHEs across the FPGA, the serial in and serial out ports of multiple SHEs are connected together resulting in a *Self-Heating Chain* (SHC), as depicted in Figure 5. The advantage of this connection is having the ability to control how many SHEs are toggling or stopped inside the SHC using a single control signal and hence, controlling the amount of heat generated from that SHC. This process is explained next. Furthermore, the SHC can contain an arbitrary number of SHEs, which gives more flexibility in its placement on the FPGA.

In each SHE in the chain, the toggling of the LUTs and the propagation of the control input signal are delayed by the control circuit for one clock cycle, as mentioned earlier. Therefore, in order to make all SHEs in the chain toggle, after a reset, the first control input of the SHC heating control) has to be '0' for as many clock cycles as there are SHEs in the chain. A timing diagram showing this process is depicted in Figure 6.

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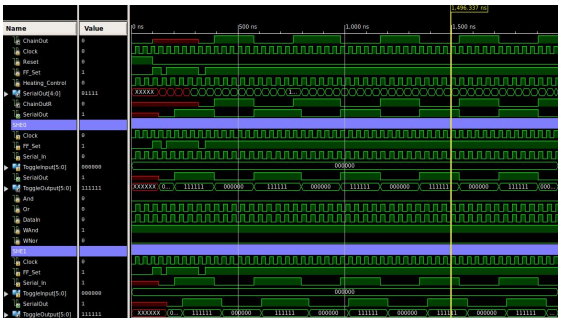


For controlling the amount of heat generated from the SHC, an input with a certain duty cycle can be applied to the heating control signal, to switch the toggling of the individual SHEs inside the chain on and off. If, for example, only half of the SHEs are desired to toggle at the same time, the duty cycle of the heating control signal should be set to 50%, as shown in Figure 7, using a chain with 5 SHEs.



While each chain could be driven by an individual control input in order to determine its power consumption and thereby the onchip temperature distribution, a single input for all chains is used to control them. This simplifies the concurrent usage of self-heating with other BIST circuits on the FPGA.

F. Results

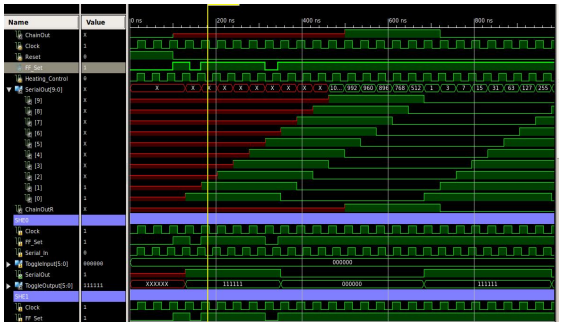


With Same Clkinput & Control Heating Input

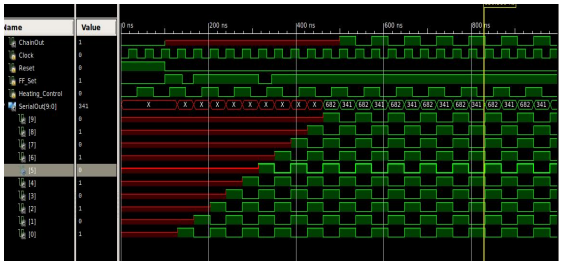


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G. Simulation of SHC with 10 SHE Elements of same clk and Control Heating Input Signal :



H. Simulation of SHC with 10 SHE Elements of same clk and double delay to change Control Heating Input Signal with reference to Clock :



In each SHE in the chain, the toggling of the LUTs and the propagation of the control input signal are delayed by the control circuit for one clock cycle, as mentioned earlier. Therefore, in order to make all SHEs in the chain toggle, after a reset, the first control input of the SHC heating control) has to be '0' for as many clock cycles as there are SHEs in the chain.
For controlling the amount of heat generated from the SHC, an input with a certain duty cycle can be applied to the heating control signal, to switch the toggling of the individual SHEs inside the chain on and off. If, for example, only half of the SHEs are desired to toggle at the same time, the duty cycle of the heating control signal should be set to 50%, as shown in Figure using a chain with 5 SHEs. 5SHE are generated to activate at one Duty cycle Period Remaining 5 SHE are at next Duty cycle period .
If both are Clocking and Serial_ In are at Same toggle Period it can be activated by one by one 5SHE Element by generating Heating Power Consumption.

V. CONCLUSION

Increasing chip temperature is one of the most important challenges that face chips at nano-scale, because of the direct relation between temperature and many reliability issues. Furthermore, various failure mechanisms are accelerated at high chip temperature, which require thermal-aware testing to detect them. External heating devices that are usually used in thermal-aware testing, suffer from many limitations. In this paper, we presented a self heating approach for thermal-aware testing of FPGA devices, in which the internal resources of FPGA are used to build controlled self-heating elements (SHEs). Thus, no external devices for heating up the FPGA are needed. The experimental results show that a wide range of maximum chip temperatures can be achieved (from 50◦C up to 125◦C on Spartan- 3E FPGA) with a high accuracy (}
1◦C).

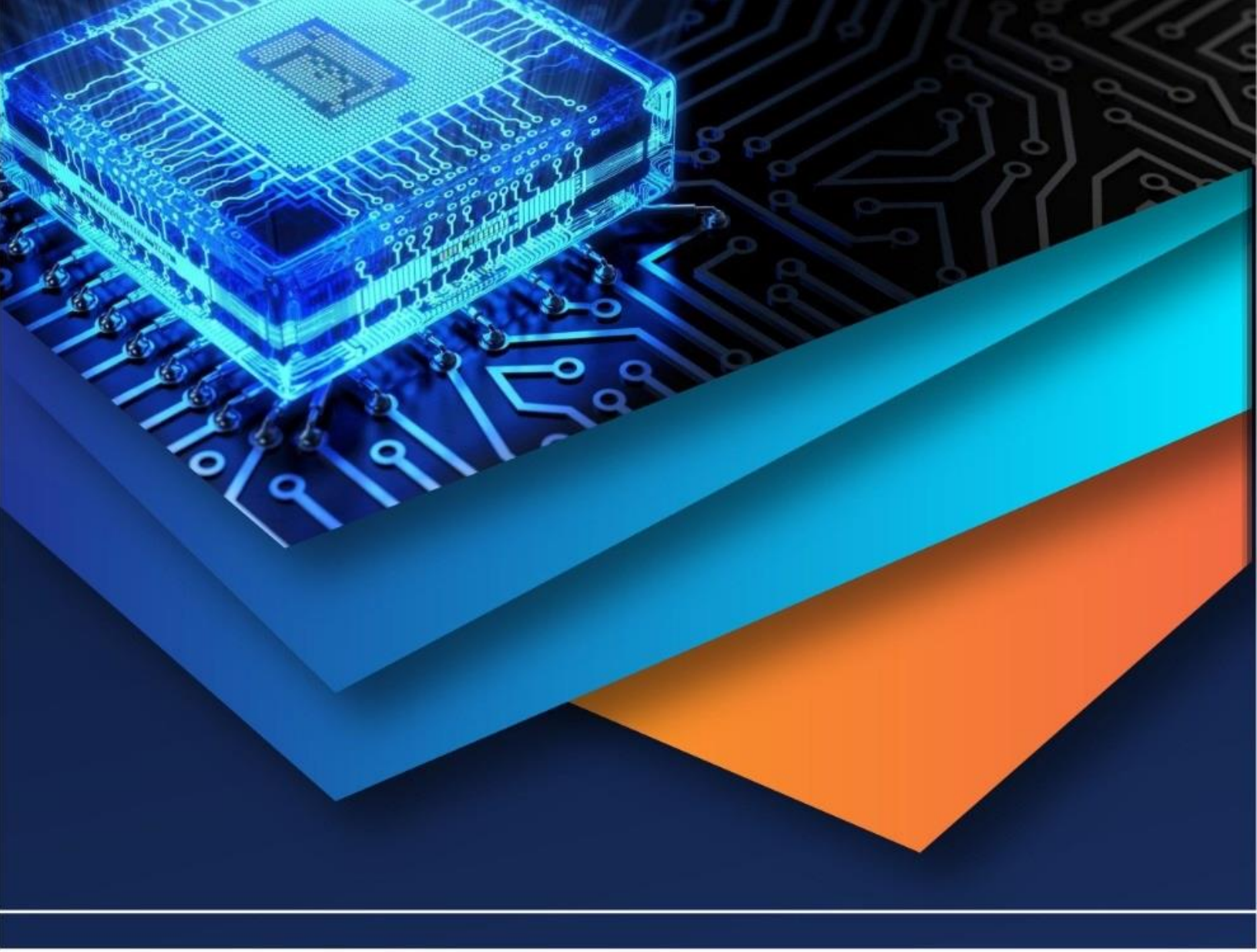
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