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# Area-Power Efficient Design of GDI 2-Bit Magnitude Comparator in 130 nm Technology by Logic Minimization

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***Abstract:*** ***Designing the circuit with optimal constraints of VLSI is the need for every designer. Designers would normally like to go for lowest level of Design Abstraction in which the scope of Optimization is Maximum. GDI is a technique in which it has only one cell and it normally saves the Area of a Design. GDI technique with 130 nm process technology has been implemented using Spice Tool. There is 33% reduction in transistor count in comparison with existing GDI comparator due to the selection of the inputs to the GDI cell.***
***Keywords*****: *Optimization, Gate Diffusion Input Technique; Logic Minimization, Boolean Expression.***

## I. INTRODUCTION

Logic minimization is the crucial aspect in designing of VLSI circuits as it leads to better hardware. Comparator does have many applications. Comparator will be comparing two group of equal number of bits and output the result of A>B, A<B and A=B.

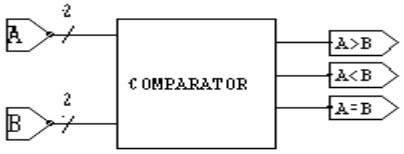


Fig. 1 Comparator symbol with 2 bits.

Fig.1 is the 2- Bit magnitude comparator and it compares two numbers A and B and gives output A>B as 1 when B is having less binary weighted value in comparison with A and A<B as 1 when B is having more binary weighted value in comparison with A. A=B is a function of nor operator with operands as A<B and A>B. GDI is a technique in which different logics can be achieved by a single cell[8].Comparator Designed by using Arithmetic operation with 30 Number of transistors[1].Power efficient method by using GDI has proposed in[2].Low Delay with CMOS Comparator proposed in [3].Mux based design of Comparator given in [4]. Low Area and Low Power Design of Comparator proposed in [5].Hybrid Design of Comparator given in [6]. Different Logic Styles design of Comparator proposed in [7].

## II. EXISTING COMPARATOR

Table1 shown below indicates Xor is the key module for Designing the Comparator[1] and normally in GDI technique, Xor needs more hardware when compared to And, Or and MUX 2to1. Whenever Designer uses more of the And,Or and MUX 2to1 then the Optimization scope will be maximum

Table1. Cells and transistor count

| Logic required | Number of cells | Total Transistor Count |
|---|---|---|
| XOR | 4 | 30 |
| AND | 2 | |
| NOT | 2 | |
| MUX 2 TO 1 | 2 | |
| NOR | 1 | |

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## III. DESIGN OF COMPARATOR

### A. *Symbol of GDI Cell*

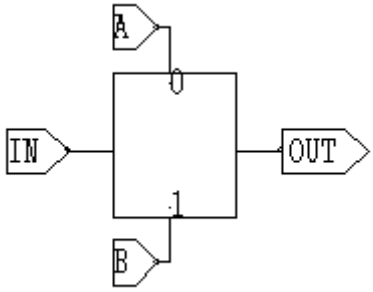


Fig. 2 Gate diffusion input symbol

Above figure 3.1 shows the working of GDI cell in which when IN=0 then A will be selected to the OUT and when IN=1 then OUT will be taking the B value.

### B. *Schematic of GDI Cell*

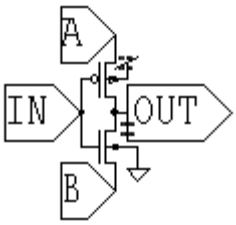


Fig. 3 Gate diffusion input schematic

Above figure 3.2 shows the Schematic representation of GDI Cell for the Symbol shown in Fig 3 in which the confirmation is that every GDI Cell consists of 2 Transistors.

### C. *Proposed Comparator Architecture*

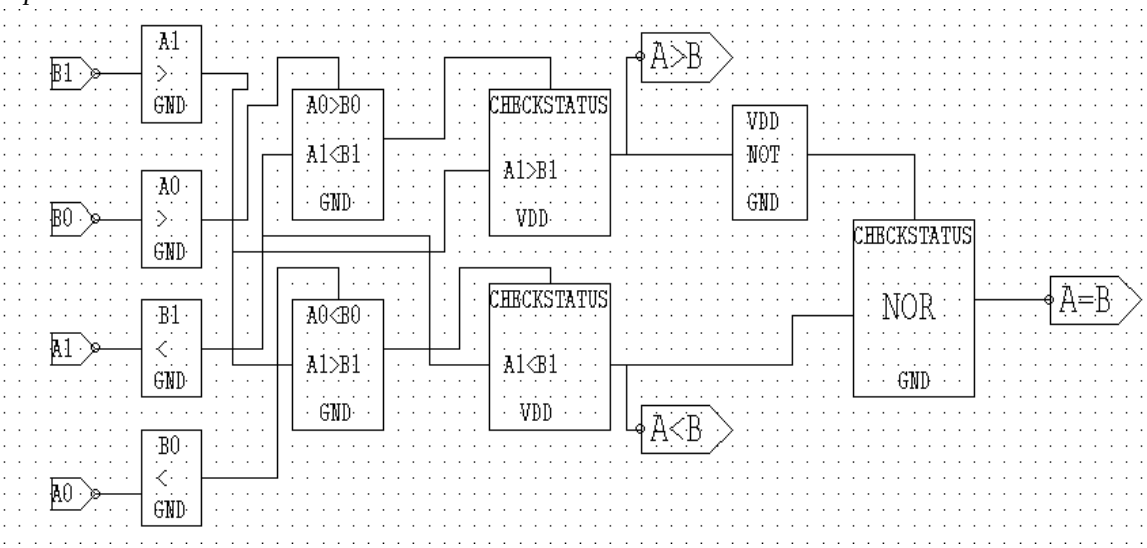


Fig. 4 Comparator architecture

Above figure 3.3 has 10 cells of GDI. Internally inside the box of GDI we have three identifiers, the top-most will be the source of the PMOS, the middle one will be the operation performed(Gate of GDI) and the bottom-most will be the source of the NMOS. Propose

X0=A1.B1……(1)
X1=A0.B0……(2)
Y0=A1.B1……(3)
Y1=A0.B0……(4)
A>B=X0+Y0.X1……..(5)
A<B=Y0+X0.Y1……..(6)
(A=B) = A>B +A<B……(7)

Table2. Functions performed by target assignment

| TARGET ASSIGNMENT | FUNCTION PERFORMED |
|---|---|
| X0 | A1>B1 |
| X1 | A0>B0 |
| Y0 | A1<B1 |
| Y1 | A0<B0 |
| A>B | A>B |
| A<B | A<B |
| A=B | A=B |

Table 3. Proposed Cells and transistor count.

| Logic required | Number of cells(Transistor Count) |
|---|---|
| > | 2(4) |
| < | 2(4) |
| MSB Status(>) | 2(4) |
| MSB Status(<) | 2(4) |
| NOR | 1(4) |

Table3 shows the logical cells required and also their individual transistor count as well as final count of the proposed design.

*D. Proposed Schematic of 2-bit magnitude comparator*

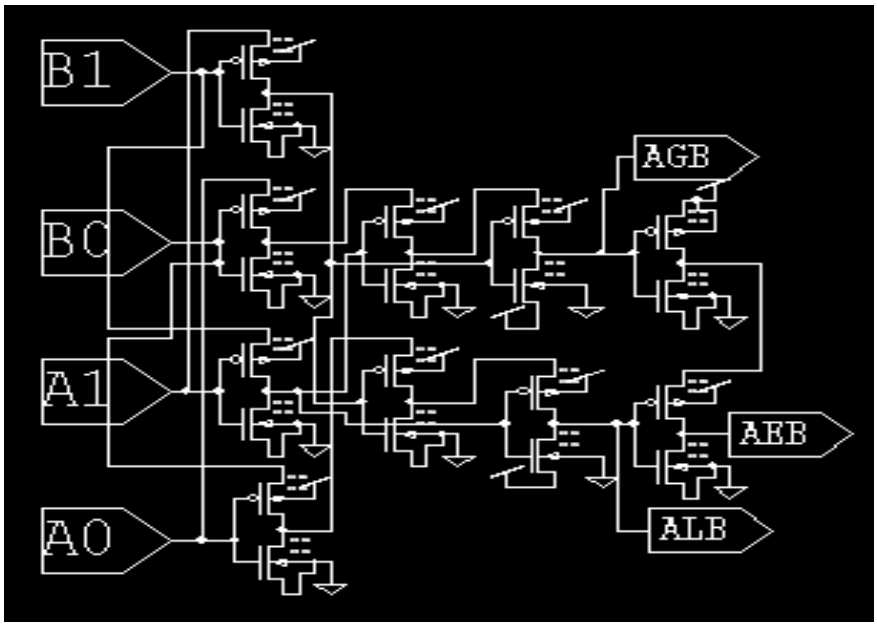


Fig. 5 Schematic of proposed 2-bit magnitude comparator

There are 2 combinations in which A>B can become true

*1)* A1>B

*2)* A0>B0 and (A1<B1 should be falseThere are 2 combinations in which A<B can become true

*3)* A1<B1

*4)* A0<B0 and (A1>B1 should be false)

As per the above figure 3.4 number of levels are 5 and in which

Level1 consists of 4 cells in which we can know the >, < status of MSB and LSB of the words.

Level2 consists of 2 cells to know the previous bits of A ,B.

Level3 consists of 2 cells to give the outputs of A>B and A<B.

Level4 consists of 1 cell to give the complimented version of A>B.

Level5 consists of 1 cell to give the output of A=B.

If A1>B1 is True then level1(row1-column1) cell will give output '1' and this will activate level3(row1-column1) cell and we get A>B output as high.If A1>B1 is True then level1(row3-column1) cell will give output '0', level2 (row2 –column1) cell will give output '0' and the level1(row3-column1) cell will activate level3(row2-column1) and we get A<B output as low.If A1<B1 is True then level1(row3-column1) cell will give output '1' and this will activate level3(row2-column1) cell and we get A<B output as high.If A1<B1 is True then level1(row1-column1) cell will give output '0', level1 (row3 –column1) cell will give output '1' and the level1(row3-column1) cell will activate level3(row1-column1) and we get A>B output as low. If A1>B1 is False then CHECK STATUS which is the result of Y0.X1 will decide the Output of A>B. If A1<B1 is False then CHECK STATUS which is the result of X0.Y1 will decide the Output of A<B.

## IV. RESULTS

All the possible combinations of 2-bit magnitude comparator in an binary (A[MSB:MSB-1], B[LSB+1:LSB]) from "0000" to "1111" are applied and the Output results from A=B, A<B and A>B in an top to bottom order of the waveform are shown below at Volts of 4,3, 2 and 1 supply voltage in Fig.4.1, 4.2, 4.3 and 4.4 accordingly.

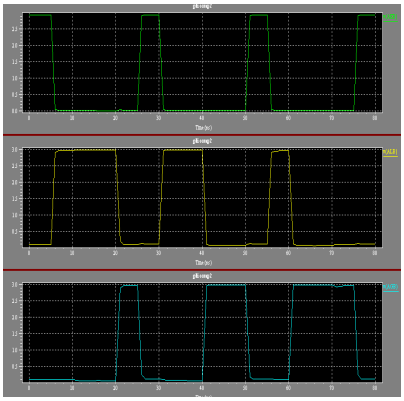

Fig. 6 Supply voltage of 4 volts

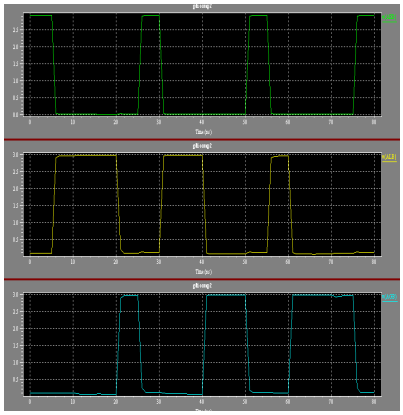

Fig. 7 Supply voltage of 3 volts

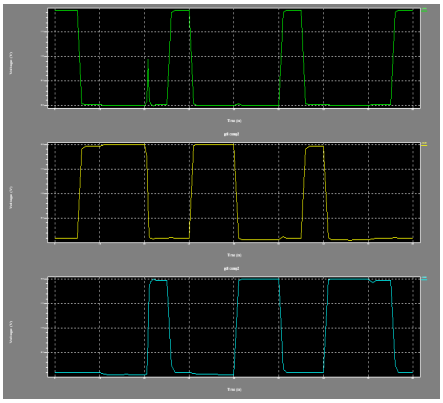

Fig. 8 Supply voltage of 2 volts

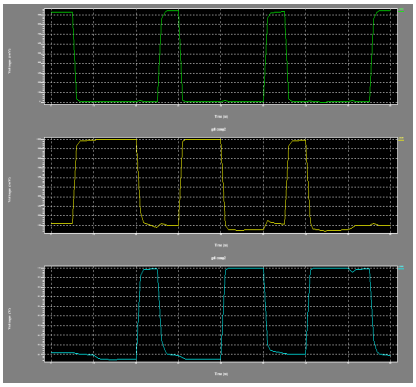

Fig. 9 Supply voltage of 1 volts

Table4. Logic levels degradation for A=B with varying supply voltages.

| SUPPLY VOLTAGE | (A=B) LOGIC '0' DEGRADATION(WORST CASE) | (A=B) LOGIC '1' DEGRADATION(WORST CASE) |
|---|---|---|
| 4V | 0.02 V | 0.06 V |
| 3V | 0.02 V | 0.06 V |
| 2V | 0.03 V | 0.06 V |
| 1V | 0.02 V | 0.08 V |

Table4 denotes that 0.02 V is the degradation of logic '0' and 0.06 V for logic '1' and it is not going to impact much the noise level margins of high and low.

Table5. Logic levels degradation for A<B with varying supply voltages.

| SUPPLY VOLTAGE | (A<B) LOGIC '0' DEGRADATION(WORST CASE) | (A<B) LOGIC '1' DEGRADATION(WORST CASE) |
|---|---|---|
| 4V | 0.13 V | 0.04 V |
| 3V | 0.11 V | 0.04 V |
| 2V | 0.09 V | 0.05 V |
| 1V | 0.15 V | 0.02 V |

Table5 indicates that 0.15 V is the degradation of logic '0' and 0.05 V for logic '1' and it is having minor impact on the noise level margin of low and minimal impact on high level noise margin.

Table6. Logic levels degradation for A>B with varying supply voltages.

| SUPPLY VOLTAGE | (A>B) LOGIC '0' DEGRADATION(WORST CASE) | (A>B) LOGIC '1' DEGRADATION(WORST CASE) |
|---|---|---|
| 4V | 0.12 V | 0.04 V |
| 3V | 0.11 V | 0.04 V |
| 2V | 0.10 V | 0.06 V |
| 1V | 0.12 V | 0.02 V |

Table6 clarifies that 0.12 V is the degradation of logic '0' and 0.06 V for logic '1' and it is going to impact noise immunity of the circuit considerably in logic '0' state and minimal in logic '1' state.

Table7. Transistor count comparison for existing and proposed.

| Area | Design in reference1 | Proposed |
|---|---|---|
| Number of GDI Cells | 15 | 10 |

Table7 specifies that 5 GDI cells are optimized and this will make sure that considerations of VLSI like Area, Power, Delay and Cost will be better.

Table8. Power consumption with different clock frequency and varying supply voltage.

| CLOCK FREQUENCY | SUPPLY VOLTAGE | | | AVERAGE POWER CONSUMPTION | | |
|---|---|---|---|---|---|---|
| 200 MHZ | 4V | 3V | 2V | 2.670608e-004 watts | 1.281257e-004 watts | 4.652350e-005 watts |
| 1000 MHZ | 4V | 3V | 2V | 2.868603e-004 watts | 1.473450e-004 watts | 5.488411e-005 watts |

Table8 mentions that if optimization goal is low power then select clock frequency 200 MHZ with supply voltage of 2V. If the constraint of interest is power -delay product then go for 1000MHZ clock frequency with supply voltage of 2V.

## V. CONCLUSION

Designing a circuit in GDI has complications like Noise Margin levels reduction and this has to be addressed. Results which we have got shows marginal reduction in Noise Margin Levels for different power supply voltages. Proposed Design can also be implemented for Low Power Applications. When the Optimization goal of a Design is Speed then by increasing Supply Voltage we can achieve Low Delay. Area Reduction has been possible due to the way we have applied the intermediate inputs to the terminals of GDI cell.

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