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A Design for Improved Very Low Power Static Flip Flop Using Two Inverters and Five NORs

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Abstract: ***This article proposed an improved very low-power static flip-flop (IVLPSFF) for very low power VLSI applications. The proposed IVLPSFF has two numbers of NOTs (inverter) and five numbers of NORs. It has a root clock for the generation of the positive edge triggered clock signal for the purpose of transmitting the data into the master flip flop. Whereas the negative edge triggered clock signal for the holding of data in the slave flip flop. The proposed method utilized 24 transistors. The simulation results for the 45nm standard CMOS procedure revealed that our method IVLPSFF attained delay in the order of 1.558 ns, power dissipation of 0.915 nW at 1.11 to 2 MHz clock frequency and 0.35V power supply. For the proposed design the layout area is 8.568µm which is very narrow as compared to other methods.***
Keywords: Improved Very Low-Power Static Flip-Flop (IVLPSFF), Flip Flop, Logic Gate, Power, Delay, Area, DRC, LVS.

I. INTRODUCTION

Low-power CMOS VLSIs have involved much attention for use in control aware applications, for example, wireless smart sensor networks and implantable bio-medical systems. Several low power techniques have been investigated. Among them, lessening the supply voltage for digital circuits is the most immediate and compelling way to achieve low power dissipation, because of the quadratic reliance of the power dissipation on the supply voltage. One major issue for low voltage digital circuits is in the designing of a flip-flop circuit. Because FFs are broadly utilized as a part of present day digital VLSI systems for example, a general purpose register, a pipeline register, and a finite state machine.

In this article, we herein propose an Improved Very Low-Power Static Flip-Flop (IVLPSFF) for extremely low power digital circuits. The IVLPSFF has two numbers of NOTs (inverter) and five numbers of NORs. The count of transistors is twenty four, which is the same as the conventional circuit shared static flip flop (CSSFF). Our proposed IVLPSFF attained delay in the order of 1.558 ns, power dissipation of 0.915 nW at 1.11 to 2 MHz clock frequency and 0.35V power supply. For the proposed design the layout area is 8.568 µm which is very narrow as compared to other methods.

II. RELATED WORK

Existing Techniques areCircuit Shared Static Flip Flop (CSSFF), Tri-state buffer based flip-flop (TBFF)**,** NAND latch based flip-flop (NLFF), Contention less flip-flop (CLFF)**.** The CSSFF is the most useful technique when compared to other conventional techniques, but the power dissipation and delay was not optimized. The CSSFF consist of same 24 transistors like TBFF. TBFF is used in most standard cell libraries. However the use of the TBFF becomes difficult to operate at lower voltage like below the V_{th}. The main reason behind this is the yield of the tri state buffers are connected in wired-Or which leads to the increase of the power dissipation. The NLFF and CLFF consist of more number of transistors when compared to TBFF and CSSFF. If the transistor count was increased the area and power dissipation also increases. To achieve low power and less delay FF, we propose an Improved Very Low-Power Static Flip-Flop consists of NORs and INVERTERs with a small number of Transistors. Which can be operates at lower voltages.

III.PROPOSED METHOD

The Improved Very Low-Power Static Flip-Flop (IVLPSFF) has two numbers of NOTs (inverter) and five numbers of NORs (NOR_1-NOR_5) and the total number of transistors is 24 as shown in Fig. 1. The NOTs are used to generate control signals of CLKB and CLK_2 from root clock of CLK. NOR_1, NOR_2, and NOR_3 form a master flip flop, while NOR_3, NOR_4, and NOR_5 form a slave flip flop. Note that NOR3 is shared both in the master and slave flip flops, and is used to acquire data in the master and transfer it to the slave. In this way Low-Power Static Flip-Flop (IVLPSFF) works. The timing diagram of circuit operation is shown in the fig.4. The master operates using a positive edge of control signal of CLK_2. NOR_2 and NOR_3 form the master flip flop. Meanwhile, the slave operates using a negative edge of clock signal of CLK. Therefore, NOR_4 and NOR_5 form the slave flip flop, and the data is

held at Q as Data (D0). This way our proposed Improved Very Low-Power Static Flip-Flop (IVLPSFF) operates as a master-slave flip-flop with a small number of transistors**.**

IV. RESULT AND DISCUSSION

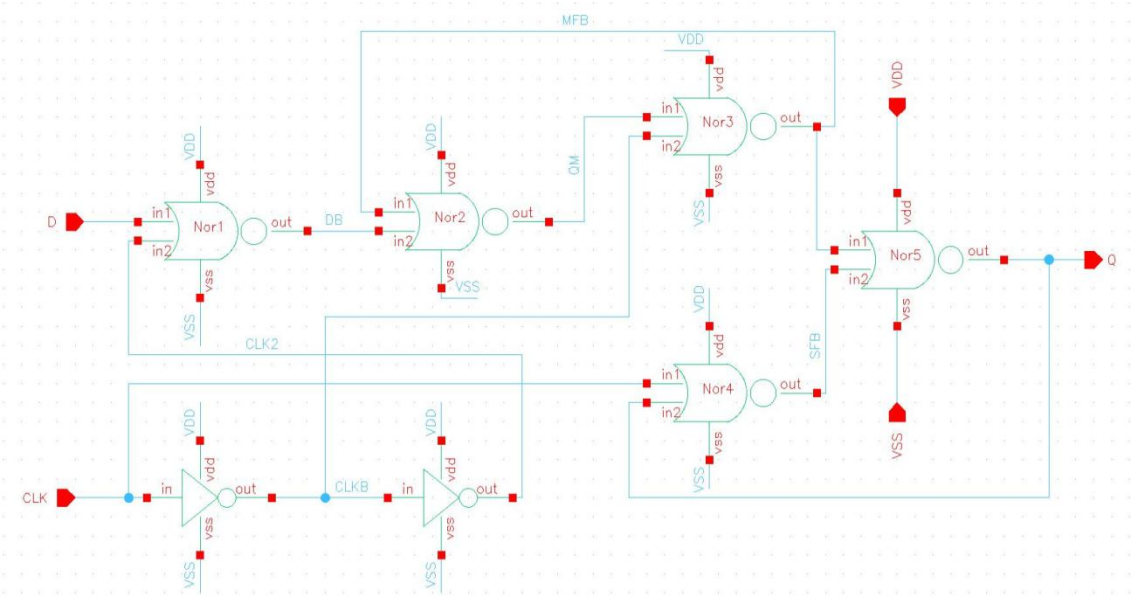

Fig.1. Schematic diagram of our proposed Improved Very Low-Power Static Flip-Flop (IVLPSFF)

A. NOR Gate

NOR gate belongs to logic family. It is the universal gate. The digital NOR logic gate which performs logical NOR operation Y= ~ (A+B). Whenever the both inputs are low, then the output will be high, for remaining input conditions the output will be low. With NOR gate we can design any logic gate, the operation of NOR gate is exactly negation of OR operator. The static NOR is designed with the combination of PMOS and NMOS, which is known as CMOS. The transistor size in the NOR is $L_{P=}$ 0.045, W_P = 0.24, $L_{N=}$ 0.045, W_N = 0.12 µm, respectively.

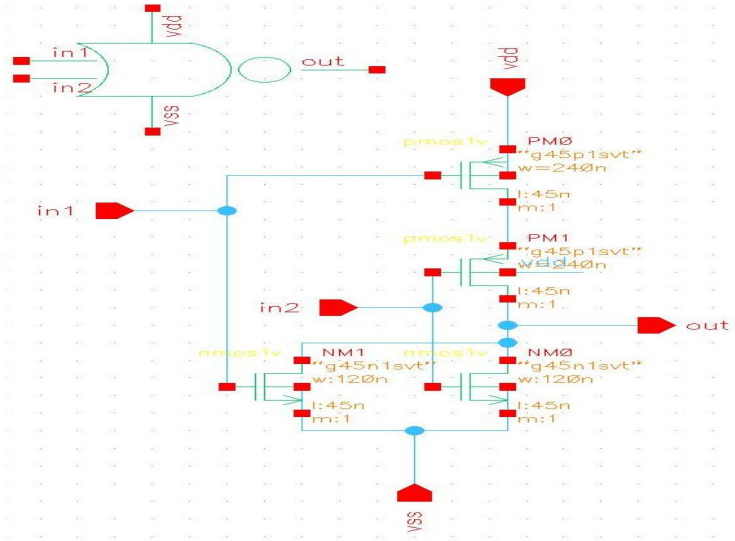

Fig.2NOR Schematic of IVLPSFF

B. NOT Gate

NOT gate belongs to logic family. It is called INVERTER. The digital NOT logic gate which performs logical NOT operation Y= ~A. whatever the input may be the output will be exactly negative of input. With the help of two INVERTER connections in a series

can form a buffer. In the conversion of NOR logic to OR and NAND logic to AND we need NOT gate. The static NOT gate is designed with the combination of PMOS and NMOS, which is known as CMOS. The transistor size in the NOT is $L_P = 0.045$, $W_P = 0.24$, $L_N = 0.045$, $W_N = 0.12$ µm, respectively.

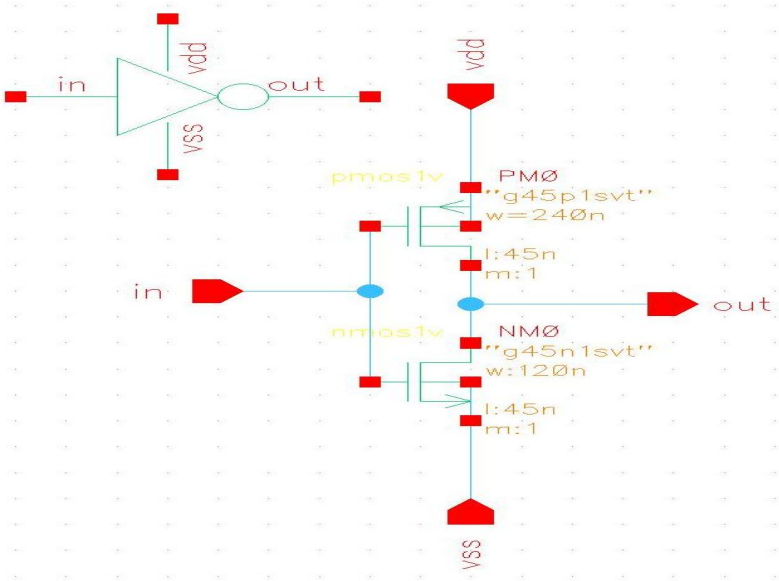

Fig.3 NOT Schematic of IVLPSFF

Fig.4 Timing Diagram of IVLPSFF

C. Full Custom Layout

Full custom Layout of Improved Very Low-Power Static Flip-Flop (IVLPSFF) as shown in fig.5, full custom designs are done by drawing stick diagram of a schematic and choosing the technology. For particular technology there are set of rules. Likewise for

45nm there are different rules when compared to different technologies, which means every technology is unique. Full custom design is very difficult. Why because, manually task should be done by us by taking the layers, placing of cells and routing of metals while designing the full custom layout. After designing of layout we need to do physical verification (Assura) for the layout. In verification part first we check for the Design Rule Check (DRC) violations and next Layout versus Schematic (LVS).

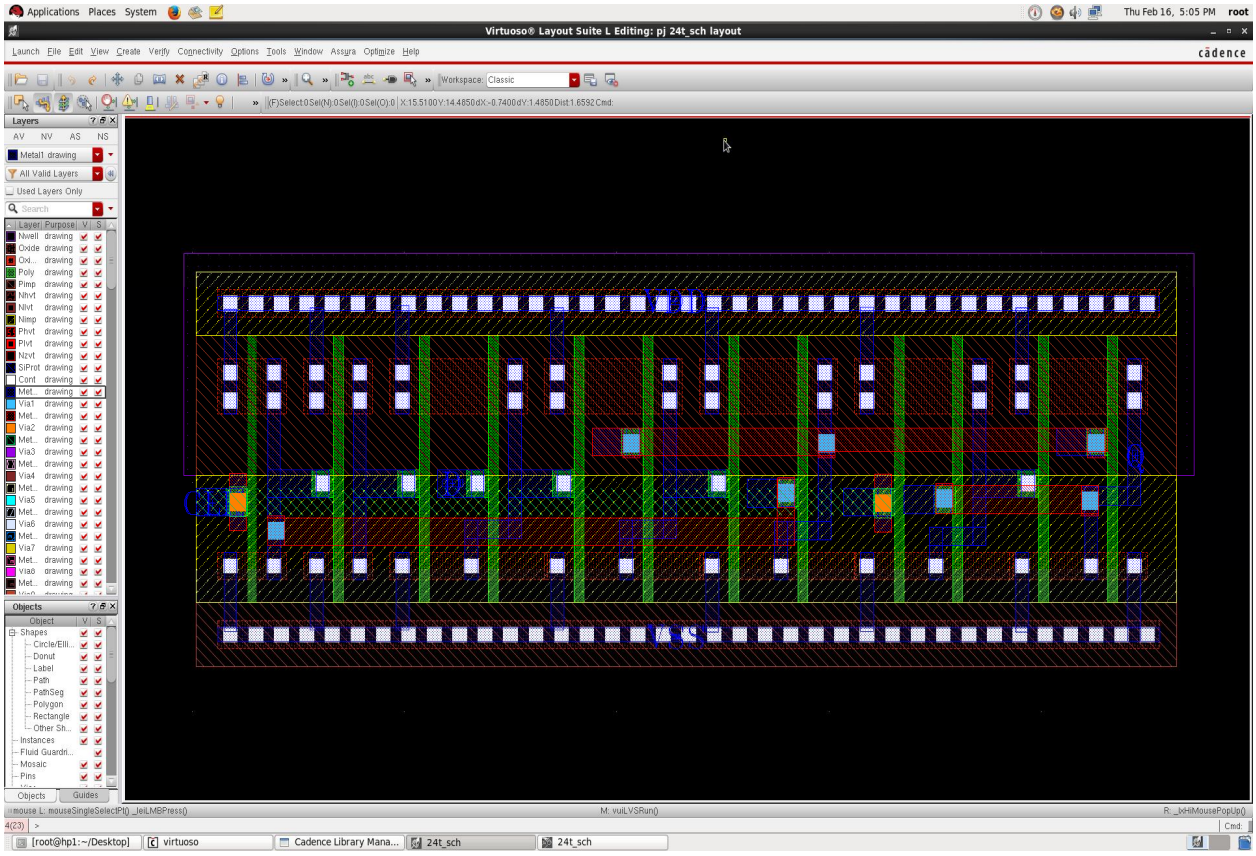

Fig.5 Full custom Layout of IVLPSFF

D. Simulation Result

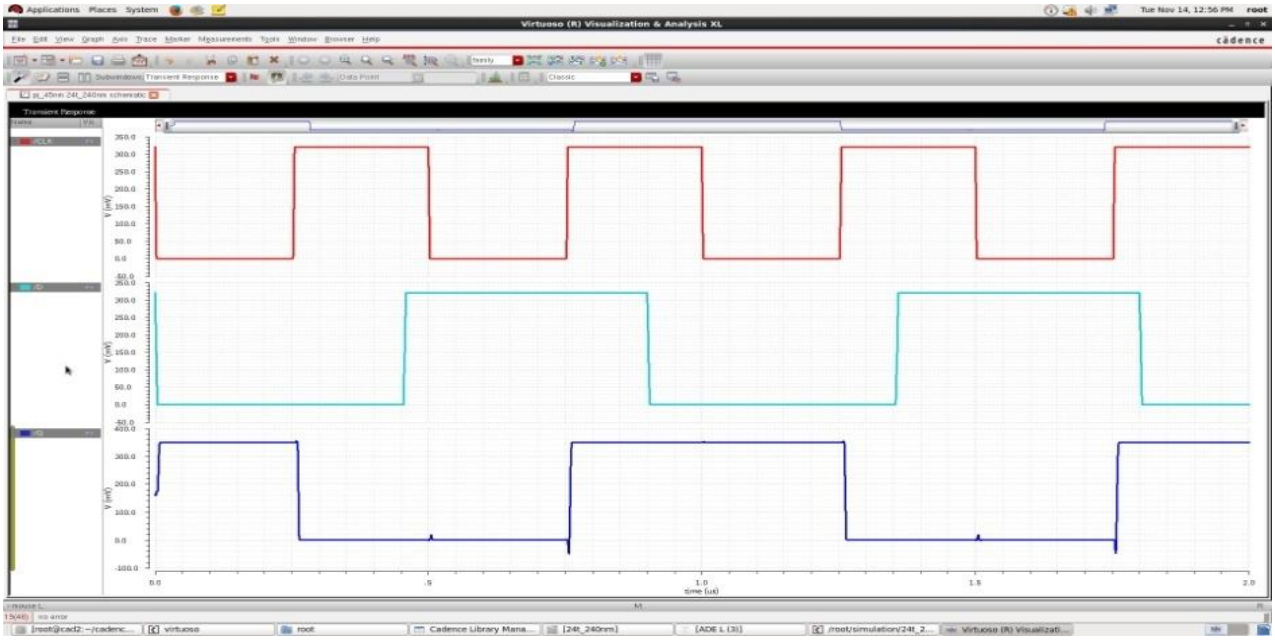

Fig.6 Simulated Waveform of IVLPSFF

Figure.7 illustrates the power dissipation of the IVLPSFF as a function of VDD 0.35V. Our proposed technique power by 0.9154nW.

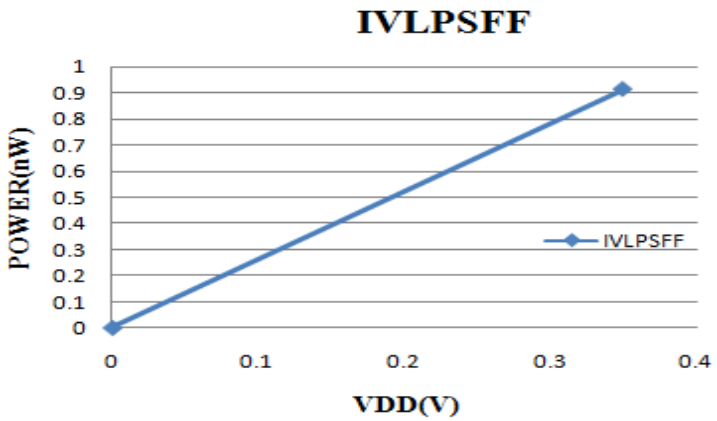

Fig.7 Power Dissipation of Flip Flop as a function of VDD

Figure 8 depicts the clock to Q delay of the IVLPSFFas function of VDD 0.35V.Our proposed technique delay by 1.55 ns.

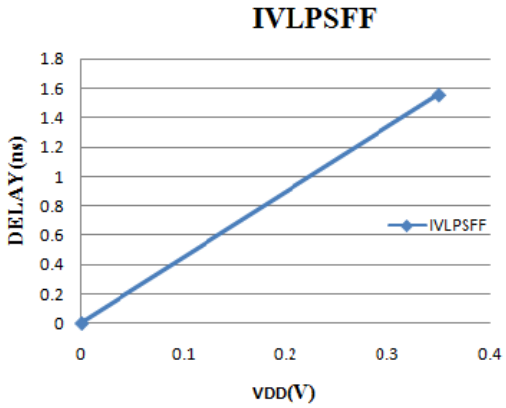

Fig.8 Delay of Flip Flop as a function of VDD

The function of the flip flop can be explained based on the parameters such as Frequency, PMOS Width, NMOS Width, Power, Delay and Area. The operating frequency of IVLPSFF was good when compared to other methods at 0.35V. This is illustrated in table 1.

TABLE I
PERFORMANCE COMPARISON AT 0.35V

FF	Frequency (MHz)	PMOS Width (µm)	NMOS Width(µm)	Power (nW)	Delay (ns)	Area (µm)
IVLPSFF	1.11-2	0.24	0.12	0.91	1.55	8.568
IVLPSFF	1.11-2	0.12	0.12	0.65	2.9	7.996

Table 2 shows the 180, 130, 90 and 45nm technology results of IVLPSFF along with CSSFF and ECSSFF.

TABLE 2
PERFORMANCE COMPARISON AT VARIOUS NANO METRE TECHNOLOGIES

FF	PMOS Width (µm)	NMOS Width (µm)	Frequency (MHz)	Voltage (V)	Power (nW)	Delay (ns)	Area(µm)
CSSFF (180nm)	1.37	1	1	0.347	6.61	586	50.5
			1	0.5	15.4	17.4	
ECSSFF (130nm)	1.37	1	1	0.347	12.1	4.957	-
ECSSFF (90nm)	0.12	0.12	2	0.5	5.253	254.4	-
IVLPSFF (45nm)	0.24	0.12	1.11-2	0.35	0.9154	1.558	8.568

V. CONCLUSION

Cadence simulation results for 45nm technology. Our proposed IVLPSFF achieved power- dissipation of 0.9154 nW and clock to Q delay of 1.55 ns at 0.35-V and 1.11-2.0 MHz clock frequency. For the proposed design the layout area is 8.568µm which is very narrow as compared to other methods. This project can also be implemented in FIN-FET to optimize power, delay and area.

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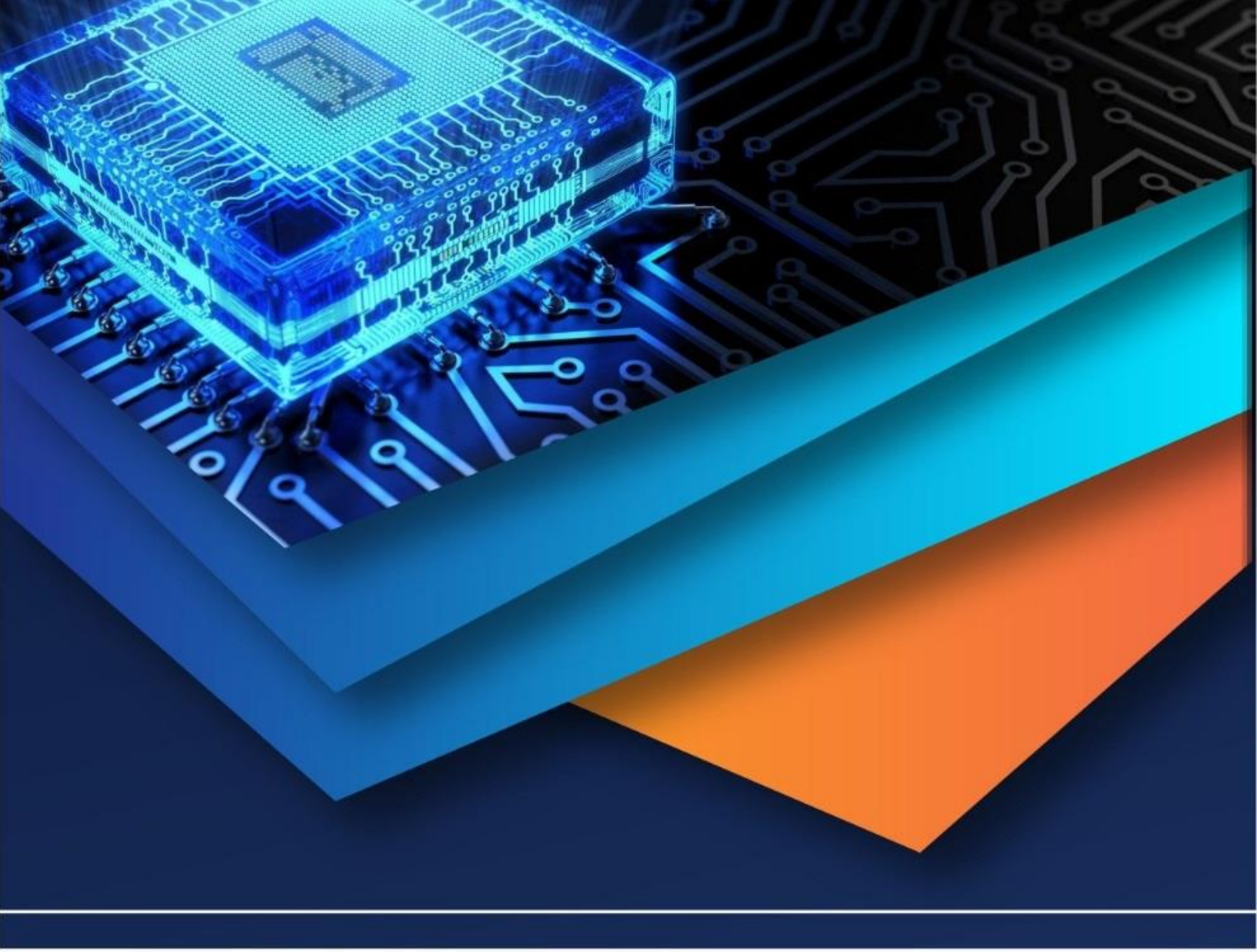

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