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Literature Review and Implementation of Multilevel Inverter by Using Capacitor for Solar PV Grid

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Abstract: The purpose of this paper gives a literature study about multilevel inverter topologies and to investigate the properties of these topologies. Especially the voltage balancing problem that is common with multilevel inverter will be investigated and also the advantages and disadvantages of the multilevel inverters will be compared to two-level inverters .It also includes an evaluation and comparison of the different topologies and a simulation presentation where two MLI topologies have been tested in simulation to investigate voltage balancing solutions and to compare with a two-level inverter. The comparisons include generated THD's, harmonic components and losses.

Keywords: Multi level inverter topologies, two level inverter, THD, Harmonic components and losses.

I. INTRODUCTION

Solar panel have a number of solar cell, a solar cell is a semiconducting device that absorbs light radiation and converts it in to electrical energy, that electrical energy source is given to the input of multilevel inverter. The ability of the proposed topologies is to generate better output performance in terms of harmonic content prompted the development of multilevel topology to higher number of voltage levels using the similar principle of clamping the intermittent levels with diodes. Such multilevel structures are known as 'diode clamped multilevel inverters.

Block Diagram

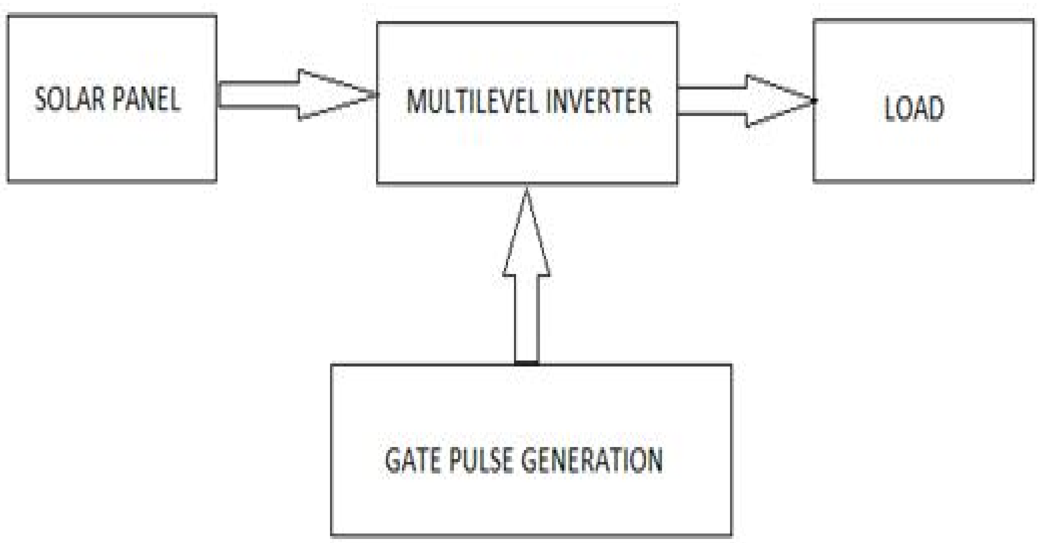

Fig-1:Block diagram of proposed system

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Volume 5 Issue XI November 2017- Available at www.ijraset.com

II. MULTILEVEL INVERTERS

Conventional two-level inverters, seen in Figure 1.1, are mostly used today to generate an AC voltage from a DC voltage. The two-level inverter can only create two different output voltages for the load, $V_{dc}/2$ or$-V_{dc}/2$ (when the inverter is fed with V_{dc}). To build up an AC output voltage these two voltages are usually switched with PWM, see Figure 1.2. Though this method is effective it creates harmonic distortions in the output voltage, EMI and high dv/dt (compared to multilevel inverters). This may not always be a problem but for some applications there may be a need for low distortion in the output voltage. The concept of Multilevel Inverters (MLI) does not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform, see Figure 1.3, with lower dv/dt and lower harmonic distortions. With more voltage levels in the inverter the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and a more complicated controller for the inverter is needed.

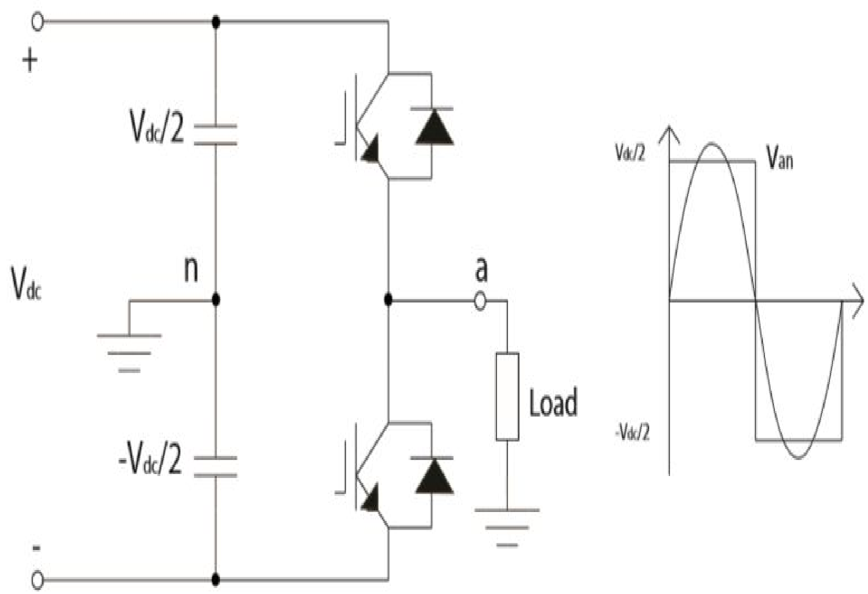

Figure 1.1: One phase leg of a two-level inverter and a two-level waveform without PWM

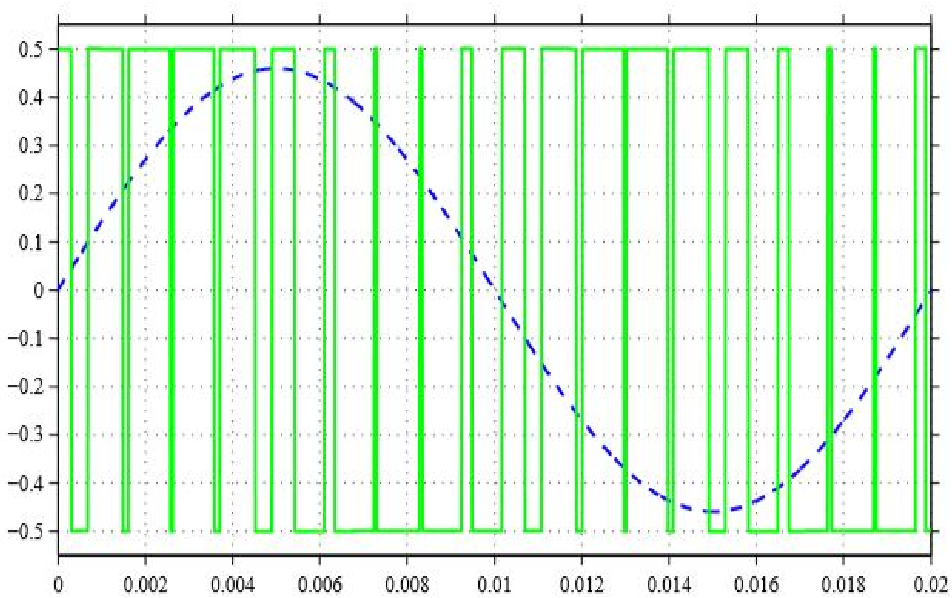

Figure 1.2: PWM voltage output, reference wave in dashed blue

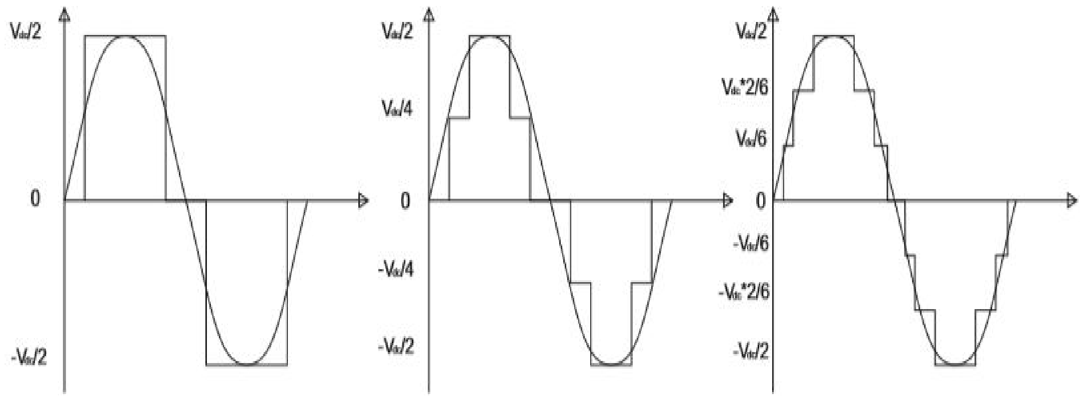

Figure 1.3: A three-level waveform, a five-level waveform and a seven-level multilevel waveform, switched at fundamental frequency

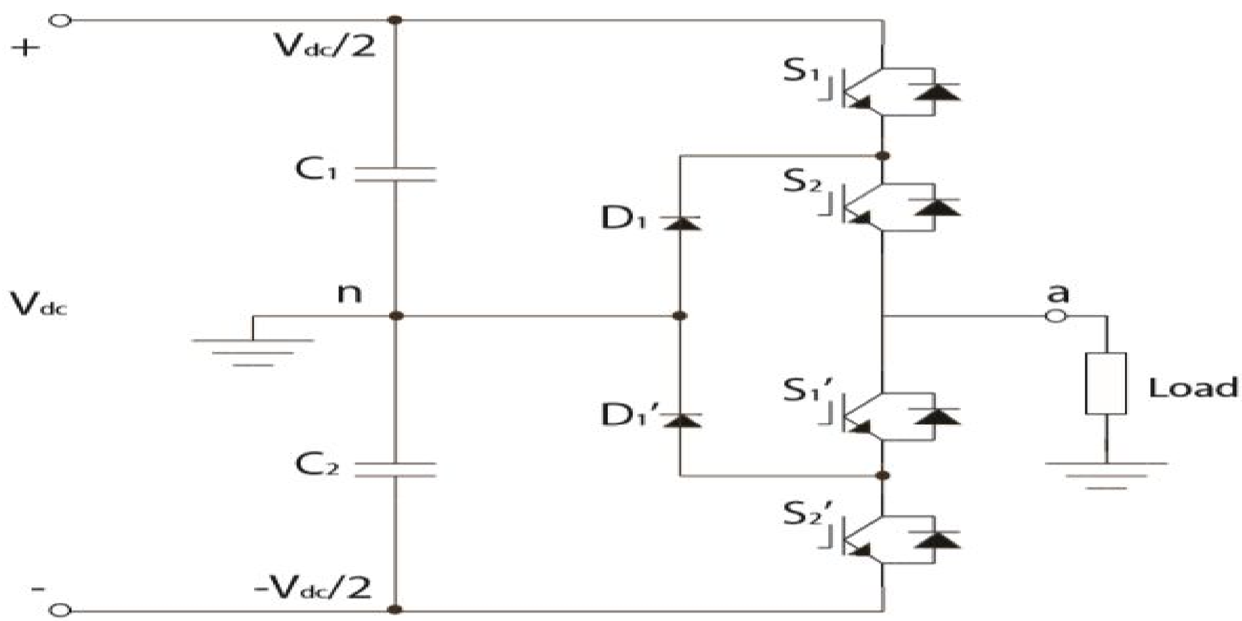

Figure 1.4: One phase leg of a three-level inverter

Midpoint in between two capacitors, marked n in the figure1.4. These capacitor build up the DC-bus, each capacitor is charged with the voltage $V_{dc}/2$. Together with another phase-leg an output line-to-line voltage with even more levels can be obtained. To create the zero voltage the two switches closest to the midpoint are switched on and the clamping diodes hold the voltage to zero with the neutral point. Now, if more valve pairs, clamping diodes and capacitors are added the inverter can generate even more voltage levels, see Figure 1.3, the result is a multilevel inverter with clamping diode topology. Some of the most attractive features in general for multilevel inverters are that they can generate output voltages with very low distortion and dv/dt, generate smaller common-mode voltage and operate with lower switching frequency compared to the more conventional two-level inverters. With a lower switching frequency the switching losses can be reduced and the lower dv/ dt comes from that the voltage steps are smaller, as can be seen in Figure 1.3 as the number of levels increase. There are also different kinds of topologies of multilevel inverters that can generate a stepped voltage waveform and that are suitable for different applications. The Multilevel inverter topologies that are investigated in this work are: Neutral Point Clamped Multilevel Inverter (NPCMLI), Capacitor Clamped Multilevel Inverter (CCMLI), Cascaded Multicell Inverter (CMCI), Generalized Multilevel Inverter (GMLI), Reversing Voltage Multilevel Inverter (RVMLI), Modular Multilevel Inverter (M2I) and Generalized Multilevel Current Source Inverter (GMCSI). The most dominant multilevel inverters use one or more voltage sources, as the three-level inverter, and most topologies presented in this report will have voltage sources, so called Voltage Source Inverters (VSI). There are however also multilevel inverters with current sources, Current Source Inverters (CSI), for example the GMCSI in the list above.

III. MULTILEVEL INVERTER TOPOLOGIES

A. Multilevel Diode Clamped/Neutral Point Inverter, NPCMLI

According to patents the first multilevel inverter (MLI) was designed in 1975 and it was a cascade inverter with diodes blocking the source. This inverter was later derived into the Diode Clamped Multilevel Inverter, also called Neutral-Point Clamped Inverter (NPC), see Figure 2.1. This topology is similar to three-level inverter in *Figure 1.4.* In the NPCMLI topology the use of voltage clamping diodes is essential. A common DC-bus is divided by an even number, depending on the number of voltage levels in the inverter, of bulk capacitors in series with a neutral point in the middle of the line, see the left part of *Figure 2.1.* From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to an m−1 number of valve pairs, where m is the number of voltage levels in the inverter (voltage levels it can generate). In *Figure 2.1* one phase-leg of a five-level NPC inverter is displayed. By adding two identical circuits the three phase-legs can together generate a three-phase signal where sharing of the DC-bus is possible. Due to more number of clamping diodes and for higher number of voltage levels the NPC topology will be impractical due to this fact. The reason for the inverter to have clamping diodes connected in series is so that all diodes can be of the same voltage rating and be able to block the right number of voltage levels. However, for low voltage application there is no need to connect components in series to withstand the voltage, since components with sufficient high voltage ratings are easy to find. With this configuration five levels of voltage can be generated between point a and the neutral point n; $V_{dc}/2$, $V_{dc}/4$, 0,$-V_{dc}/4$ and$-V_{dc}/2$, depending on which switches that are switched on. A waveform from one phase-leg of the inverter can also be seen in *Figure 2.1* in which the steps are clearly visible. For NPCMLI: s with a higher number of voltage levels the steppes will be smaller and the waveform more similar to a sinusoidal signal. Of course, with a higher number of voltage levels the complexity of the inverter increase and also, as earlier mentioned, more the number of components needed. To achieve the different voltage levels in the output a setup of switching state combinations are used. In *Table 2.1* the different states for the five-level NPC inverter are shown. Note that there is the possibility to only turn on (and off) every switch once per cycle, meaning that the inverter can generate a stepped sinusoidal waveform with a Fundamental

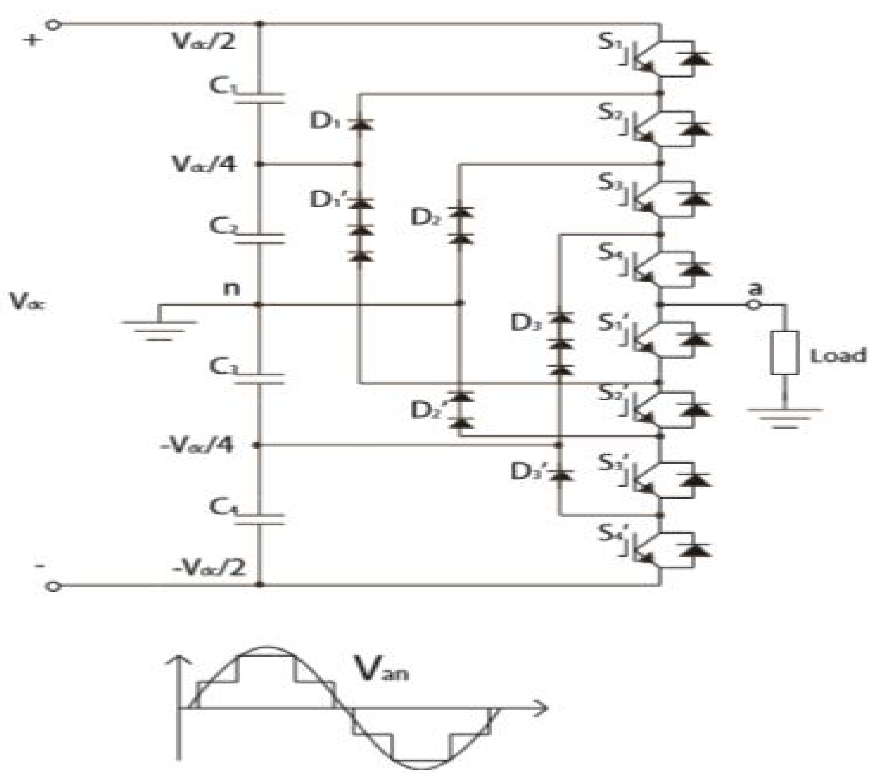

Figure 2.1: One phase-leg for a five-level NPC Inverter

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Switching frequency. From *Table 2.1* it can be seen that for the voltage $V_{dc}/2$ all the upper switches are turned on, connecting point a to the $V_{dc}/2$ potential, see Figure 2.2. For the output voltage $V_{dc}/4$ switches S2, S3, S4 and S0 1 are turned on and the voltage is held by the help of the surrounding clamping diodes D_1 and $D^{o}{}_{1}$. For voltage levels $-V_{dc}/4$ or $-V_{dc}/2$ clamping diodes D2 and $D^{1}{}_{2}$ or D3 and $D^{1}{}_{3}$ hold the voltage, respectively. For the voltages $\pm V_{dc}/2$ the current, when both voltage and current are positive (positive current goes out from the inverter), goes through the four top or bottom switches. For the other states positive current, while voltage is positive, goes through the Dx diodes and negative current through the $D^{1}{}_{x}$ diodes and also through the switches in between the clamping diodes and the load. For example, for state $V_{dc}/4$ positive current goes through diode D1 and switches S2, S3 and S4. In Figure 2.2 the turned on switches for every state are shown, switches in parallel to the thick dashed lines are on. In the figure the current paths are also shown, thin dashed lines, for every state and for both positive and negative current. For example for the $V_{dc}/2$ state the switches (positive current) or the diodes (negative current) are conducting and for the $V_{dc}/4$ state the current goes either through D1 and three switches (positive current) or D'_1 and through one switch (negative current). If there is a DC-source charging the DC-bus there are also currents following through the DC-bus to keep the DC-bus voltage constant. Table 3.1 also shows that some switches are on more frequently than others, mainly S4and S0 1, as long as a sinusoidal output wave that requires the use of all voltage levels is created. When the inverter is transferring active power this leads to unbalanced capacitors voltages since the capacitors are charged and discharged unequally, partly due to different workloads and that current is drawn from nodes between capacitors.

Output Voltage	S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-\frac{V_{dc}}{4}$	0	0	0	1	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

Table 2.1Switching states of one five-level phase leg. A '1' means turned on and "0"means turned off.

The total DC-bus voltage will be the same but the capacitors voltage will deviate from each other. While transferring real power current is drawn from, for example, capacitor C1 and C2 during different amount of time, as can be seen in the left part of Figure 2.2. The time intervals in the figure represent the discharge time and as can be seen C2 is discharged more, leading to unequal capacitor voltages. Also, during for example the $V_{dc}/2$ state current discharges both C1 and C2 but in the $V_{dc}/4$ state current is drawn from the point between C1 and C2, discharging C2 but charging C1. This makes the voltages over the capacitors to deviate in a special way. When only transferring reactive power however the NPCMLI does not have this voltage unbalancing problem, see right part of Figure 2.3. This is because of that time intervals during which the capacitors charged and discharged are equal during reactive power transfer, as the figure suggests. To solve the voltage balancing problem an additional balancing circuit can be added or more complex control methods can be implemented. Due to the complications of the capacitor voltage balance, the NPCMLI at higher number of voltage levels is unusual. When it comes to component quantities, such as number of needed components and their ratings, some things have to be considered that have been partially mentioned in the text above. As mentioned the inner switches are on more frequently than the outer switches since they are used in several of the switching states. Because of this a different amount of RMS current will flow through the switches depending on their position, with higher current rating needed for the inner switches. The positions of the clamping diodes are also important to their ratings since they need to block different levels of reverse voltage depending on where they are connected. If equal ratings are assumed for every individual diode, for every extra level of voltage that needs to be blocked and extra diode is required. This in turn explains why the NPC topology is unpractical with higher amounts of voltage levels since, because of the extra blocking diodes, the number of diodes grows quadratic ally with the level m following the equation $(m-1)*(m-2)$. This is however not valid for low voltage inverters, but since this report focuses on high and medium voltage application this is still the case. As for the other components $(m-1)$ DC-capacitors, $2(m-1)$ main diodes and $2(m-1)$ switches are needed for the NPCMLI topology. For three-phase inverter of the NPC type the DC-bus can be shared and only the mentioned $m-1$ DC-capacitors are needed but the requirements for all other components are multiplied by three.

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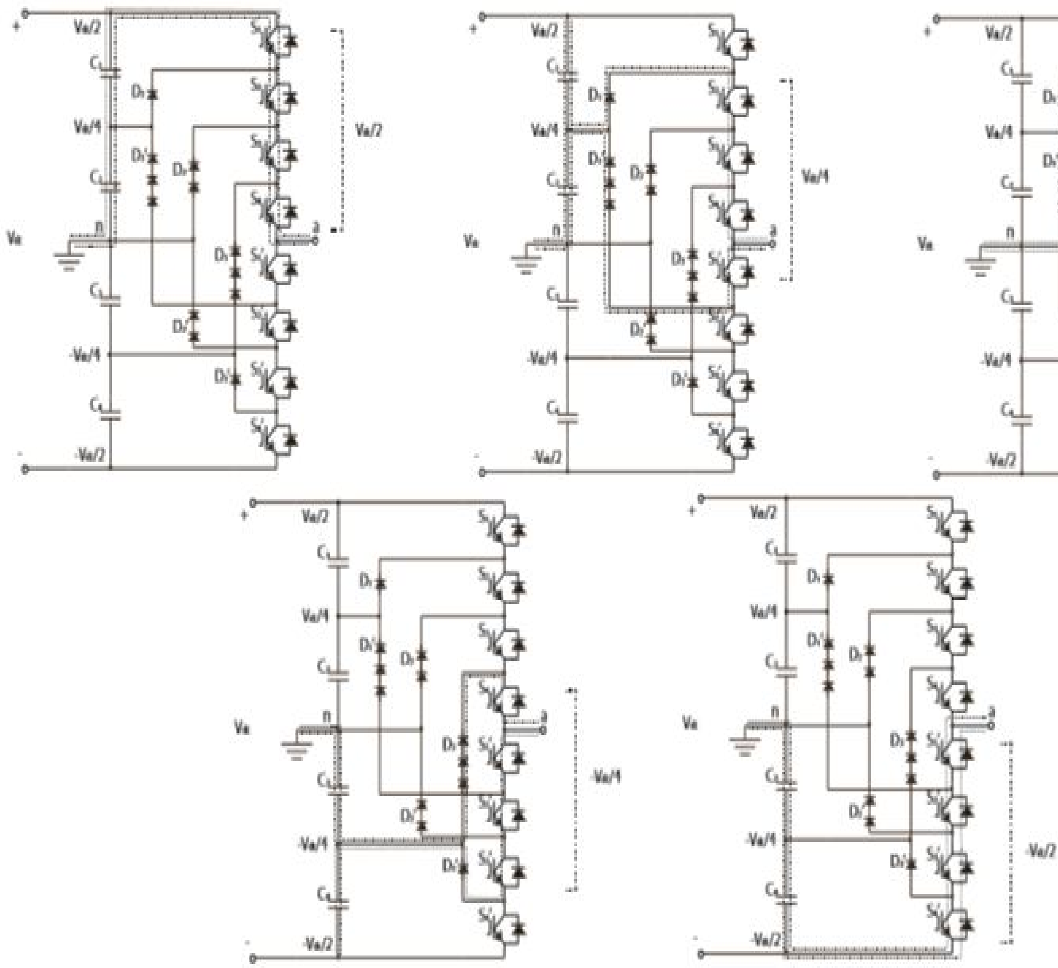

Figure 2.2: The thick dashed bar shows which switches that are on for every state. When both current and voltage is positive the current goes through these switches, otherwise through the diodes in parallel (depending on angle). Thin dashed line represent current path.C2,C1&C2 ,Capacitors charged Capacitors.

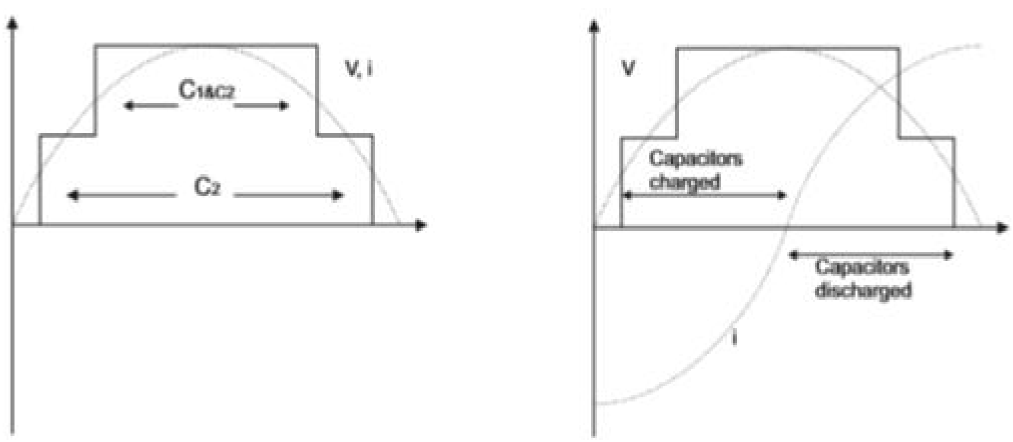

Figure 2.3: When voltage and current are in phase, to the left, capacitors are discharged unequally, but when the voltage and the current are 90 degrees out of phase, to the right, the charges is balanced.

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Volume 5 Issue XI November 2017- Available at www.ijraset.com

Pro's and Con's of NPCMLI

+ High efficiency since fundamental switching frequency can be used for all devices
+ Controllable reactive power low
+ Simple control method for back-to-back power transfer system
- High number of clamping diodes with high number of voltage levels
- Difficulties with active power low
- Capacitor Voltage Balance problem that need complex modulation

B. Capacitor Clamped Multilevel Inverter (CCMLI)

A similar topology to the NPCMLI topology is the Capacitor Clamped (CC), or Flying Capacitor, multilevel inverter topology, which can be seen in Figure 2.4. Instead of using clamping diodes it uses capacitors to hold the voltages to the desired values. The big difference is the use of clamping capacitors instead of clamping diodes, and since capacitors do not block reverse voltages the number of switching combinations increases.

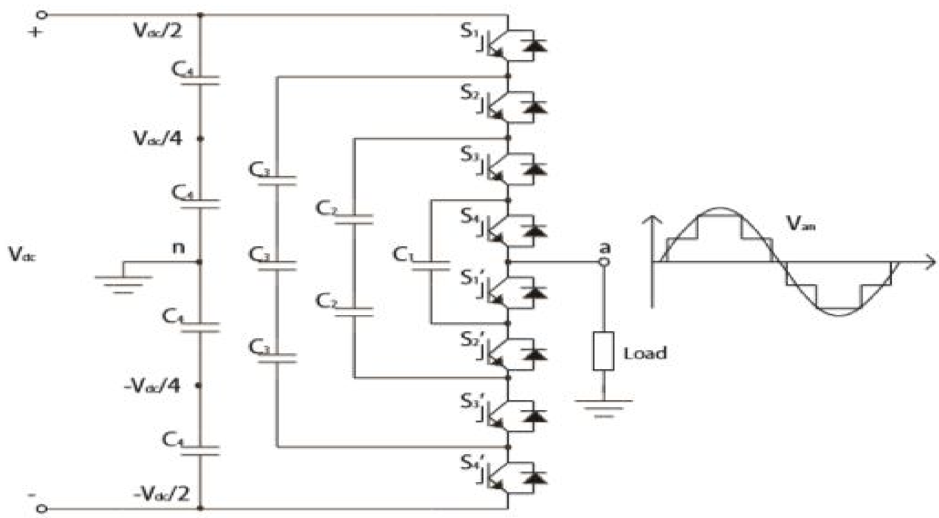

Fig: 2.4 Capacitor Clamped Multilevel Inverter with five voltage levels

Output Voltage	S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4
$\frac{V_{dc}}{2}$	1	1	1	1	0	0	0	0
$\frac{V_{dc}}{4}$	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
$-\frac{V_{dc}}{4}$	1	0	0	0	1	1	1	0
$-\frac{V_{dc}}{2}$	0	0	0	0	1	1	1	1

Table 2.2: Switching states for a five level Capacitor Clamped Inverter. A "1" means turned on and "0" means turned off.

Pro's and con's of CCMLI:

+ Capacitors can function as power storage during outage
+ Voltage balancing with redundant switching states
+ Can control both active and reactive power transfer
- Requires many capacitors

- Complicated control, leading to high switching frequency and losses, when transferring real power

Pro's and Con's of Cascaded Multicell Inverter (CMCI)

+ Requires a low number of components per level
+ Modularized structure without clamping components
+ Possibility to implement soft-switching
+ Simple voltage balancing modulation
- Needs separate isolated DC sources for real power transfer
- No common DCbus.

Generalized Multilevel Inverter (GMLI)The Generalized Multilevel Inverter (GMLI), seen in Figure 2.5, does however do not have the voltage balance problem since it is able to self-balance its own capacitors without the need for extra circuits. The NPCMLI, CCMLI and CMCI, among others, can also be derived from this generalized MLI topology.

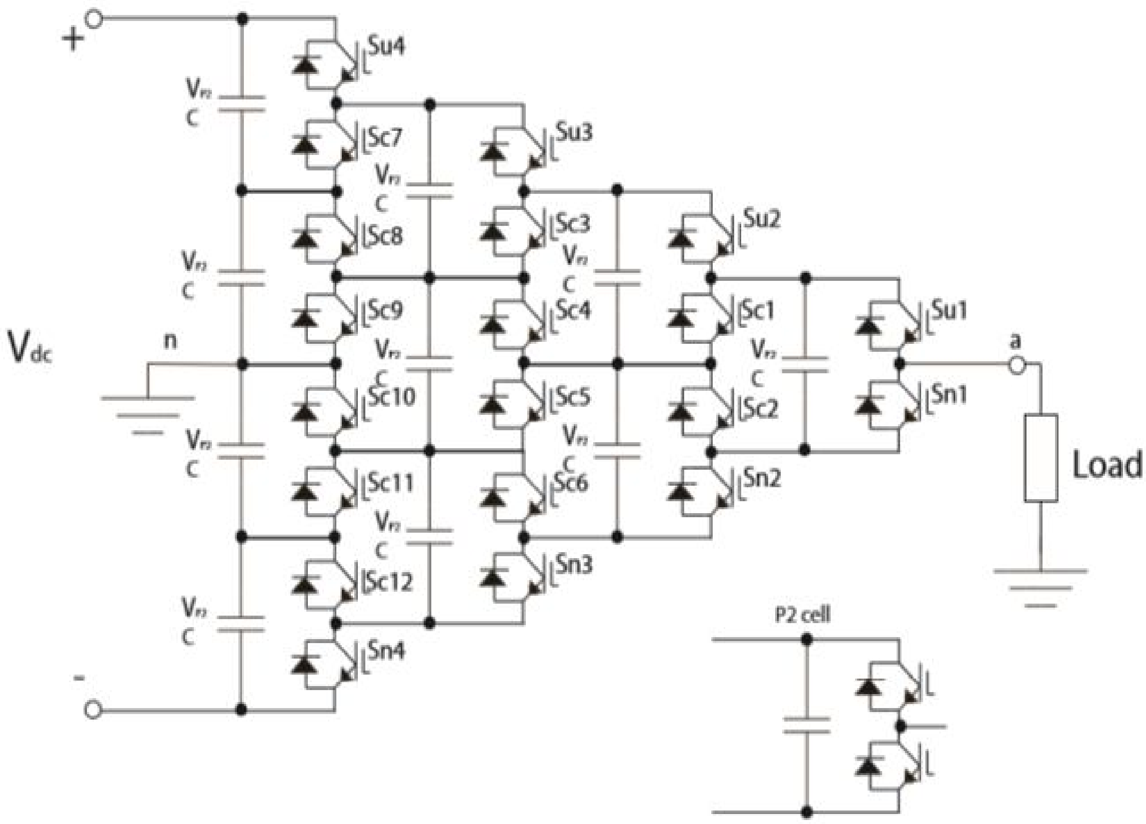

Figure 2.5: A five-level Generalized Multilevel Inverter

Pro's and Con's of GMLI:

+ True multilevel structure with auto voltage balancing
+ Able to eliminate need of transformer
+ Suitable for DC/DC applications
- Number of components required is not linear

Modular Multilevel inverter (M2I)

The Modular Multilevel Inverter (M2I), seen in Figure 2.6, is a newer topology first introduced in 2002. It uses a modularized setup of sub modules, essentially half bridges, which are connected or bypassed to generate a certain output voltage level.

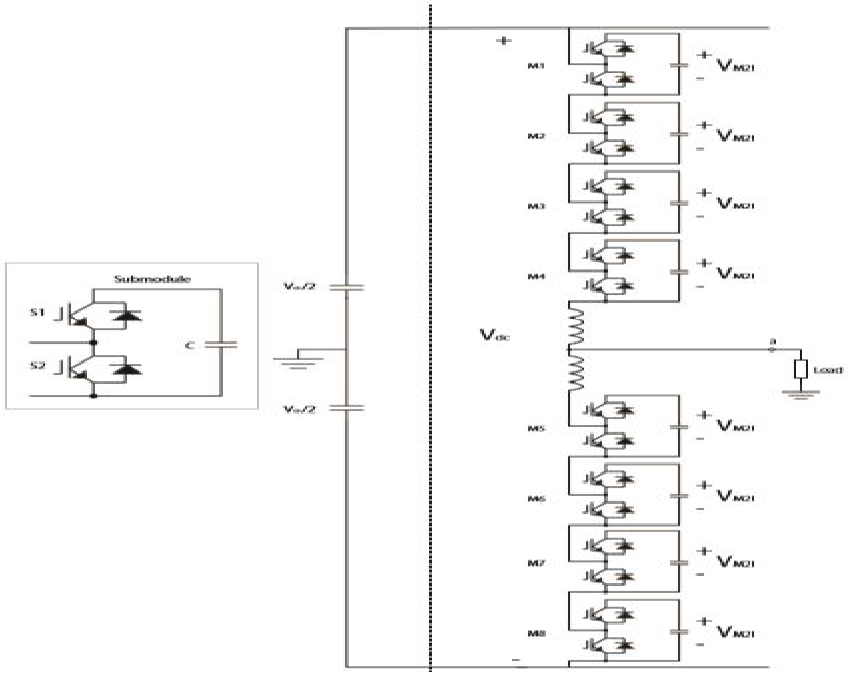

Figure 2.6: One phase-leg of a five-level Modular Multilevel Inverter

Pro's and Con's of M2I
+ Modular design
+ Low number of components
+ Simple voltage balancing
- Many DC-capacitors

IV. SIMULATION RESULTS

A. BlockDiagram

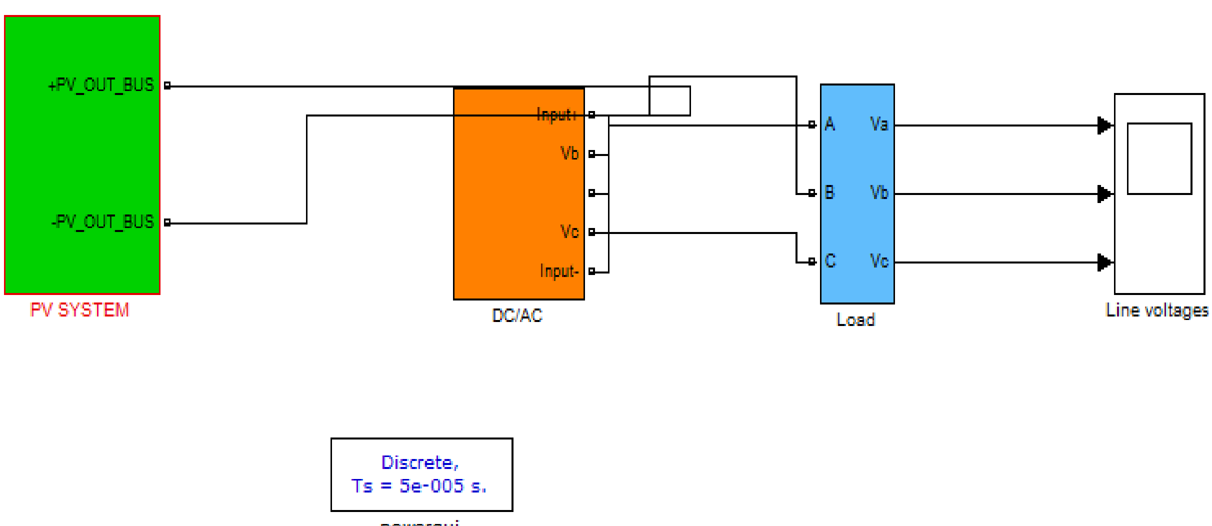

Fig:4.1 Block diagram

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Volume 5 Issue XI November 2017- Available at www.ijraset.com

B. Circuit Diagram

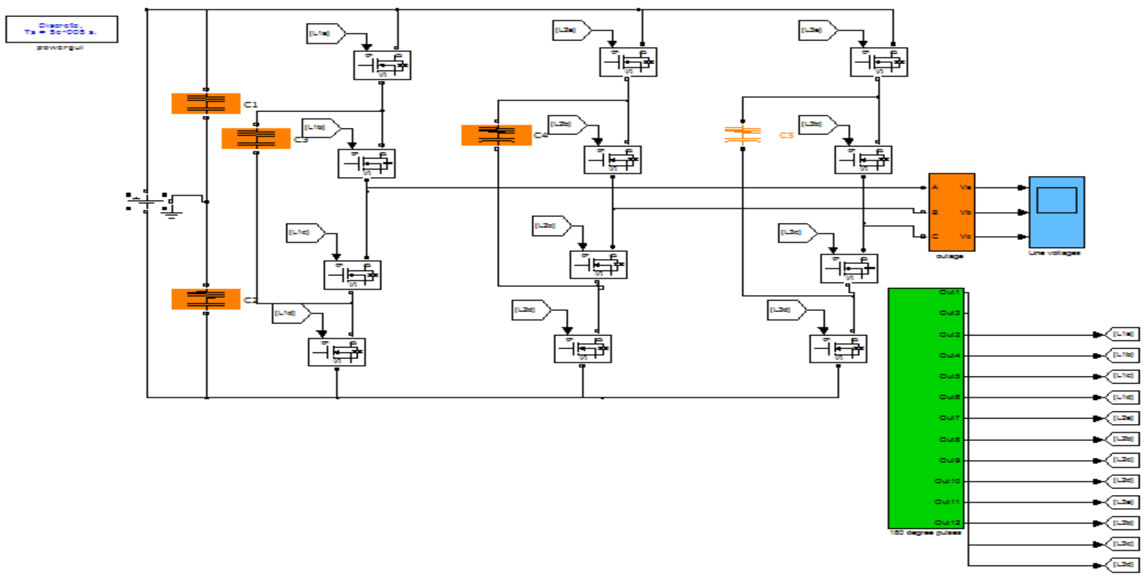

Fig:4.2The block diagram of multilevel inverter by using capacitor for solarpv grid

In this multilevel inverter the input is normally using PV cell (grid) and fuel cell (grid) .Any one of the grid is connected to the converter to boost up the dc source. DC/DC, AC/DC and AC/DC conversion is required for several applications such as HVDC-transmission application and back-to-back configurations for asynchronous grid connection; The DC is connected to the inverter to convert the DC in to AC source. The AC (inverter) source is connected to the load. In this below circuit capacitor is connected at the input side capacitors for input smoothing circuits used on commercial voltages (100 VAC,200 VAC) and commercial frequencies (60 Hz,50 Hz) must have a high withstand voltage and a ripple current resistance complying with twice the commercial frequency.

C. Control Signals

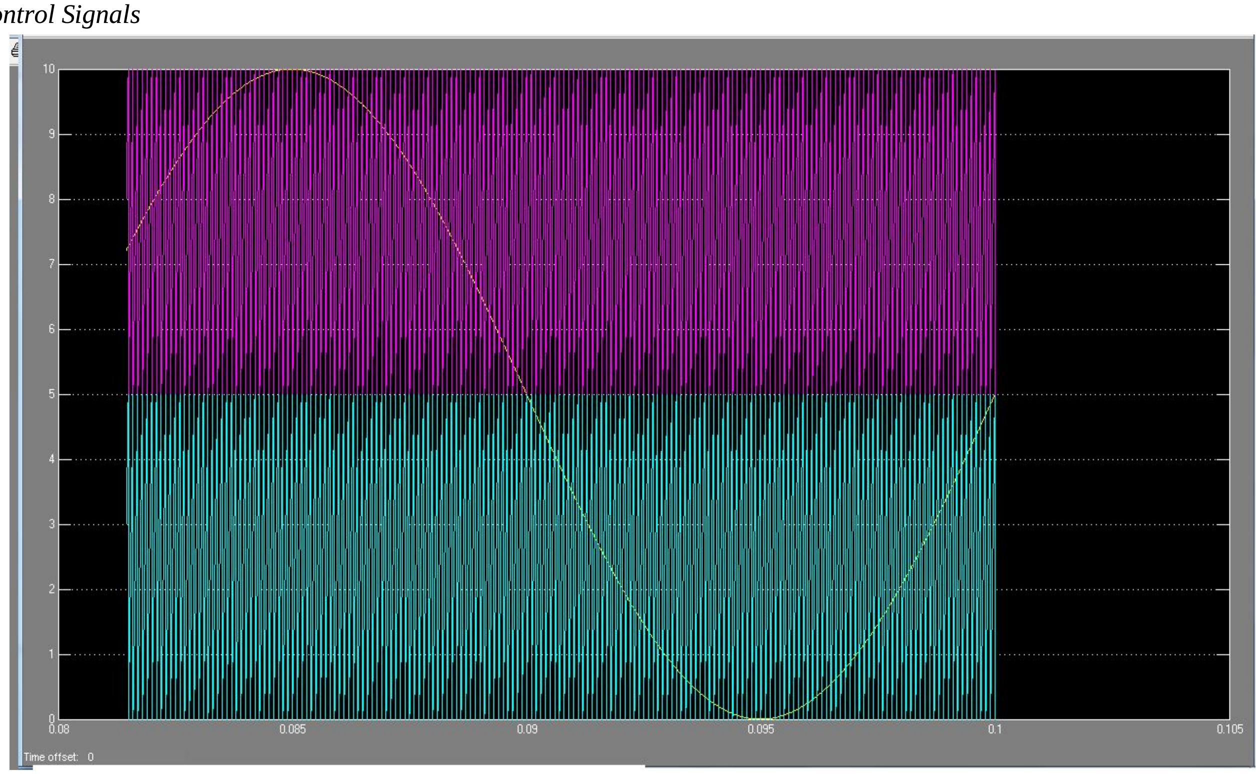

Fig:4.3.Single phase voltage waveform

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Volume 5 Issue XI November 2017- Available at www.ijraset.com

The below diagram is three-phase waveform

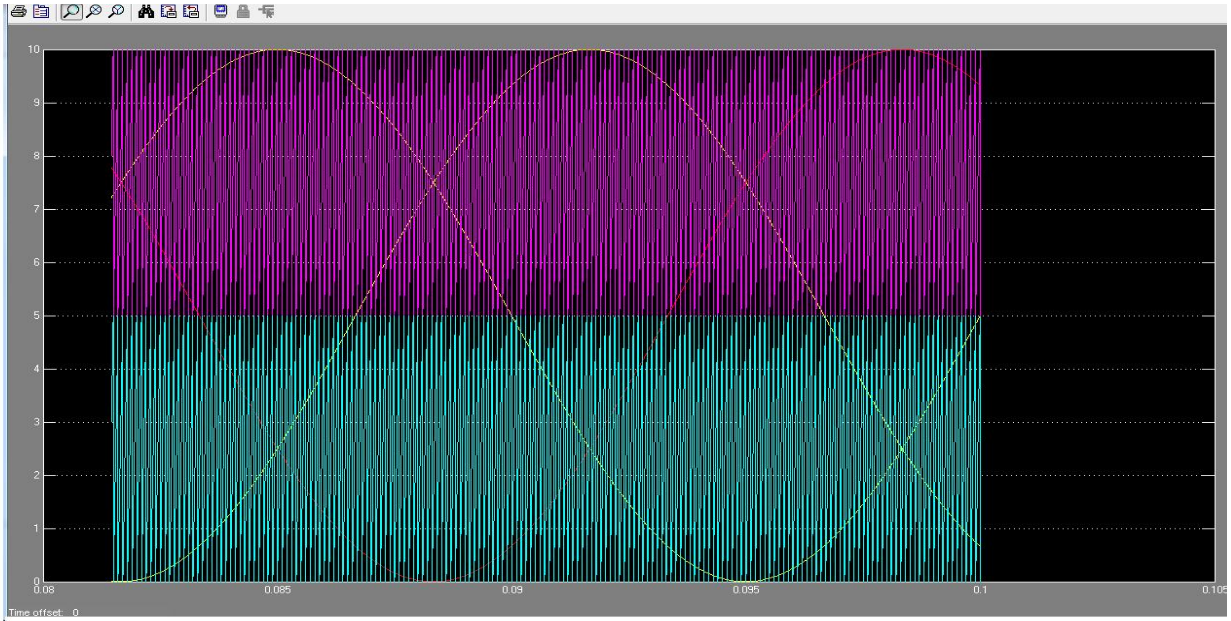
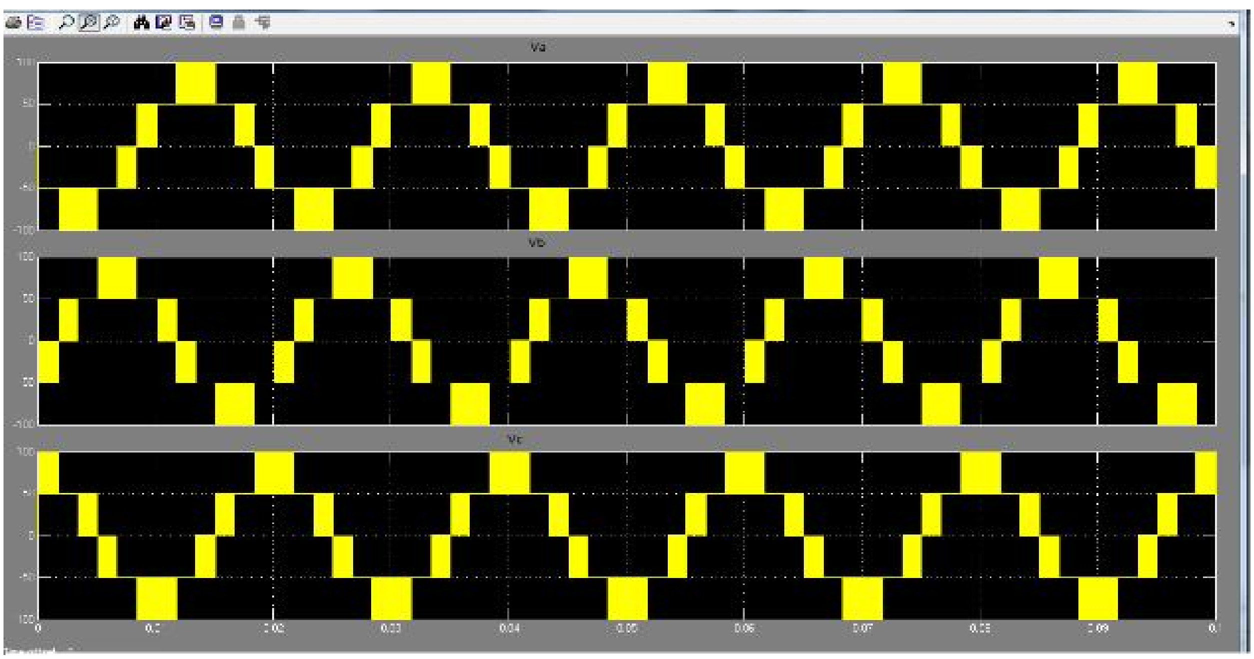


Fig: 4.4.Output Waveform

By using simulation the above diagram is appears at the output side.
The below diagram is 3-phase output waveform at the load side.



The simulation of output waveform are $V_{ab,}V_{bc}$, $V_{ca,}$ are at the load side.

V.CONCLUSION

This paper presented several topologies for multilevel inverters (MLI) with its pro’s and con’s some of them are well known with applications in the market. This paper shows that multilevel inverters compete with two-level inverters in the area of voltage ratings for their components (diodes, switches and such), even though the number of components needed for multilevel inverters, as shown, are very high. For a five-level MLI case the voltage rating requirements is only one fourth of that of the two level inverter but four times more switches are needed (for components with deferent ratings).

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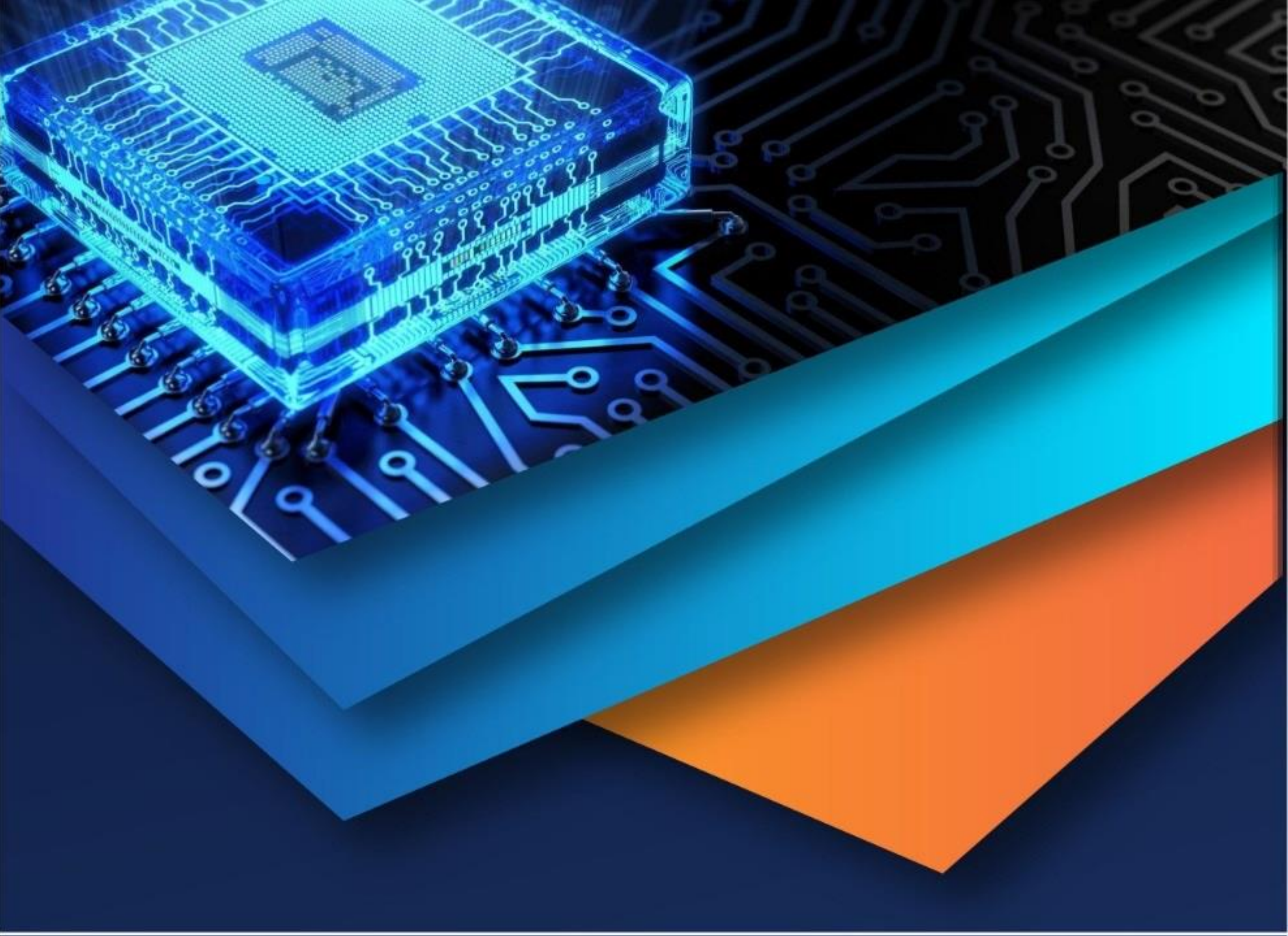

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