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Design of 3T Gain Cell for Ultra Low Power Applications

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Abstract: ***Design of a power efficient SRAM cell is one of the most important factor in order to achieve better chip performance. This paper presents a stable SRAM Gain Cell for low power applications. The 6T SRAM has been the traditional choice for the implementation of embedded memories due to its high-access speed and refresh-free static data retention. However, the 6T bit cell has several drawbacks in modern systems, which includes its large transistor count. In order to provide full CMOS logic compatibility a gain-cell (GC)-embedded DRAM (eDRAM) consisting of 3-transistor (3T), GC-eDRAMs which provides a reduced silicon footprint, along with inherent two-port functionality, nonratioed circuit operation, and very low static leakage currents from VDD to GND. With the benefit of read and write access, we modify the 8-TSRAM cell as 3-T SRAM cell with transmission gate that reduces the read and write time access with comparatively low power and eliminating the usage of signal booster. In this paper we designed the 3T GC cell by using MICROWIND/DSCH 180 nm technology and simulation results obtained by using HSPICE 180 nm technology.***

Key Words: Low power, Gain cell (GC), 3T (3 Transistor), SRAM,

I. INTRODUCTION

Today world aims in designing low power devices due to the rampant usage of portable battery powered gadgets. Scaling of MOS technology creates new challenges to the SRAM circuit design, mainly leakage power and stability. SRAM design furnishes an approach towards reduces the hold power dissipation devices due to the uncontrolled usage of portable battery powered gadgets. . The proposed cell has similar structure to conventional 6T SRAM cell with the addition of two buffer transistors, one tail transistor and one complementary word line. Dueto stacking effect, the proposed cell achieves lower power dissipation. In this paper, impact of process parameters variations on various design metrics of the proposed cell are presented and compared with conventional differential 6T (D6T),transmission gate based 8T (TG8T) and single ended 8T (SE8T) SRAM cells. Impact of process variation, like threshold voltage and length, on different design metrics of an SRAM cell like, read static noise margin (RSNM), read access time(TRA) and write access time (TWA) are also presented. In deep submicron technology, system-on-chip (SoC) products requires a high speed memory to support increased storage capability. Furthermore static random access memory (SRAM) is widely used for SoC products. Static Random Access Memories (SRAMS) would utilized Likewise cache memory which need aid inserted to microprocessor, System-on-Chip (SoC), Network-on-Chip (NoC) modules. This will be because of those certainty that they would quick contrasted with eDRAM (such Likewise DRAM) Furthermore primary memory (DRAM) [1].They need to be created on the same die of a processor. Concerning illustrations expressed by ITRS, 90% of the processor's chip region is possessed by SRAM [2].increase in processor's speed has risen in recent years, whereas memory speed not got such an extensive increase. Thus, a variation between performing ability of memory and processor may be extending for the long haul. To decrease that gap, silicon industry is embedding memory on chip which is used for cache memory. In order to get faster cache memory, SRAM cell should be quicker. For getting the speed, threshold voltage of MOSFETs should be reduced. However, there is a limitation up to which threshold voltage could be reduced. SRAM cells are used in Emerging applications like implanted medical instruments and bioelectronics which demand for power efficient SRAM. Moreover, noise margin will be crucial parameter at the time for read operation over the hold operation. SNM is influenced by technology and supply voltage scaling [3]. Thus, a SRAM cell is required to be speed and also disturb-free throughout the read operation. Several techniques were proposed to reduce the power consumption of SRAMs. the read power is reduced by limiting the swing voltages of bit lines and data bus to small voltages during read operation. However SRAM cell requires more power during write cycles than read cycles [4]. Since in many processors caches occupy about 50% of the die area, the leakage power of caches is one of the major sources of power consumption in high performance microprocessors. Although many techniques have been proposed to address the problem of low-leakage SRAM design, most of the methods address only standby leakage power consumption. In traditional 6T-SRAM, cells must be stable during read as well as write events. Ignoring redundancy, such functionality should be preserved for each cell under worst-case variation.

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Concessions should be made in power and performance to achieve required output. While at the basic cell level, transistor strength ratios must be chosen to meet cell static noise margin and write margin are to be maintained, which represents constraints on the transistor strengths [6].Eventually by lowering the supply voltage (VDD), dynamic power decreases quadratic ally and first order leakage power reduces linearly [10]. Hence, by operating the cell in sub threshold region (i.e. by lowering the supply voltage below threshold voltage), it is made to achieve low power SRAM cell [11]-[14].

II. PREVIOUS WORKS

A. Existing Method

A low-power 8T SRAM cell (LP8T) is shown in (see Fig. 1). In order to achieve improved performance and density, device scaling is done. The cell is very similar to the conventional 6T, except the two extra buffer transistors (MN5/6), one tail-transistor (MN7) and one complementary word line (WWLB). The proposed architecture is shown in Fig. 2. During read operation one of the buffer transistor (gate of which is connected to node, storing '1') conducts. Because of these buffer transistors, read stability is improved. Because of tail transistor and WWLB, hold power consumption is minimized. Transistor sizing is an important factor for an SRAM cell. In conventional differential 6T SRAM (D6T) (see Fig. 3) cell, improvement in RSNM (read staticnoise margin) can only be achieved at the cost of degradation of WSNM (write static noise margin) and vice versa.

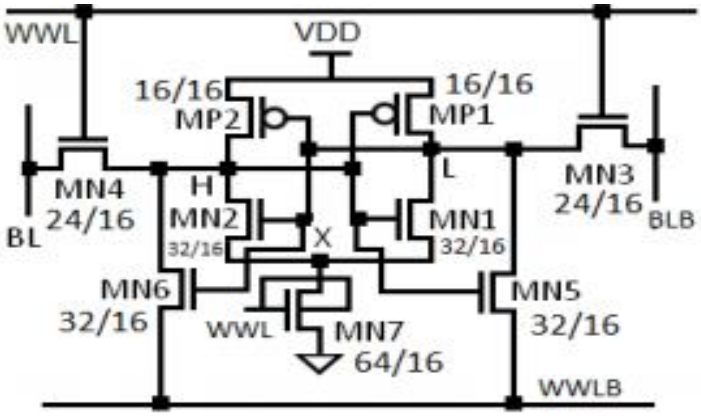

Fig. 1. Low power consuming 8T SRAM cell (LP8T).

1) Read Operation: The read operation is performed by precharging the bit-lines (BL and BLB) to VDD, then raising WWL to VDD and lowering WWLB to GND. Transistor MN7 is turned ON (as WWL is high) during read operation. Depending upon the content of the storage nodes (H/L), one of the buffer transistors (MN5/6) conducts. BLB/BL discharges through access transistors (MN3/4), followed by two paths, one through buffer transistor (MN5/6) and WWLB, other through pull-down transistor (MN1/2) and tail-transistor MN7. This results in faster read operation. For instance, if storage node H stores logic '1', pull-down transistor MN1 and buffer transistor MN5 conduct. Therefore, BLB finds two paths to discharge. One through MN3/1/7 and other through MN3/5/WWLB, while BL is held at VDD as MN6 and MN2 are OFF (due to logic '0' stored at node L) (see Fig. 2).

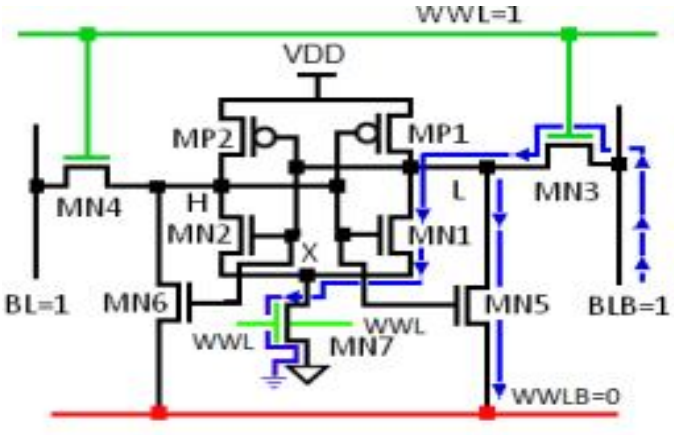

Fig. 2. Read Operation of the LP8T SRAM cell.

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2) *Write Operation:* During write operation WWL is raised to VDD. Therefore, the complementary of WWL (i.e. WWLB) is pulled down. Because of high WWL, both the access transistors (MN3/4) are ON. Transistor MN7 is kept ON (as WWL is high). Let's assume initially storage node H stores logic '1' and L stores logic '0'. Now to write '1' at L and '0' at H, BLB and BL are loaded with '1' and '0' respectively by write driver (not shown). Storage node H discharges through MN4 by BL. Simultaneously, voltage at node L increases towards VDD through MN3 by BLB (see Fig. 3). Note that, for brief initial time node L discharges through MN1/7 to GND and MN5 by WWLB but for brief final time node H discharges through MN2/7 to GND and MN6 by WWLB. Therefore, the desired data is written successfully.

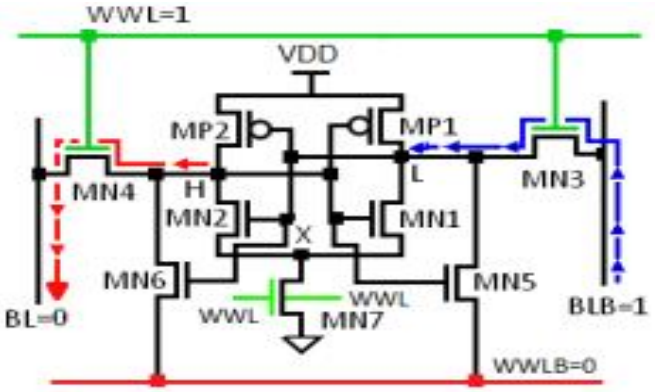

Fig.3. Write Operation of the 8T SRAM cell.

3) *Hold Operation :*The hold operation is performed by lowering WWL to GND (WWLB is at VDD). Thus, the access transistors MN3 and MN4 are OFF. Transistor MN7 is kept OFF during hold operation. The reason behind keeping WWLB at VDD and transistor MN7 OFF, are to achieve less leakage current. Leakage current increases on increasing the number of junctions due to extra cell transistors.

III. PROPOSED METHOD

In recent years, memories have occupied increasingly large portions of the die area of VLSI systems-on-chip (SoCs), in general, and of microprocessors, in particular, as shown in [1]. This is due to the large 6-transistor (6T) SRAM bitcell and its area-consuming peripheral circuitry that are the basis for the vast majority of these. In addition, the standby power of ultralow-power (ULP) systems, such as biomedical implants and wireless sensor networks, is often dominated by embedded memories, which continue to leak during the long retentive standby periods that characterize these systems. The 6T SRAM has been the traditional choice for the implementation of embedded memories due to its high-access speed and refresh-free static data retention. However, the 6T bit cell has several drawbacks in modern systems, including its large transistor count, its impeded functionality under voltage scaling, and the aforementioned static leakage currents from the supply voltage (VDD) to GND. One of the interesting alternative implementations that addresses these limitations, while continuing to provide full CMOS logic compatibility, is gain-cell (GC)-embedded DRAM (eDRAM), such as the circuit shown in Fig. 4(a) [2]–[5]. Most often consisting of 2-transistor (2T) or 3-transistor (3T), GC-eDRAMs provide reduced silicon footprint, along with inherent two-port functionality, nonratioed circuit operation, and very low static leakage currents from VDD to GND. However, as opposed to static memories, such as SRAM, the data retention of GC-eDRAM depends on dynamically stored charge, and thereby requires periodic, power-hungry refresh operations.

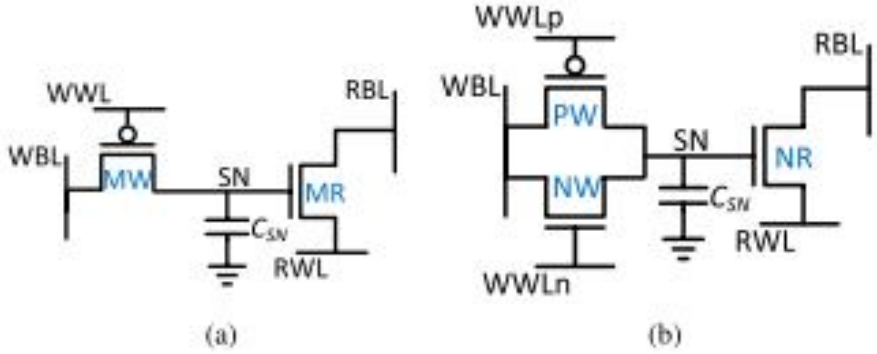

Fig.4. Schematic of conventional and proposed GCs. (a) 2T mixed GC. (b) Proposed 3T GC.

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A. Structure and design

Fig. 4(b) shows the schematic of the proposed single-supply 3T GC. The circuit comprises a write port featuring a complementary TG PMOS Write (PW) and NMOS Write (NW), a read port based on an nMOS device (NR), and a SN composed of the parasitic capacitance (CSN) of the three devices and the stacked metal interconnect. The cell is built exclusively from standard VT transistors and is fully compatible with standard digital CMOS technologies. The gates of PW and NW are connected to the complementary word lines, WWLp and WWLn. A common write bit line (WBL) is used to drive data through the TG during write operations. The full-swing passing capability of the TG enables the propagation of strong levels to the SN without the need for a boosted word line. Read is performed by recharging the read bit line (RBL) and subsequently driving the read word line to GND, thereby conditionally discharging the RBL capacitance if the SN is high (data 1) or blocking the discharge path if the SN is low (data 0). To achieve a reasonable tradeoff between speed, area, power, and reliability, a dynamic sense inverter is used on the readout path. However, other sense amplifiers can be used for improved read performance, such as demonstrated in [3], [8], and [9].

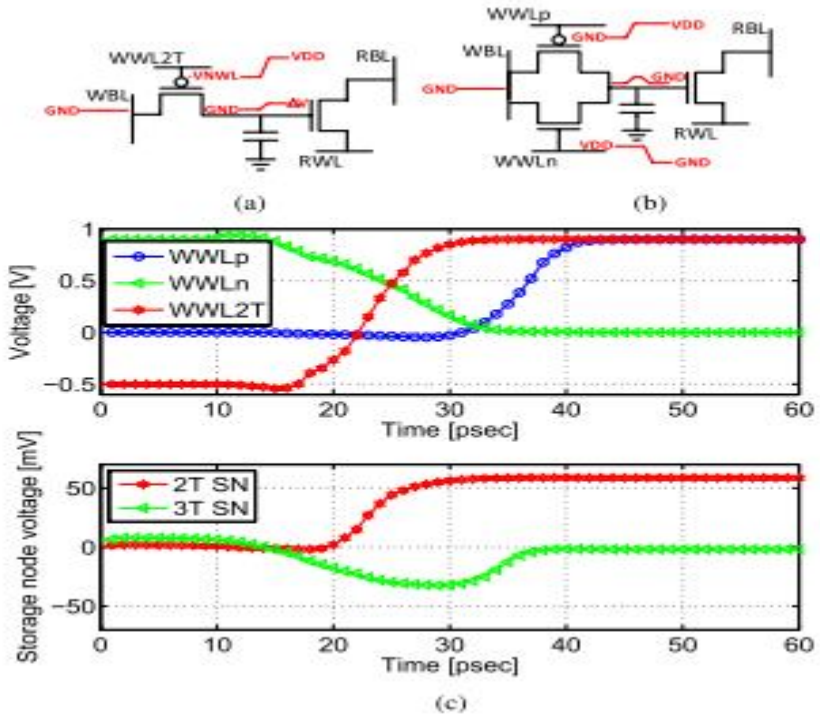

Fig. 5.Effects of CI and CF mechanisms. (a) Conventional 2T bit cell. (b) Proposed 3T bit cell. (c) Waveform comparison of the two bit cells during write operation

B. Readout circuitry

Many previous low-voltage embedded memories, targeted at ULP systems, employ a simple sense inverter in order to provide robust, low-area, and low-power data readout. However, such an inverter suffers from a very slow readout, as it requires the RBL to be discharged (charged for a pMOS read device) past the switching threshold of the inverter, which is hard to deviate away from VDD/2. This operation is further impeded by the aforementioned RBL saturation during readout that slows down the discharging (charging) operation, as the RBL voltage decreases (increases). Therefore, the readout path that was integrated into the proposed 3T GC-Edram macro cell has two sensing modes: 1) a faster, yet potentially more error-prone, dynamic readout mode and 2) a slightly slower, yet more reliable, static mode. In all measured prototype chips, both the dynamic (preferred for speed) and static modes were tested successfully. In both sensing modes, Low Threshold device (LVT) pMOS transistors were used in order to allow a faster yet accurate read-access time, due to the aforementioned issues. The supply voltage to the readout circuitry is gated with the read enable signal in order to save substantial static power due to the leaky LVT devices. The schematics of the two alternative readout circuits are shown in Fig. 4. The rising edge of the read clock creates a precharge pulse that charges the parasitic capacitance of RBL and discharges the output capacitance of the dynamic sense inverter (DOdyn) through the discharge transistor, Ndyn. Subsequently, RBL is conditionally discharged during the read operation, turning on Pdyn to flip the output if a 1 is stored in the

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selected cell. Therefore, an RBL swing of only one VT is required to complete a read operation. Transistor sizes for the dynamic sense inverter and pulse generator were chosen according to post layout simulations under global and local parametric variations.

C. Write circuitry

While the proposed single-supply 3T bit cell provides a significant improvement in both write time and initial SN level over standard GC implementations, the dual-transistor write port adds an additional leakage path to/from the SN. The increased aggregated sub-VT current causes faster degradation of the stored charge, leading to reduced DRT, as compared with a reference 2T cell. In addition, several previous works have shown that the data dependent, asymmetric DRT (for data 0 and 1) of standard GCs can be manipulated to overall enhance DRTs by biasing the WBL at the best case voltage for the weaker data level during standby and read operations [10]. For the proposed 3T configuration, the worst case DRTs of the 1 and 0 levels are similar, and significant deterioration of the stored levels occurs for both extreme values of WBL bias (VDD and GND). However, a neutral bias of VDD/2 can be applied, thereby greatly reducing the sub-VT current through the TG. Fig. 5 shows the benefit of this measure, displaying the level degradation of stored 1 and 0 data with WBL biases of opposite polarity and VDD/2. With a WBL bias of VDD/2, the DRT can be extended by ~1000×.The write circuitry to implement the median WBL bias during standby and read cycles is shown in Fig. 5(c). A standard inverter chain conditionally drives the data-in level on to the WBL through a TG, controlled by complementary write enable signals Write Enable (WE) and Write Enable Negative (WEN). In parallel, pair of long-channel I/O devices drive WBL during nonwrite cycles. These devices create a short-circuit path between VDD and GND when WE is low, providing a median potential (VDD/2) at WBL. Due to the thick oxides and long channel-lengths of the I/O devices, process variations are significantly reduced, and the static current is extremely low. Based on the chosen transistor sizes, the static power consumption of the proposed WBL driver during nonwrite cycles is only a few femtowatts under a 900-mV supply voltage, which is negligible compared with the refresh power of the array.

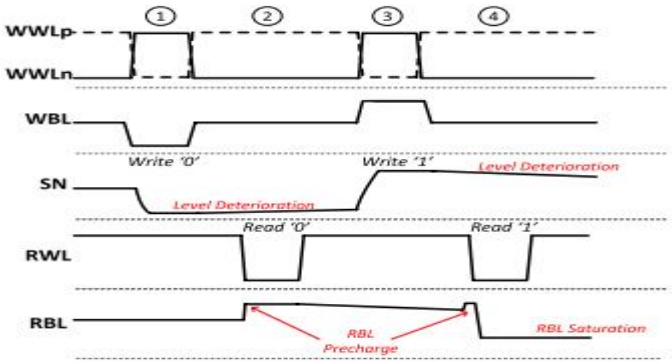

Fig. 6. Timing diagram of subsequent write and read operations. ① Write 0.② Read the stored 0. ③ Write 1.④ Read the stored 1. Plots extracted from Specter simulations with nominal parameter values

IV. SIMULATION RESULTS

This section describes the performance of the proposed design using MICROWIND/DSCH tool on 0.18-µm CMOS technology and simulation results using HSPICE tool on 0.18-µm technology. The simulated output of the 3T Gain Cell is shown in figures.

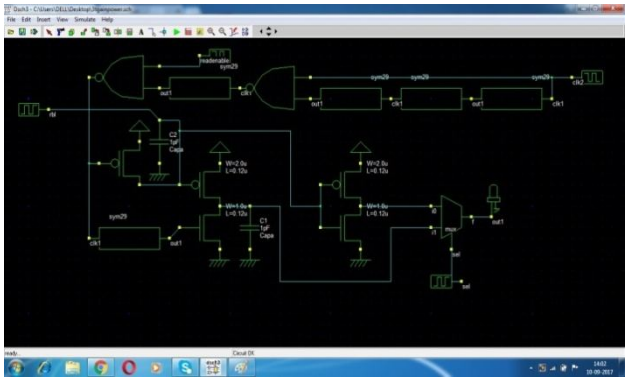

Fig:7 Schematic diagram of existing method

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Fig:8 output waveforms of existing method

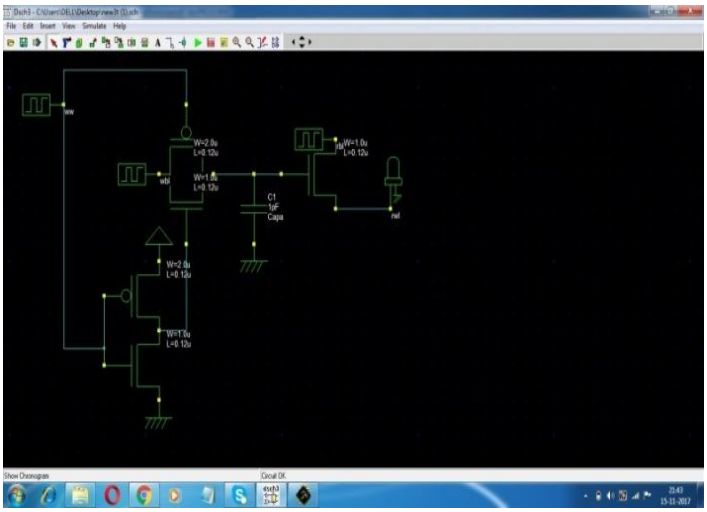

Fig:9 Schematic diagram of existing method

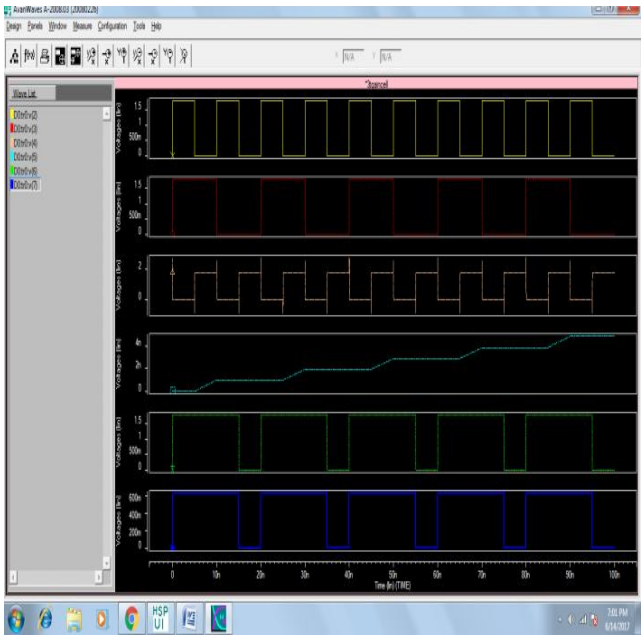

Fig:10 output waveforms of existing method

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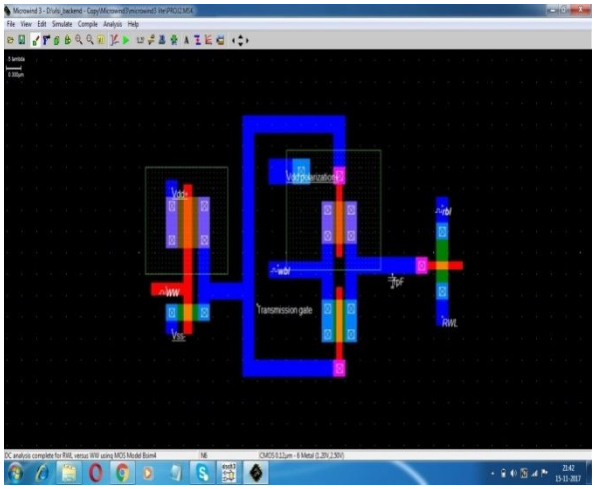

Fig 11: Layout of proposed method

V. CONCLUSION

This brief proposes a novel 3T GC eDRAM macro cell targeted at ULP systems and providing high storage density. The proposed GC is operated from a single-supply voltage, eliminating the need for boosted voltages, commonly found in prior-art implementations. The proposed cell exhibits faster write-access than conventional GC circuits, while minimizing CI and CF through effects, thereby increasing DRTs and reducing refresh power consumption. A test-chip containing a 2-kb memory macro based on the proposed 3T GC was fabricated in a mature 0.18-µm CMOS technology and several chips were tested. Measurement results show full functionality at voltages ranging from 600 mv to 1.8 V with retention power as much as 17× lower than a previously reported 8T SRAM in the same technology node.

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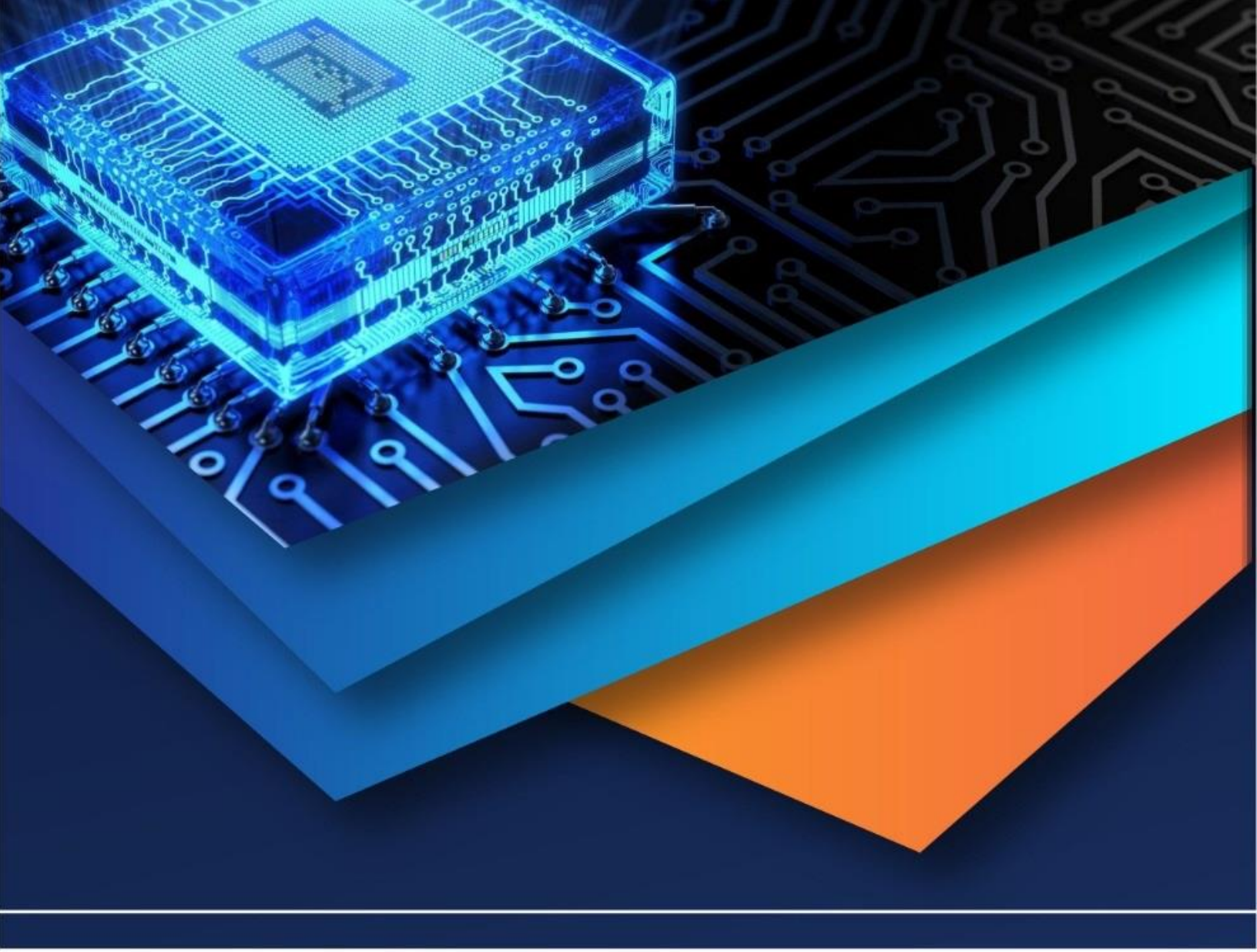

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