iJRASET
International Journal For Research in Applied Science and Engineering Technology



INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Volume: 2 **Issue:** Issue- II **Month of publication:** October 2014

DOI:

www.ijraset.com

Call: 08813907089 | E-mail ID: ijraset@gmail.com

International Journal for Research in Applied Science & Engineering Technology(IJRASET

CMOS Full adder Design in Submicron Technology With Low Leakage Power

P.Reddappa[1], K.Ganesh Naveen Kumar[2], N. Pushpalatha[3]

[1]M.Tech (DECS) Student, [2, 3]Assistant professor, Department of ECE,
Annamacharya Institute of Technology and Sciences, Tirupati, India-517520

***Abstract:** In designing of CMOS circuits contribution of scaling factor and power consumption plays a crucial role. The Proportionality relation between power and scaling improves the circuit performance .The performance of the circuit is degrade due to the leakage power, total power consumption is going monotonically in deep submicron Technologies. lately, the power density has improved due to combination of elevated clock speeds, greater efficient integration, and less significant process geometries. This shows major impact on static power consumption. This is a challenge for the layout designer. However, there are number of methods that are applied to reduce the static power consumption .But all of the methods have some drawback. In order to accomplish poor static power consumption, one has to sacrifice area of the layout and circuit performance. a new method is proposed to reduce static power in the CMOS VLSI circuit using dual stack approach without being penalized in area requirement and circuit performance.*
Keywords—Dual sleep approach, state saving technique, stack effect, dual V-th, static power reduction.

I. INTRODUCTION

Some of Digital functional blocks are not always in active all time they are active for particular amount of time. Leakage power exists even though functional block is not operating particularly in deep submicron technologies, leakage power is very serious problem due to the reduced voltage from scaling. 40% of total power is wasted by the leakage in today's high performance logic circuits. So, leakage power plays a vital role in low power design. For achieving high density and high performance threshold voltage and scaling down is have been used from decades. Transistor leakage Power has increased monotonically due to technology scaling. sub-threshold leakage current increases due to shorter channel lengths and low threshold voltage and transistor completely turned off .Consideration of all above reasons make new way to leakage power consumption and total power consumption problems.No.of technologies are there to reduce this leakage power but each one have some advantages and disadvantages of its own. For that reason we are going to provide a new solution to reduce the leakage power consumption in this paper.

II. SUB MICRON TECHNOLOGY

Mixed signal front-end systems are formed by using deep submicron CMOS technologies. These are the circuits which we use widely today in all applications.They provide the required integration density, they are very harm due to its radiation effect. The micron size and thickness reduction of both gate and isolation of dielectric layers, The above properties make CMOS devices less susceptible to ionization of layers.if we consider the analog performances of a circuit the methods for scaling of devices indicate along the need of understanding the noise properties of transistors with a few lengths of micron channel. The formation of this research program, perform static and, mainly, characteristics of the noise in deep submicron CMOS technologies. The short channel effects and parasitic noise contributions between resistance of a substrate and gate are most important considerations. The submicron technology characteristics make a way to CMOS processes with minimum channel lengths like 355, 240, 190, 120, 85 and 70 nm. In the case of the 120, 95 and 60 nm technologies, the thickness of gate oxide is below 3 nm, a deep analysis on the properties of the CMOS devices fabrication,direct tunneling of gate current has been performed.

III. FULL ADDER CIRCUITS

The circuit reliability and immunity to noise is depend upon it's static logic style. The no. of transistors in a circuit can be reduced by Pseudo NMOS and Pass-transistor logic. But the static power consumption problems are more in these type logic circuits. The advantages of pass transistor logic plays a vital role in multiplexers and XOR based circuits. A small silicon area is required for the dynamic logic implementation of complex functions. The CMOS 28 transistor adder shown in Figure 1,

main consideration of this paper. The size of a transistor is defined as a ratio of Width Length (W/L). It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is two for an inverter. Further, one of the techniques to reduce the leakage power is power gating. The power gating uses a sleep transistor this is connected between actual ground and circuit ground. when the circuits are connected with a sleep transistor ground bounce noise is estimated. The sizing will reduce the standby leakage current greatly because sub-threshold current is directly proportional to the Width/Length ratio of transistor. On the other hand, the area occupied by the circuit is going to shrinks. This will reduce the area occupied by the silicon chip and in turn reduction in the cost.

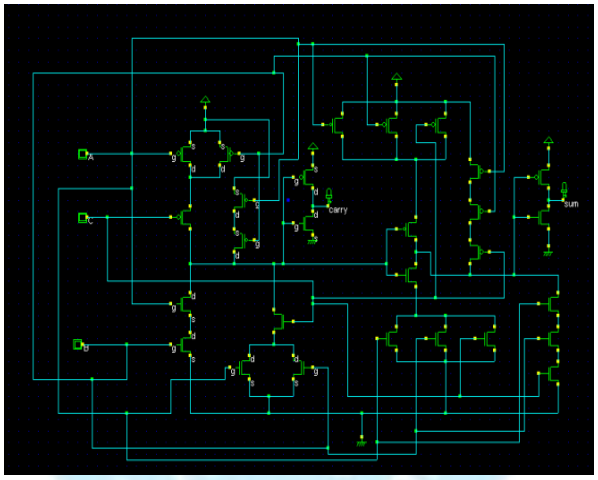


Figure 1. Conventional CMOS full adder

Modified adder circuit of Design 2 shown in Figure 3, The aspect ratio (W/L) is an important choice for the selection of PMOS and NMOS transistors. The W /L ratio of PMOS is 1.5 times that of W /L ratio of NMOS and each block has been treated as an equivalent inverter. an inverter circuit outputs a voltage representing the opposite logic-level of its input. These can be constructed using a NMOS transistor or a single PMOS transistor coupled with a resistor. Since this 'resistive-drain' approach uses only a single type of transistor, which was manufactured for least cost. However, current flows along the resistor in one of these two states, the resistive-drain configuration have seviour effect for power consumption and processing speed. inverters can be made using one pmos and one nmos transistors. This will the reduces power consumption since one of the transistors is always off in both logic states. The speed of processing can also be improved due to the relatively low resistance compared to the NMOS-only or PMOS-only type devices. The goal of this design is to reduce the standby leakage power. Further compared to the Basic analysis, Design 1 and Design 2, ground bounce noise produced when a circuit is connected to sleep transistor is reduced.

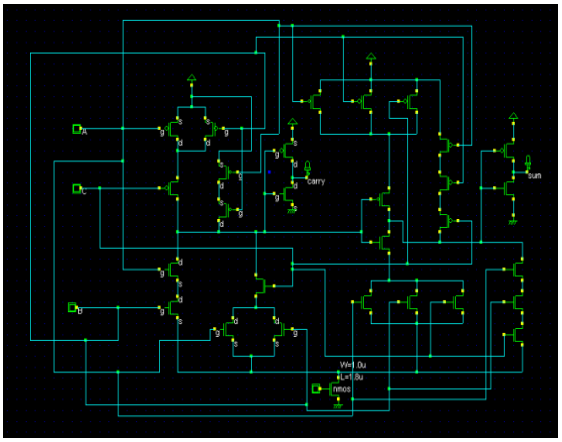


Figure 2. Full adder (Design I) circuit with sleep transistor

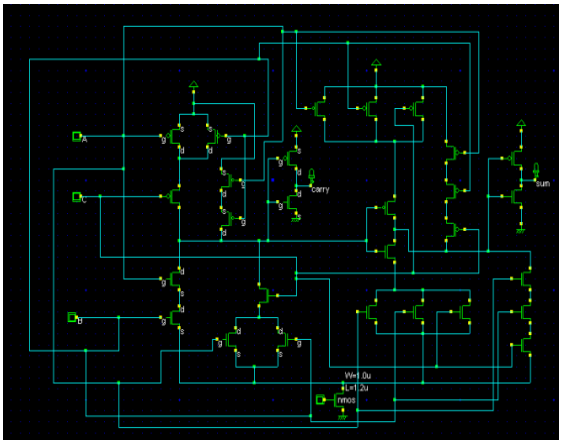


Figure 3. Full adder (Design2) circuit with sleep transistor

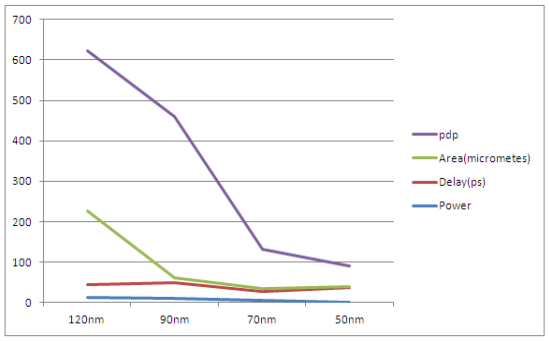


Figure 4. Conventional cmos power and area calculations.



Figure 5. Design 1 power and area calculations.

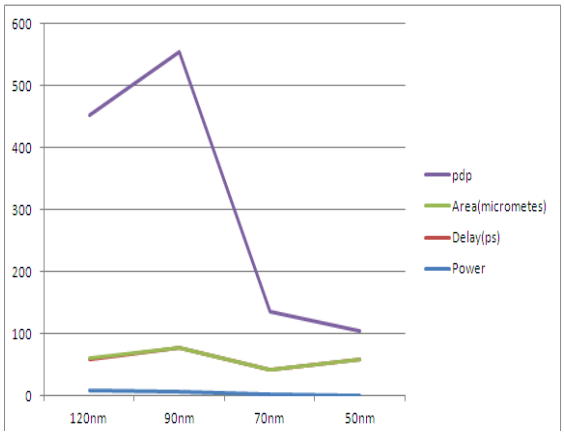


Figure 6. Design 2 power and area calculations.

A. Junction leakage

The junction leakage occurs between the drain or source to the substrate through the reverse biased diodes when a transistor is turned off. A reverse-biased pn junction leakage has two main categories: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction. For instance, in the case of an inverter with low input voltage, the NMOS is going to OFF, and at the same time the PMOS is going to ON, hence the and the output voltage is logic "1" i.e is high. and the drain-to-substrate voltage of NMOS transistor is equal to the supply voltage. It will results a leakage current from the drain to the substrate through the reverse-biased diode.

B. Gate-Induced Drain Leakage

The gate induced drain leakage (GIDL) is caused by high field effect in the drain junction of MOS transistors. For an NMOS transistor for which gate is going to grounded and drain potential at VDD allows electron-hole pair generation through avalanche multiplication and band-to-band tunneling. Holes are rapidly going out of the substrate results a null effect depletion condition, at that moment, drain is going collect the electrons, which results GIDL current. This type of leakage power mechanism is made worse by high drain to body voltage and high drain to gate voltage.

C. Gate Direct Tunneling Leakage

The gate leakage flows from the gate through the "leaky" oxide insulation to the substrate. In oxide layers thicker than 2–4 nm, kind of current results from the electrons tunneling into the conduction band of the oxide layer under a high applied electric field across the oxide layer. For lower oxide thicknesses (which are typically found in 0.15µm and lower technology), direct tunneling along the sio2 layer is caused for effect of tunneling. The direct tunneling through the silicon oxide includes electron tunneling in the conduction band (ECB), electron tunneling in the valence band (EVB), and hole tunneling in the valence band (HVB), among which ECB is the dominant one. The amount of the direct tunneling through the gate increase current exponentially with the gate oxide thickness.

D. Leakage control in standby circuits

Micro electronic systems spend considerable state. The energy consumed by the time in a standby logic and the DC-DC converter to enter or exit a low power mode must be considered carefully. If the cost of transitioning to and from a low standby power state is low enough then the greedy policy of entering the low power state as soon as the system is idle may be adopted. Otherwise, the expected duration of the standby state must be accurately calculated and taken into account when devising a power management policy.

E. Power Gating and Multi-Threshold CMOS

The best way of reducing the leakage power dissipation of circuits in the STANDBY mode is to switch off its voltage supply. It can be done by using one PMOS transistor and one NMOS transistor in series with the transistors of each logic block to create a virtual ground and virtual power supply as depicted in Figure 7. Notice that in practice only one transistor is necessary because of their on-resistance is smaller, NMOS transistors are usually used.

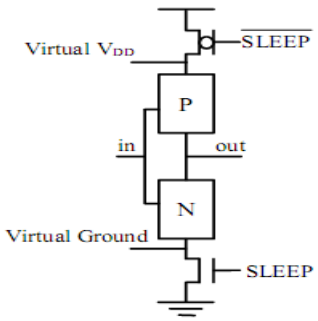


Fig 7 Power gating Circuit

In the ACTIVE state, the sleep transistor is going to on. Therefore, the circuit functions as normally. In the STANDBY mode, the transistor is switched off, which disconnects the gate from the ground. Note that lower the leakage power, the sleep transistors threshold must be large. Otherwise, the leakage current in sleep transistor will have a high value, which will make the

power gating less effective. power consumptions may be reduced if the width of the sleep transistor is smaller than the combined width of the transistors in the pull-down Network.

IV. PERFORMANCE ANALYSIS

A. Active Power

Voltage scaling is perhaps the most effective method of saving power due to the square law dependency of digital circuit active power on the supply voltage. Regrettably, scaling VDD also reduces the circuit speed since the gate drive, VGS – VT, is reduced. To deal with this, systems may exploit dynamic voltage scaling to allow the lowest VDD necessary to meet the circuit speed requirements while saving the energy used for the computation. Different combination of inputs are applied to the circuit and average power dissipation is measured. and the same inputs have been given to all three designs Base case, Design 1 and Design2, and a comparison has been made for the same in both 80nm and 90nm technology.

B. Standby leakage power

Standby leakage power present in the circuit and it is measured when the circuit is in standby mode. The full adder circuit is connected to sleep transistor of the pull down network. When the input voltage is applied sleep transistor is going to OFF, and the size of the largest transistor in the circuit is equivalent to the size of the sleep transistor. Due to the resizing of the adder cells the sleep transistor size reduced as shown in Design1 and Design2 .By applying different input combination to the circuit Stand by leakage power is going to be measure. As shown in Design1 and Design2 both are in 80nm and 90nm.

C. Four bit adder active and standby power

Four bit Full adder circuit is designed by using the Cmos and Nmos gates the design Full adder cells shown in Figure 1, 2 and 3 are used to design 4-bit ripple carry adder. 4-bit adders in all three designs- Conventional, Design 1 and Design2, for both 90nm and 65nm technology, are constructed. The active power and standby power are calculated. Active power is calculated by setting the Select terminal of the adder to logic high and Standby power is calculated by setting the Select terminal to 0V. Comparison of active and standby power of all the designs in both 80nm and 90nrn as shown in figure.

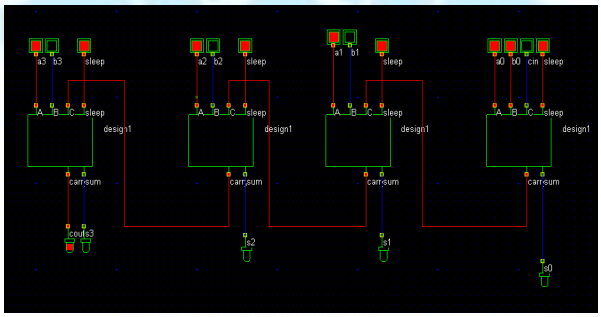


Fig 10: four bit adder design using single sleep approach

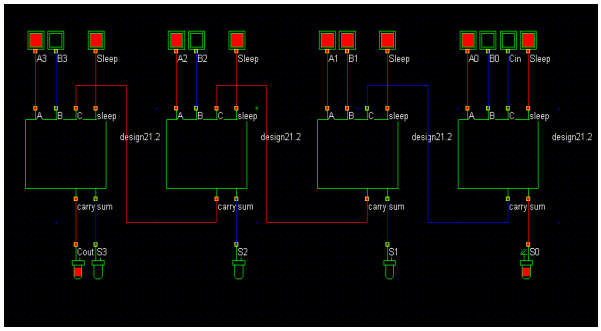


Figure 11: layout design for four cmos full adder using single sleep

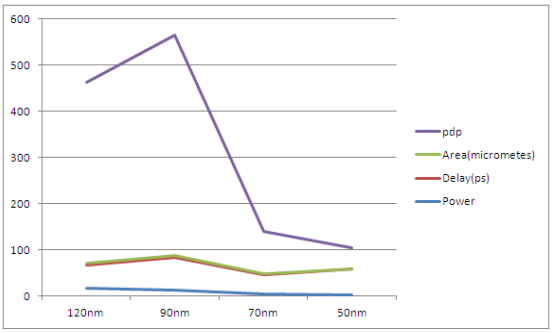


Figure 8. Design 1 power and area calculations

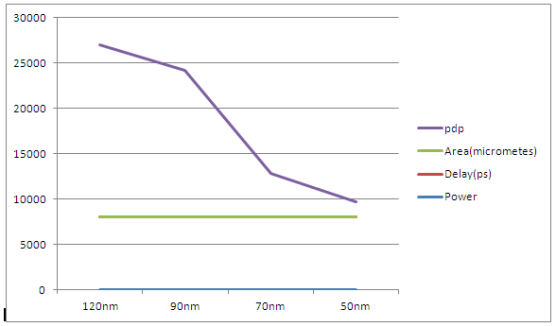


Figure 9. Design 2 power and area calculations

V. PROPOSED DESIGN

We here review previously proposed circuit level approaches for sub-threshold leakage power reduction.

A. Dual Sleep Approach

Dual sleep approach uses the advantage of using the two
extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit.

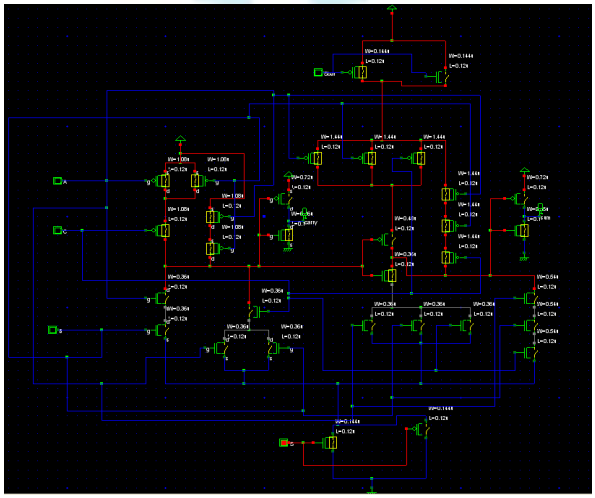


Fig 12: I bit full adder using dual sleep approach

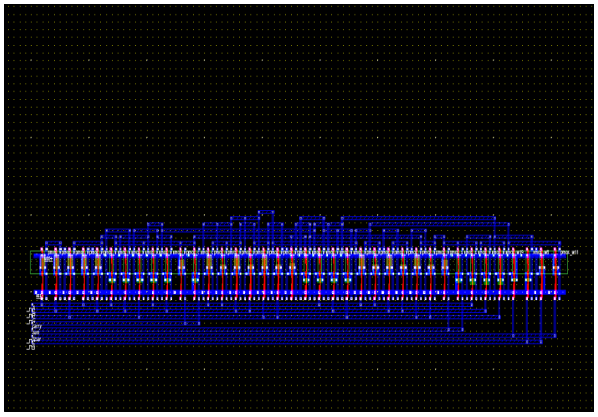


Fig 13: layout for 1 bit full adder using dual sleep approach.

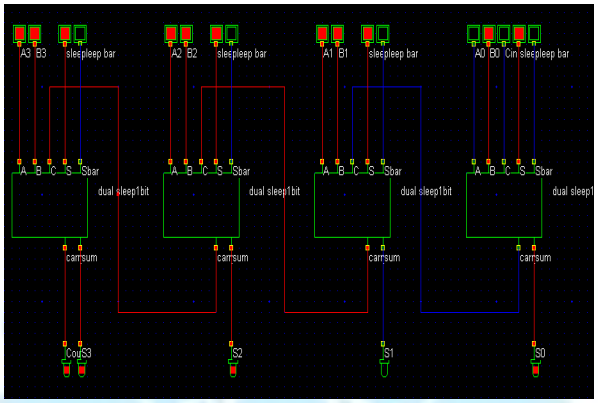


Fig 14: four bit full adder design using dual sleep approach

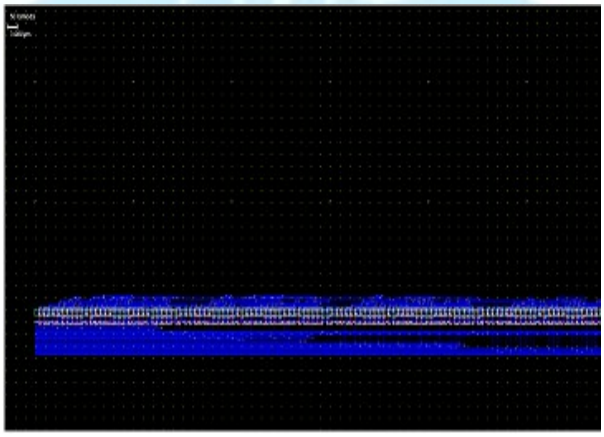


fig 15: layout for four bit full adder design using dual sleep approach

V. SIMULATION METHODOLOGY

We compare the dual sleep technique with previous approaches explained earlier namely; conventional cmos, conventional cmos with sleep transistor, and ripple carry adder. Thus, we compare these design approaches in terms of power consumption (dynamic and static), delay and area.

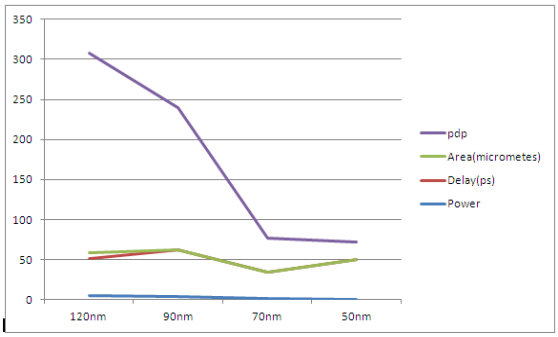


Fig 16: one bit full adder dual sleep approach power& area calculations

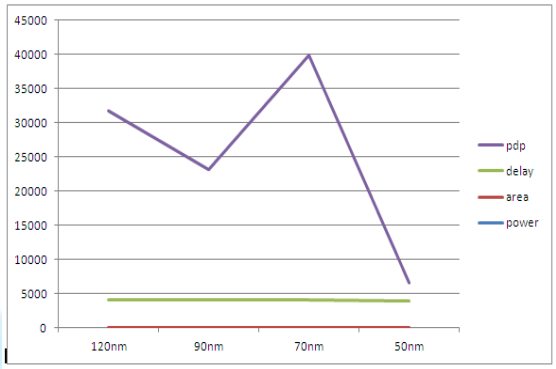


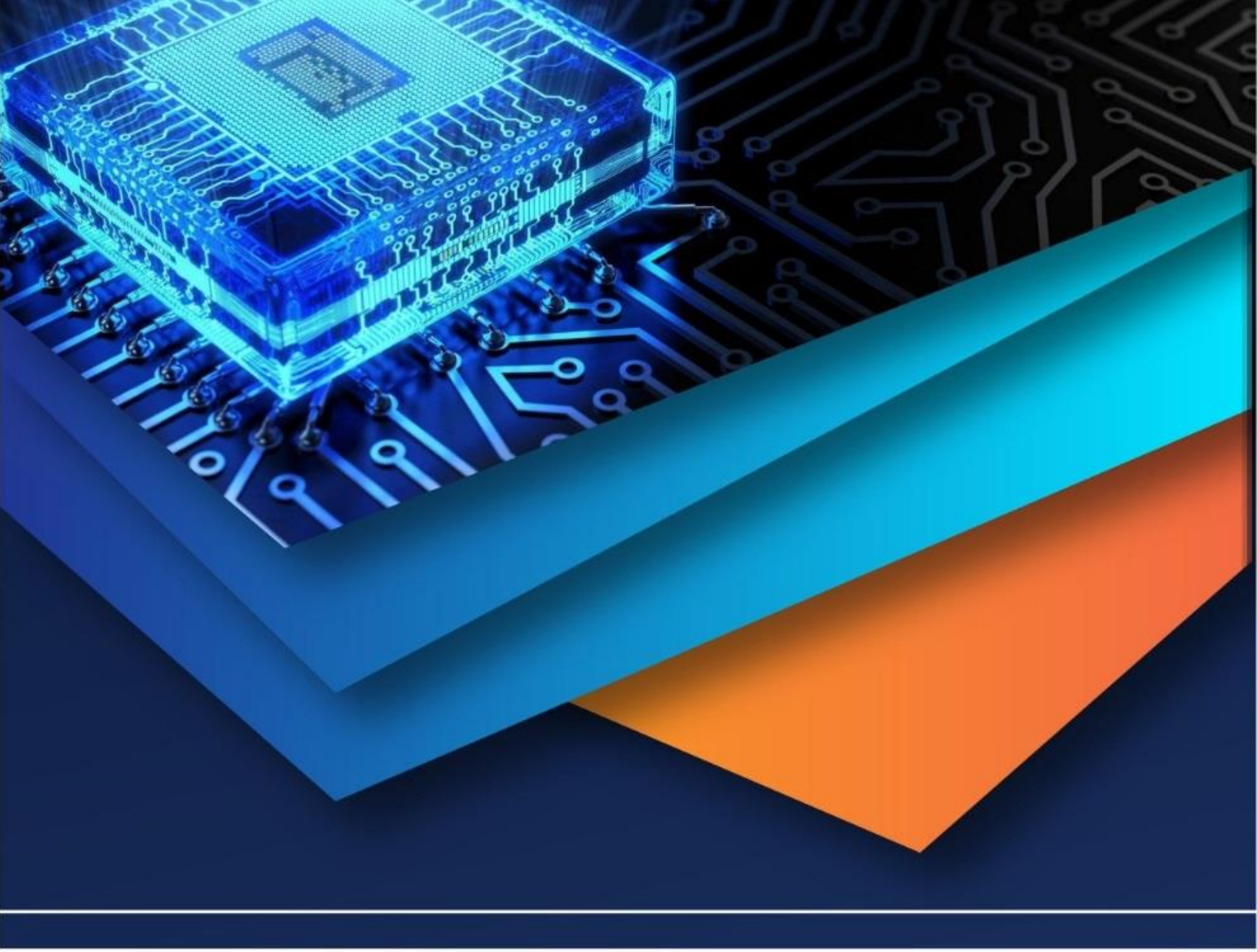
Fig17: four bit full adder dual sleep approach power & area calculations

VI. CONCLUSION

Miniaturization of CMOS technology achieving high performance has resulted in increase of leakage power dissipation. We have presented an efficient methodology for reducing leakage power in VLSI design. Our Dual sleep approach shows improved results in terms of static power, dynamic power and power delay product. It gives the CMOS circuit designers another option in designing integrated Circuits more efficiently.

REFERENCES

[1] S. Mutoh et al., "1-V Power Supply High-speed Digital Circuit Technology with Multi threshold-Voltage CMOS," IEEE Journal of Solis-State Circuits, Vol. 30, No. 8, pp. 847-854, August 1995.
[2] R. Gonzalez, B. Gordon, M. Horowitz, "Supply and threshold voltage scaling for low power CMOS,"
IEEE Journal of Solid State Circuits, Vol. 32, August 1997, pp. 1210-1216.
[3] T. Ishihara and H. Yasuura, "Voltage scheduling problem for dynamically variable voltage
processors," Proc. of Int'l Symp. on Low Power Electronics and Design, August 1999, pp.197-202.
[4] S. Lee and T. Sakurai, "Run-time power control scheme using software feedback loop for low-power
real-time applications," Proc. of Asia-Pacific Design Automation Conf., January 2000, pp.381-386.
[5] M.Powell, S.-H. Yang, B. Falsafi, K. Roy and T. N. Vijaykumar, "Gated-Vdd: A Circuit Technique to Reduce Leakage in Deepsubmicron Cache Memories," International Symposium on Low Power Electronics and Design, pp. 90-95, July 2000.
[6] K.Bernstein et aI., "Design and CAD challenges in sub-90nm CMOS technologies," in Proc. int. conf. compute. Aided Des., 2003, pp. 129- 136
[7] J.C. Park, V. J. Mooney III and P. Pfeiffenberger,"Sleepy Stack Reduction of Leakage Power," Proceeding of the International Workshop on Power and Timing Modeling, Optimization and Simulation, pp. 148-158, September 2004
[8] S G. Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies. New York: Springer-verlag, 2006.
[9] Ku He, Rong Luo, Yu Wang, "A Power Gating Scheme for Ground Bounce Reduction During Mode Transition, " in ICCD07, pp. 388-394,2007.
[10] K. Choi, R. Soma and M. Pedram, "Fine-Grained Dynamic Voltage and Frequency Scaling for Precise
Energy and Performance Trade-off based on the Ratio of Off-chip Access to On-chip Computation
Times," Proc. of Design Automation and Test in Europe, February 2004, Vol. 1, pp. 10004.
[11] R. Gonzalez, B. Gordon, M. Horowitz, "Supply and threshold voltage scaling for low power CMOS,"
IEEE Journal of Solid State Circuits, Vol. 32, August 1997, pp. 1210-1216.



10.22214/IJRASET

45.98

IMPACT FACTOR: 7.129

IMPACT FACTOR: 7.429

INTERNATIONAL JOURNAL FOR RESEARCH

IN APPLIED SCIENCE & ENGINEERING TECHNOLOGY

Call : 08813907089 (24*7 Support on Whatsapp)